MM101

8 Channel MEMS High Voltage Driver

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Product Overview

Description

The MM101 is an 8-channel low-voltage serial-to-high-voltage parallel converter with push-pull outputs and an internal charge pump converter. The device is designed for MEMS applications where high-voltage generation and driving capability are desired in a high integration form factor. The internal charge pump operates with a 5.0 V input source to generate a high-voltage source for the 8-channel output drivers.

The circuitry includes power-on-reset and power ON/OFF sequence control. The communication interface consists of two modes of operation: GPIO and SPI, selected with the input control MODE pin.

Features

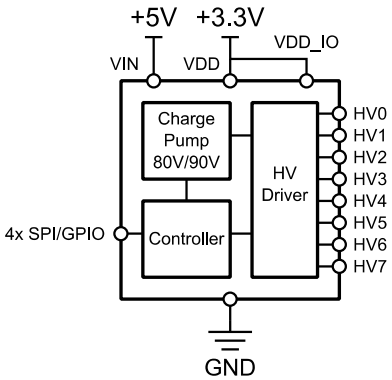
- Eight High-Voltage Push-Pull Output Channels
- Internal Charge Pump Voltage Converter
- Power-On-Reset (POR)
- Selectable Communication Interface (SPI, GPIO)
- Up to 33 MHz SPI Clock Speed
- V_{DD_IO} Supply allows I/O levels to range from 1.8 V to 5.0 V
- SPI can be daisy-chained
- Under Voltage Protection
- Fault Indicators (Latched SPI register bit and unlatched Open-Drain FLTB pin)
- Available in a 5x5mm QFN package, and WLCSP Flip Chip package

Applications

- Microelectromechanical Systems
- Displays
- High Voltage Driver Applications

Markets

- Load/DIB for Semiconductor Test
- RF Systems
- Test and Measurement



Typical Applications

Dotted lines indicate optional components and connections.

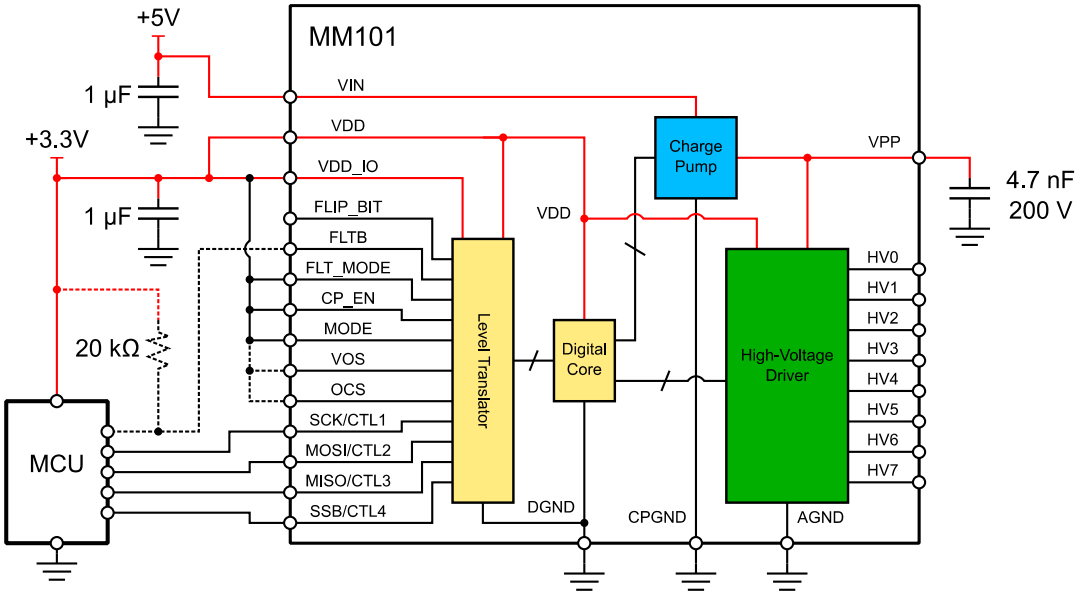


Figure 1: Application Circuit – GPIO

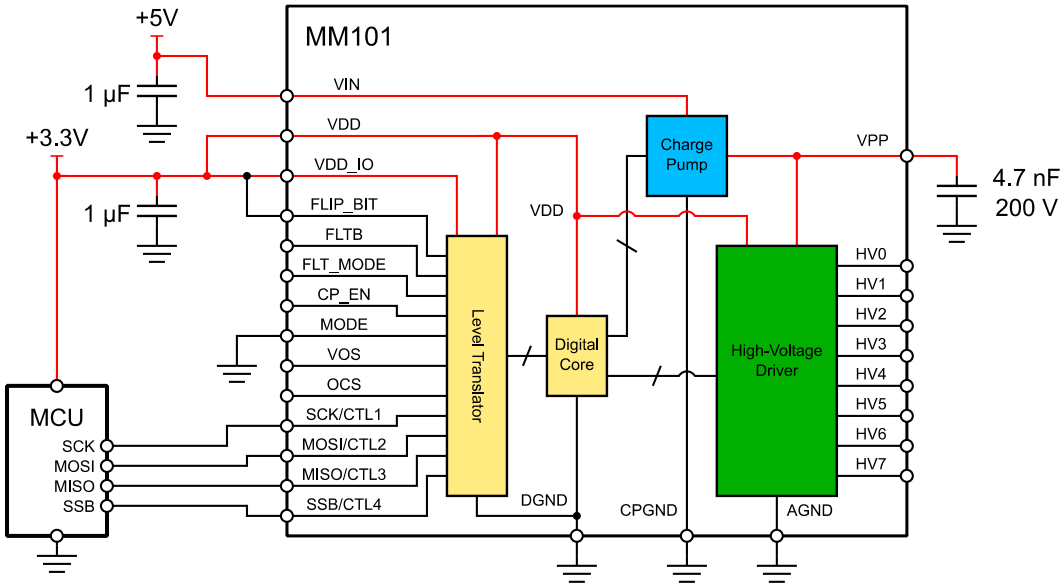


Figure 2: Application Circuit – SPI

Electrical Specifications

Operating Characteristics

Absolute Maximum Ratings

Exceeding the maximum ratings as listed in Table 1 below may reduce the reliability of the device or cause permanent damage. Operation of the MM101 should be restricted to the limits indicated in the recommended operating conditions listed in Table 2

Electrostatic Discharge (ESD) Safeguards

The MM101 is a Class 1A ESD device. When handling the MM101, observe precautions as with any other ESD sensitive device. Do not exceed the voltage ratings specified in Table 1.

Power Sequencing

When using the internal charge pump, no specific power sequencing is required for power-up or power-down. When using an external high-voltage supply, see below.

Power-up Sequence

1. Connect Ground.
2. Apply V_{DD}, V_{DD_IO}, and V_{IN} – no supply sequencing restrictions on V_{DD}, V_{DD_IO}, and V_{IN}.
3. Apply V_{PP} (if using external high voltage supply).
4. Apply input control signals.

Power-down Sequence

Reverse the power-up sequence.

Table 1. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Charge Pump Power Supply	-0.3	5.5	V
Digital Power Supply	-0.3	3.6	V
Logic Reference Level	-0.3	5.5	V
High Voltage Power Supply	-0.3	105	V
Logic Input Levels	-0.3	V_{DD_IO} + 0.3	V
ESD Rating HBM Control and Power Pins	—	2000	V HBM
ESD rating of VPP & HV# pins	—	500	V HBM
Junction Temperature Range	-55	165	°C
Storage Temperature Range	-55	165	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Charge Pump Power Supply	V_{IN}	4.5	5.0	5.5	V
Digital Power Supply	V_{DD}	3.0	3.3	3.6	V
Logic Reference Level	V_{DD_IO}	1.71	—	5.25	V
High Voltage Power Supply[1]	V_{PP}	10	—	100	V
Operating Temperature	T_A	-40	—	125	°C
SPI Clock Frequency	f_{SCK}	—	—	33	MHz
HV0-7 Load Resistance[2]	R_L	40	—	—	MΩ

Notes:

1. When using an external high voltage supply.
2. For internal charge pump operation, VOS = 1, OCS = 0, single HV output on test condition. Standard 10 MΩ multimeter and oscilloscope probes will exceed this rating and cause VPP voltage droop. Use high-impedance (100 MΩ or higher) probes to measure HV outputs.

Electrical Characteristics

All specifications valid over full supply voltage and operating temperature range unless otherwise noted (Note 1). Operating with all analog and digital GND pins connected to system ground (0 V). VPP = 85 V, CPP = 4.7nF, unless otherwise specified.

Table 3. Power Supply Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Conditions
VIN Current (Dynamic)	I_{VIND}	—	1.5	2.5	mA	CP ON, V_{PP} = 85 V, outputs switching at 10 kHz, C_L = 2 pF per CH
VIN Quiescent Current	I_{VINQ}	—	1.25	2.0	mA	CP ON, V_{PP} = 85 V, all I/O static
VDD UVLO Rising Threshold	$UVLO_{RISE}$	2.77	—	2.95	V	
VDD UVLO Falling Threshold	$UVLO_{FALL}$	2.72	—	2.90	V	
Low Voltage Digital Current	I_{DD}	—	520	700	µA	SPI mode outputs switching at 10 kHz, OCS = 0, C_L = 2 pF per CH.
Low Voltage Digital Quiescent Current	I_{DDQ}	—	470	550	µA	CP OFF, all I/O static
Low Voltage Digital Sleep Mode Current	$I_{DDSLEEP}$	—	<1	10	µA	CP OFF, Sleep Mode ON
I/O Logic Supply Current	I_{DD_IOQ}	—	<10	50	µA	Outputs switching at 10 kHz.

Table 4. Digital Interface AC and DC Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
Logic I/O Level High	I/O_{VH}	0.7 x V_{DD_IO}	—	V_{DD_IO}	V	
Logic I/O Level Low	I/O_{VL}	0	—	0.3 x V_{DD_IO}	V	
Logic I/O Hysteresis (SCK only)	I/O_{HYS}	—	0.25	—	V	
Digital Input Capacitance (MM101-03ADA)	C_{IN}	—	2	5	pF	
MISO Load Capacitance[3]	C_{MISO}	—	—	10	pF	
MISO Source Current @ V_{DD_IO}						VOUT = 0.8 x V_{DD_IO}
5.0 V	I_{MISOH}	180	290	—	mA	
3.3 V		75	140	—	mA	
1.8 V		20	35	—	mA	
MISO Sink Current @ V_{DD_IO}						VOUT = 0.2 x V_{DD_IO}
5.0 V	I_{MISOL}	140	260	—	mA	
3.3 V		65	140	—	mA	
1.8 V		20	40	—	mA	
SSB pull-up resistor (to V_{DD_IO})	R_{PU}	120	200	280	kΩ	SSB pull-up is only in SPI mode
Internal pull-down resistors[5]	R_{PD}	120	200	280	kΩ	SSB pull-down is only in GPIO mode
CP_EN pin toggle low time	T_{TOGGLE}	500	—	—	ns	Minimum time CP_EN must be held low to re-start the IC from fault condition
FLTB pin max sink current		65	140	—	mA	FLTB = GND V_{DD_IO}=3.3V

Table 5. Digital Interface Timing Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
MOSI Valid to SCK Setup Time	t_{SU}	2	—		ns	
MOSI Valid to SCK Hold Time	t_{HD}	5	—		ns	
SCK High Time	t_{HI}	15.5	—	—	ns	
SCK Low Time	t_{LO}	15.5	—	—	ns	
SSB Pulse Width	t_{CSH}	15	—	—	ns	
LSB SCK to SSB High	t_{CSHLD}	15	—	—	ns	
SSB Low to SCK High	t_{CSSU}	15	—	—	ns	
MISO Propagation Delay from SCK Falling Edge	t_{MISOH}	10	—	—	ns	C_L = 10pF
MISO Output Valid after SSB Low	t_{CMISO}	20	—	—	ns	
SSB Inactive to MISO High Impedance	t_{MISOZ}	—	—	10	ns	

Table 6. Charge Pump and Driver Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Test Conditions
High Voltage CP Output						
VOS = 0	V_{PP}	77	80	83	V	
VOS = 1		87	90	93	V	
Charge Pump Output Ripple	V_{RIPPLE}	—		10	mV_{p-p}	All HV Driver Outputs Off
Droop in V_{PP} Voltage	V_{DROOP}	—	—	0.6	V	Droop in V_{PP} Voltage when 8 HV outputs toggle on, C_L = 3.5pF
Power-On-Reset	POR	—	<0.5	2.50	ms	Delay from application of VIN and VDD to all circuits active and stable
Charge Pump Start-Up Time[4]	T_{ST}	—	8	33	ms	V_{IN} = 4.5 V, V_{PP} = 90 V, I_{OUT} = 20 uA, C_{PP} = 4.7nF
Driver Output Voltage High	HV_{OH}	V_{PP}-1	—	—	V	
Driver Output Voltage Low	HV_{OL}	—	—	1	V	
Driver Output Current	$I_{HV\#}$					Per channel V_{PP} = 85 V
OCS = 0		24	30	36	µA	
OCS = 1		48	60	72	µA	
Output Enable Rising Threshold	V_{EN}					
VOS = 0		65	69	71	V	
VOS = 1		75	79	81	V	
Output Disable Falling Threshold	V_{DIS}					
VOS = 0		64	68	70	V	
VOS = 1		74	78	80	V	

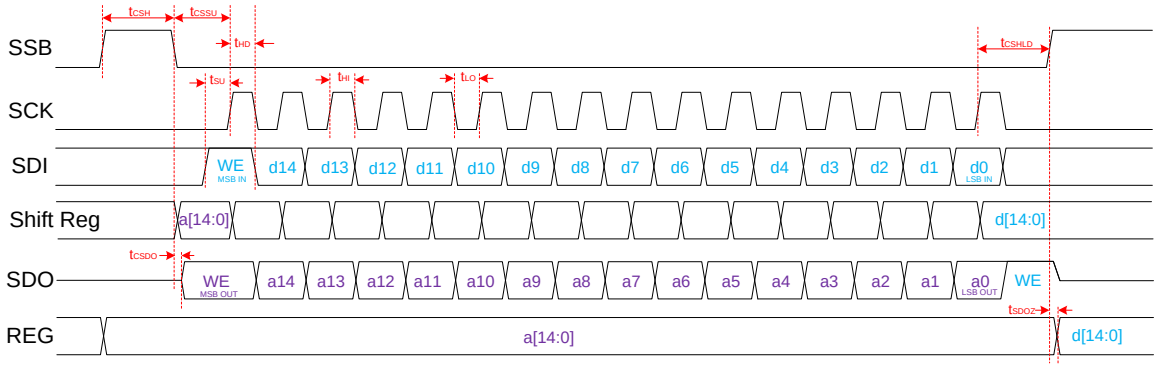


Figure 3. SPI Timing Diagram

Functional Block Diagram

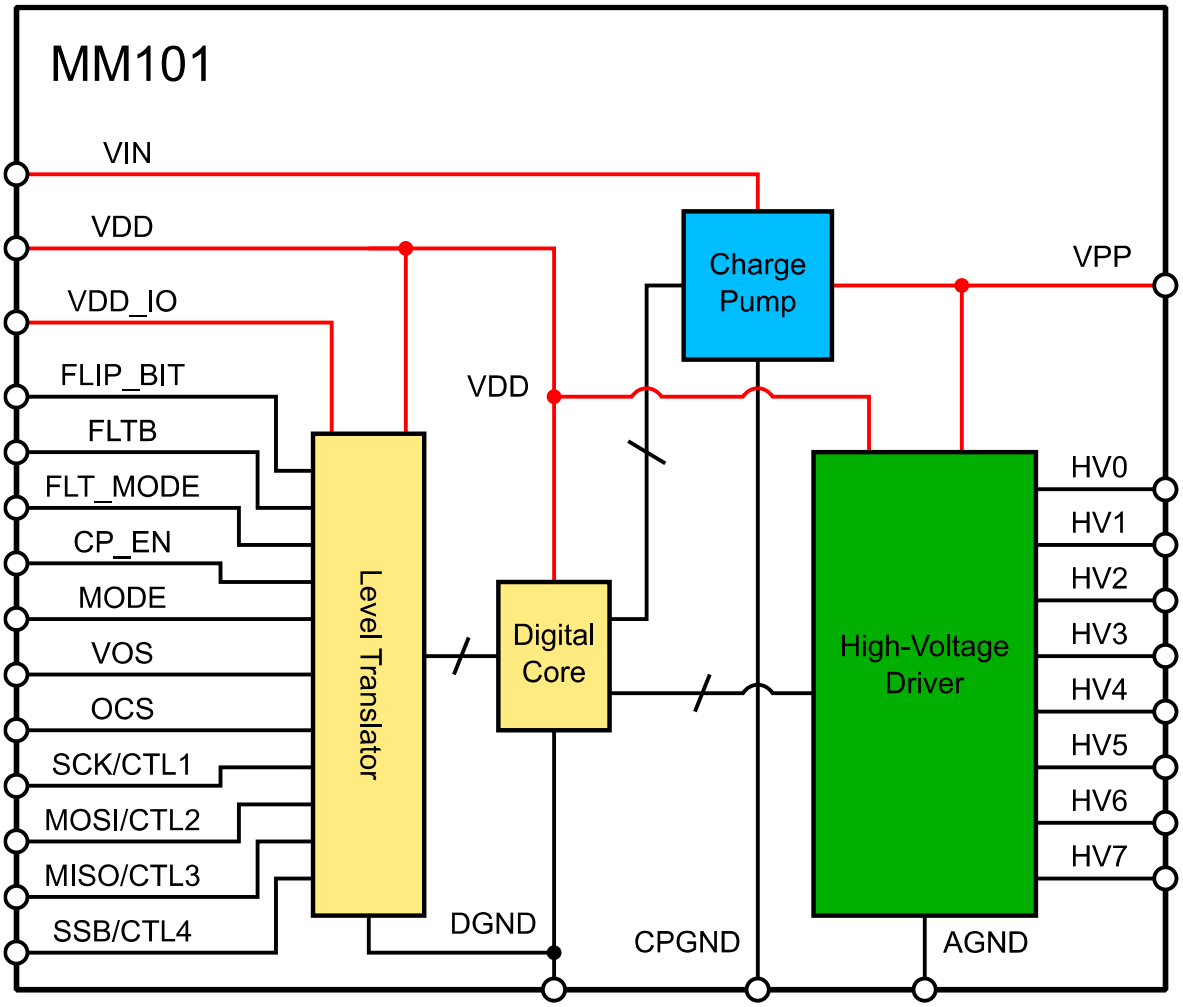


Figure 4. Functional Block Diagram

32-Lead QFN Package Pinout

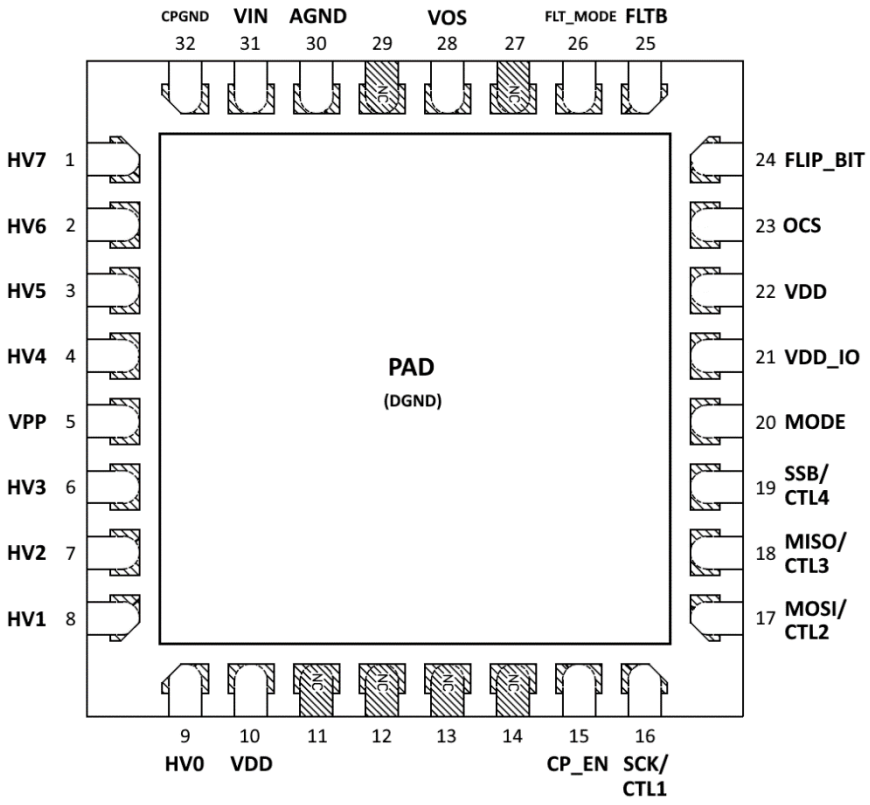


Figure 5. MM101 5 mm x 5 mm QFN Package Pinout (Top View/As Mounted)

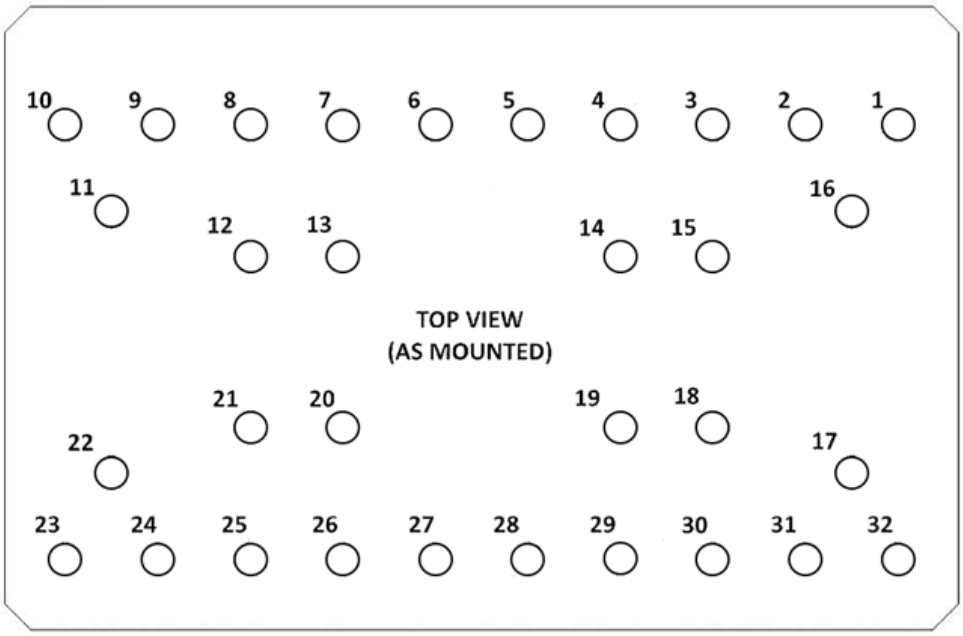


Figure 6. MM101 2.37 mm x 1.58 mm Flip-Chip Package Pinout (Top View/As Mounted)

Table 7. Detailed Pin Description

QFN Pin #	Flip Chip Pin #	Name	Description
1-4, 6-9	2-9	HV#	High-voltage outputs.
5	14, 15	VPP	High-voltage input to the output drivers. Bypass with a 4.7 nF, 200 V, 10 % C0G ceramic capacitor to AGND.
10, 22	1, 20, 21	VDD	3.3 V supply to digital/analog circuits. Bypass with a low ESR 1 µF ceramic capacitor to AGND.
11-14, 27, 29	32	NC	No connect, can optionally be connected to PCB ground.
15	17	CP_EN	Charge pump enable pin in GPIO mode. Pull-up to VDD_IO to enable the charge pump. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
16	31	SCK/CTL1	Clock input in SPI mode; HV output control in GPIO mode. Has an internal pull-down resistor.
17	30	MOSI/CTL2	SPI data input in SPI mode (SDI); HV output control in GPIO mode. Has an internal pull-down resistor.
18	16	MISO/CTL3	SPI data output in SPI mode (SDO); HV output control in GPIO mode. Has an internal pull-down resistor.
19	29	SSB/CTL4	Chip select in SPI mode; HV output control in GPIO mode. Has an internal pull-up resistor to VDD_IO in SPI mode, and an internal pull-down resistor in GPIO mode.
20	28	MODE	Logic level input to switch inputs between SPI and GPIO modes. Connect to GND for SPI mode. Connect to VDD_IO for GPIO mode.
21	27	VDD_IO	For 3.3 V nominal digital I/O levels, connect to VDD. For alternate I/O levels, connect to a separate supply (+1.8V to +5.0V). If separate from VDD, bypass with a low ESR 1 µF ceramic capacitor to DGND.
23	26	OCS	Output Current Select in GPIO mode. Connect to VDD_IO for high level or GND for low level. Has an internal pull-down resistor. Pin is ignored in SPI mode.
24	12, 13	FLIP_BIT	In GPIO mode FLIP_BIT controls the logic mapping between CTL1-4 and HV0-7. Refer to Table 8. Set high in SPI mode. Has an internal pull-down resistor.
25	25	FLTB	Fault indicator in GPIO and SPI modes. Open drain output to allow “Wire-OR” of multiple ICs. Goes low when fault is detected. Can be left open if not used. Pull-up voltage must be ≤ VDD_IO.
26	22	FLT_MODE	Fault Mode select in GPIO mode. Pull to VDD_IO to disable Fault Mode. Has a built-in pull-down resistor. Pin is ignored in SPI mode.

QFN Pin #	Flip Chip Pin #	Name	Description
28	23	VOS	Output voltage select in GPIO mode. Connect to VDD_IO for high level or GND for low level. Has a built-in pull-down resistor. Pin is ignored in SPI mode.
30	24	AGND	Analog ground, should be connected to PCB ground.
31	10	VIN	Connect to 5 V power supply. Bypass with a low ESR 1 µF ceramic capacitor to CPGND.
32	11	CPGND	Charge pump ground, should be connected to PCB ground.
PAD	18, 19	DGND	Digital ground, should be connected to PCB ground.

Functional Description

The MM101 is an 8-Channel Low-Voltage Serial to High-Voltage Parallel Converter with Push-Pull Outputs and an Internal Charge Pump Converter. The device is designed for MEMS applications where high voltage generation and driving capability are desired in a high integration form factor.

The device consists of three main design blocks:

- Internal charge pump
- Communication interface
- 8 high-voltage push-pull drivers

Charge Pump

The internal charge pump operates from a 5.0 V nominal input to generate the high voltage VPP for the HV Drivers. The output voltage can be selected to be either 90V or 80V using the VOS pin in GPIO mode or VOSET bit in SPI mode.

The VOS pin has a low current internal pull-down to GND. If the pin is left open or connected to GND, the output voltage defaults to 80 V. Pulling the pin to V_{DD_IO} sets the output high level to 90 V. Likewise, in SPI mode, if the VOSET register bit is zero, the output level (HV#) high levels are 80 V. If VOSET is set to 1, the HV# output levels are 90 V.

To measure the VPP or HV outputs accurately, a load resistance greater than 40 MΩ (including probes or other test equipment) is required. Standard 10 MΩ multimeter and oscilloscope probes will exceed this rating and cause VPP voltage droop. Use high-impedance (100 MΩ or higher) probes to measure HV outputs.

Supplying an External High Voltage

If it is desired to use an external voltage instead of the internal charge pump:

- VIN should be connected to CPGND.
- VPP should be applied 0.1 msec or more after VDD is applied.
- VOS pin should be set according to the VPP voltage that will be applied externally (80 V/ 90 V). This will ensure that the internal VPP under-voltage comparators function correctly.
- When using an external supply to drive VPP in GPIO mode, the status of the CP_EN pin affects VPP under voltage faults.

High Voltage Outputs

The eight high-voltage outputs are powered from VPP and controlled by the digital inputs.

In SPI mode, the output current may be set to either the low level or high level by using the OCS register bit. The default state of OCS is a logic zero, which sets the output current level to low. In GPIO mode, the output current level is determined by the state of the OCS pin.

The MM101 is designed to simultaneously drive the 8 high-voltage outputs with a total load capacitance of 10 pF. Multiple HV outputs can be tied together to increase the transient drive current, but the total load capacitance of all 8 HV outputs should be below 10 pF.

Programming

Communication Interface

The driver interface two modes of operation, Serial and GPIO (Parallel), selected by the MODE input pin.

Note: If MODE is toggled from GPIO to SPI, it is a good practice to pulse SSB low before the first 16-bit transaction. This will reset the SPI and ensure that it is ready to receive the first data packet.

All the SPI pins (except the SSB pin) the FLIP_BIT, and the MODE pin have an internal pull-down resistor to ensure that no digital input pins can float.

The SSB pin has a pull-up current source in SPI mode. This ensures that the IC defaults to a disabled state in SPI mode. In GPIO mode, this pin is CTL4. In this case, the CTL4 pin has a pull-down resistor. This ensures that the input is low by default in GPIO mode.

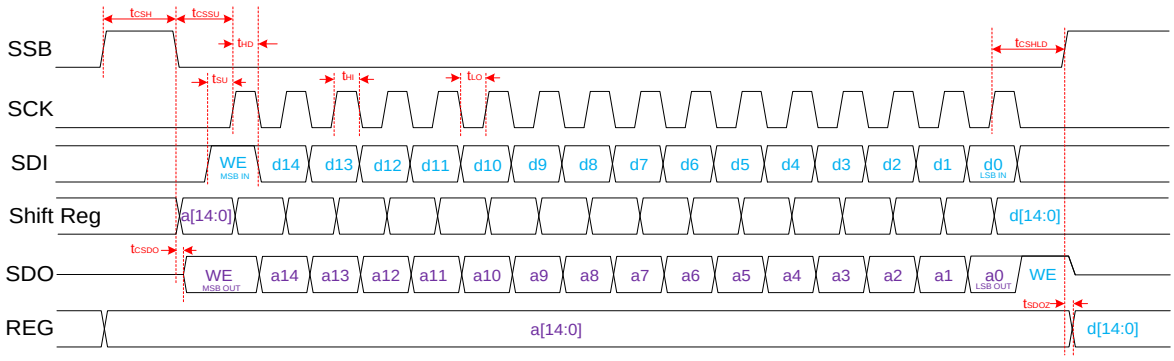


Figure 7. SPI Timing Diagram

Serial Communication

MODE = 0, activates the 16-Bit Serial Peripheral Interface (SPI) module for operation. Multiple devices can be daisy-chained to drive multiple ICs using one SPI bus. See Daisy Chain Operation Figure 10, Figure 11, and Figure 12.

The SPI works at any frequency up to a maximum of 33 MHz and may operate at significantly lower frequencies if the logic signals adhere to the data setup and hold requirements.

SPI Interface Mode

SPI timing diagrams are provided in Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, and Figure 12. In SPI mode, data transmission starts when SSB goes Low, causing the Target to output the Most Significant Bit (MSB) of data to the SDO (MISO) pin. Data transfer from Host to Target takes place during the rising edge of the clock (SCK), which is idle when SSB is High. This mode of operation requires data for Host and Target to be present on SDI (MOSI) before the rising edge of the clock (defining SDI to SCK setup time). Data is pushed out of the SDO (MISO) pin during the falling edge of the clock. After the first 16-bit transaction, Host writes the latest data (DN) to Target, while Target passes its previous (DN-1) stored data to the Host. Data is latched into the internal registers at the rising edge of SSB, if WR_EN = 1.

SPI Data Format

SPI data is sent in a 16-bit format. The first MSB bit (WE), if high, enables the Write mode. The following 7 MSB bits hold the Control and Fault Status bits. The 8 LSB bits hold the Switch State bits.

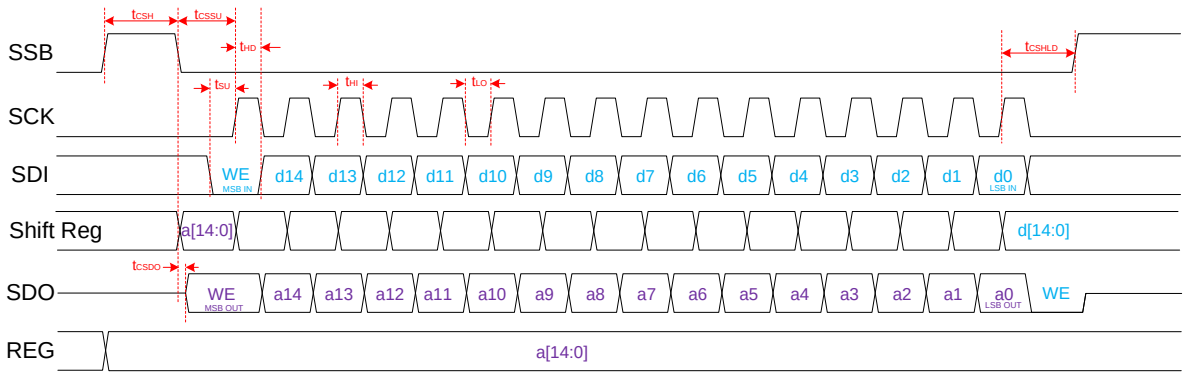


Figure 8. SPI Read Only (1 IC, No Daisy Chain)

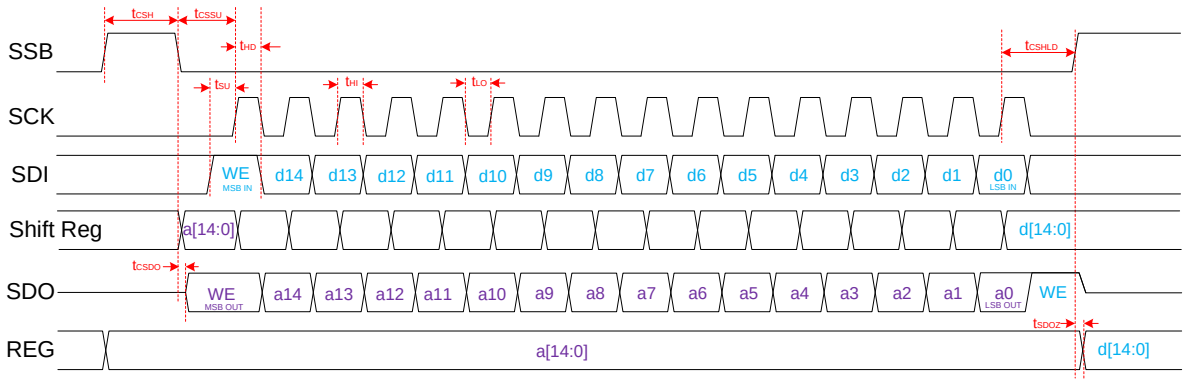


Figure 9. SPI Read & Write (1 IC, No Daisy Chain)

SPI Control Registers

The SPI interface provides access to two 8-bit Internal Registers: Register STATE and Register CONTROL that are Read/Write registers. Register data is read by toggling SSB low and monitoring the data at the SDO pin while clocking the SCK pin. Register STATE holds the state of the 8 high-voltage outputs and is updated when SSB goes from LOW to HIGH, if the Write Enable bit is high.

Register CONTROL holds six control bits (OCSET, CPEN, VOSET, VPPCOMP, FLT_MODE, and SLEEP), and the fault status bit (FSTAT). The MSB bit enables the Write mode if high.

In SPI mode, the OCS, VOS, CP_EN, and FLT_MODE pins are ignored. Settings in the CONTROL register are used instead.

Note: The first row of the register tables below shows the read/write type, and default state. At power-on-reset (POR), all bits in both registers are set to LOW internally.

State Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
HV7	HV6	HV5	HV4	HV3	HV2	HV1	HV0
bit 7							bit 0

bit 7: **HV7**

1 = HV7 Output is Enabled (High)

0 = HV7 Output is Disabled (Low)

bit 6: **HV6**

1 = HV6 Output is Enabled (High)

0 = HV6 Output is Disabled (Low)

bit 5: **HV5**

1 = HV5 Output is Enabled (High)

0 = HV5 Output is Disabled (Low)

bit 4: **HV4**

1 = HV4 Output is Enabled (High)

0 = HV4 Output is Disabled (Low)

bit 3: **HV3**

1 = HV3 Output is Enabled (High)

0 = HV3 Output is Disabled (Low)

bit 2: **HV2**

1 = HV2 Output is Enabled (High)

0 = HV2 Output is Disabled (Low)

bit 1: **HV1**

1 = HV1 Output is Enabled (High)

0 = HV1 Output is Disabled (Low)

bit 0: **HV0**

1 = HV0 Output is Enabled (High)

0 = HV0 Output is Disabled (Low)

Control Register

R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W - 0	R/W – 0
WR_EN	FSTAT	SLEEP	FLTMODE	VPPCOMP	VOSET	CPEN	OCSET
bit7							bit 0

bit 7: **WR_EN**
- 1 = Enable write mode
- 0 = Disable Write mode (read only)

bit 6: **FSTAT** (see Note 1 below)
- 1 = VPP OR VDD Fault status = faulted
- 0 = VPP OR VDD Fault status = NOT faulted

bit 5: **SLEEP** (see Note 2 below)
- 1 = SLEEP mode active (all analog circuits disabled)
- 0 = SLEEP mode inactive (all analog circuits enabled)

bit 4: **FLTMODE**
- 1 = Fault Mode Disabled (shutdown disabled)
- 0 = Fault Mode Enabled (shutdown enabled)

bit 3: **VPPCOMP**
- 1 = VPP under-voltage comparator is disabled
- 0 = VPP under-voltage comparator is active

bit 2: **VOSET**
- 1 = VPP is set to 90 V
- 0 = VPP is set to 80 V

bit 1: **CPEN**
- 1 = Charge Pump is enabled
- 0 = Charge Pump is disabled

bit 0: **OCSET**
- 1 = Output current is set to 60 µA
- 0 = Output current is set to 30 µA

Notes:

3. VPP and VDD faults are latched. Once this bit is set high, it must be written to 0 to clear the fault.
4. The SLEEP bit is forced low in GPIO mode.

Daisy Chain Operation

Daisy chaining the ICs is permitted and involves connecting the MISO of one chip to the MOSI of the next chip in the chain, as shown in Figure 10. SPI timing diagrams with daisy-chained devices are provided in Figure 11 and Figure 12.

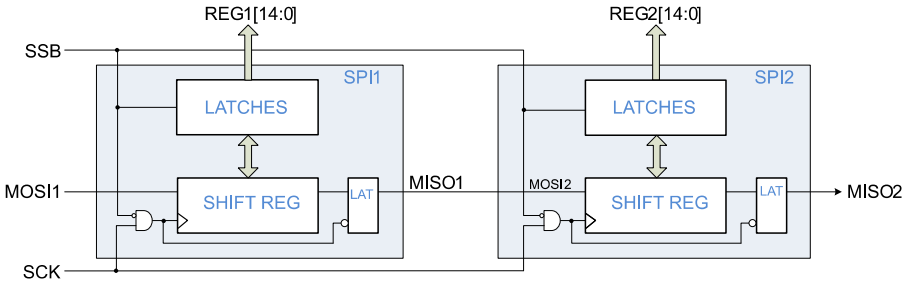


Figure 10. SPI with 2 ICs Daisy-chained

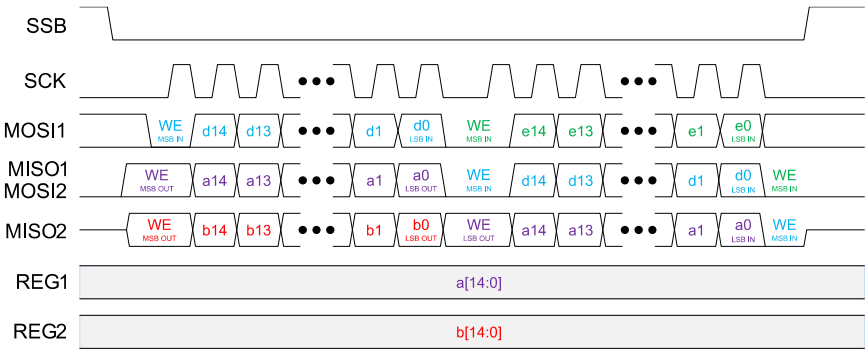


Figure 11. SPI Read Only (2 ICs Daisy-chained)

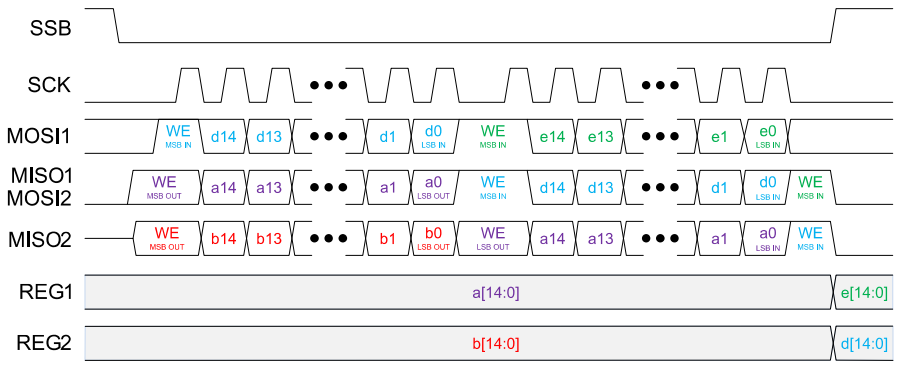


Figure 12. SPI Read and Write (2 ICs Daisy-chained)

Table 8. Switch State Table in GPIO Mode

Count	Input Signals					HV							
	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	7	6	5	4	3	2	1	0
0	1	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
1	1	0	0	0	1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**
2	1	0	0	1	0	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF
3	1	0	0	1	1	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	OFF
4	1	0	1	0	0	OFF	OFF	OFF	OFF	**ON**	OFF	OFF	OFF
5	1	0	1	0	1	OFF	OFF	OFF	**ON**	OFF	OFF	OFF	OFF
6	1	0	1	1	0	OFF	OFF	**ON**	OFF	OFF	OFF	OFF	OFF
7	1	0	1	1	1	OFF	**ON**	OFF	OFF	OFF	OFF	OFF	OFF
8	1	1	0	0	0	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF
9	1	1	0	0	1	**ON**	OFF	**ON**	OFF	**ON**	OFF	OFF	**ON**
10	1	1	0	1	0	**ON**	OFF	**ON**	OFF	OFF	**ON**	**ON**	OFF
11	1	1	0	1	1	**ON**	OFF	OFF	**ON**	**ON**	OFF	**ON**	OFF
12	1	1	1	0	0	OFF	**ON**	**ON**	OFF	**ON**	OFF	**ON**	OFF
13	1	1	1	0	1	**ON**	OFF	**ON**	OFF	**ON**	OFF	**ON**	OFF
14	1	1	1	1	0	OFF	**ON**	OFF	**ON**	OFF	**ON**	OFF	**ON**
15	1	1	1	1	1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
16	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
17	0	0	0	0	1	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	**ON**
18	0	0	0	1	0	OFF	**ON**	OFF	OFF	OFF	OFF	**ON**	OFF
19	0	0	0	1	1	**ON**	**ON**	OFF	OFF	OFF	OFF	**ON**	**ON**
20	0	0	1	0	0	OFF	OFF	**ON**	OFF	OFF	**ON**	OFF	OFF
21	0	0	1	0	1	**ON**	OFF	**ON**	OFF	OFF	**ON**	OFF	**ON**

Count	Input Signals					HV							
	FLIP_BIT	CTL4	CTL3	CTL2	CTL1	7	6	5	4	3	2	1	0
22	0	0	1	1	0	OFF	**ON**	**ON**	OFF	OFF	**ON**	**ON**	OFF
23	0	0	1	1	1	**ON**	**ON**	**ON**	OFF	OFF	**ON**	**ON**	**ON**
24	0	1	0	0	0	OFF	OFF	OFF	**ON**	**ON**	OFF	OFF	OFF
25	0	1	0	0	1	**ON**	OFF	OFF	**ON**	**ON**	OFF	OFF	**ON**
26	0	1	0	1	0	OFF	**ON**	OFF	**ON**	**ON**	OFF	**ON**	OFF
27	0	1	0	1	1	**ON**	**ON**	OFF	**ON**	**ON**	OFF	**ON**	**ON**
28	0	1	1	0	0	OFF	OFF	**ON**	**ON**	**ON**	**ON**	OFF	OFF
29	0	1	1	0	1	**ON**	OFF	**ON**	**ON**	**ON**	**ON**	OFF	**ON**
30	0	1	1	1	0	OFF	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**	OFF
31	0	1	1	1	1	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**

Fault Conditions

There are two comparators that can signal a fault condition:

- VDD under voltage fault
- VPP under voltage fault

Note: The VPP under voltage comparator can be disabled. In SPI mode, it is disabled when the VPPCOMP bit in the CONTROL register is high. In GPIO mode, the comparator is disabled when CP_EN pin is set low.

Faults are reported differently depending on the mode of communication - SPI or GPIO. The outputs of the VDD and VPP fault comparators are logically OR'ed. The output of the OR gate controls the FLTB pin. FLTB is an open-drain output and is ON (low impedance) if either fault is detected. In SPI mode, bit 6 of the CONTROL register provides VDD and VPP fault status.

At start-up, the FLTB pin is held OFF (high impedance). It is allowed to change state only after each voltage goes past its Enable threshold (VDD goes higher than UVLORISE and VPP goes higher than VEN). This prevents a race condition at startup.

Once VDD and VPP go above their thresholds, the comparators monitoring VDD and VPP actively monitor for faults. If VDD goes below UVLOFALL or VPP goes below VPPDIS, a fault condition is signaled by setting the FLTB pin low and the Fault Status bit high (bit 6 in the CONTROL register). The FLTB pin returns to an open state when the fault condition is cleared – the FSTAT bit remains latched high until it is cleared via a SPI write.

If Fault Mode is enabled (in GPIO mode, FLT_MODE pin = 0, in SPI mode, FLT_MODE bit = 0), the outputs are all set low and the charge pump is turned off. The user must toggle the CP_EN pin (GPIO mode) or the CPEN register bit (SPI mode) low and then high to re-start the device.

If Fault Mode is disabled (in GPIO mode, FLT_MODE pin = 1; in SPI mode, FLT_MODE bit = 1), no action is taken by the IC. The fault condition is reported, but does not affect the charge pump operation or switch states

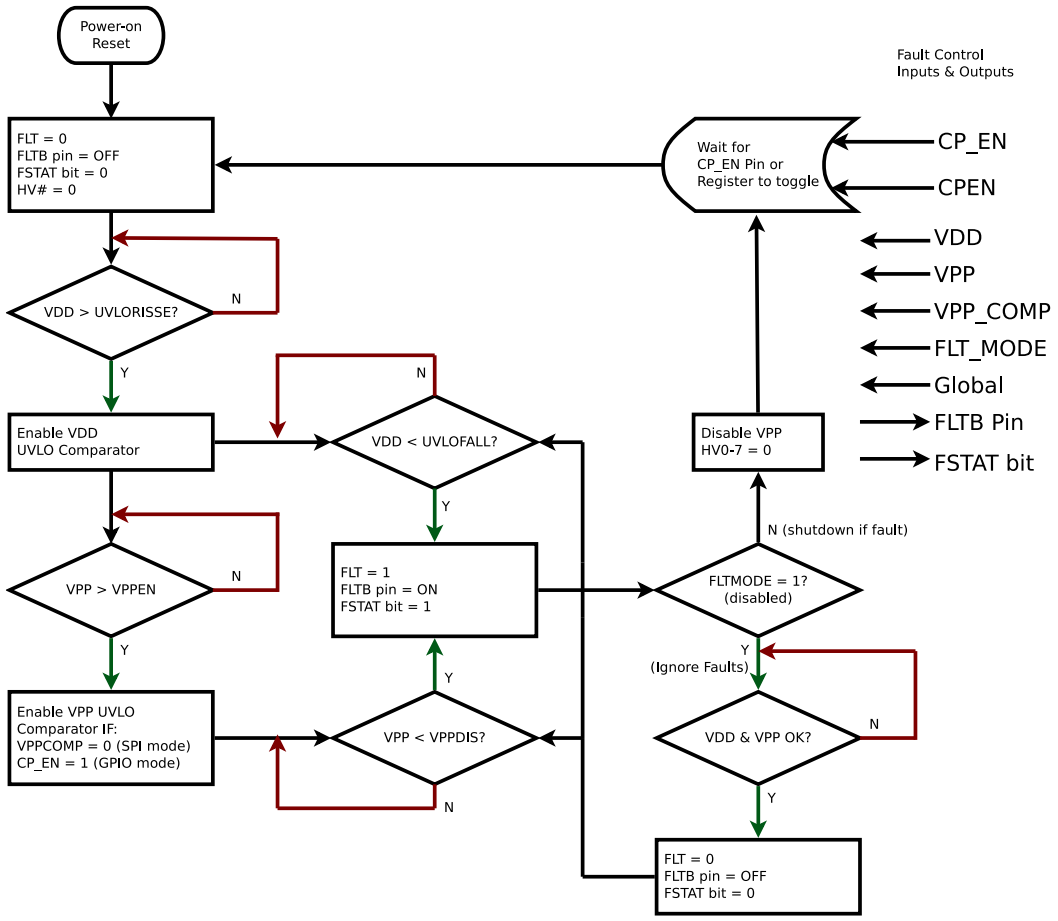


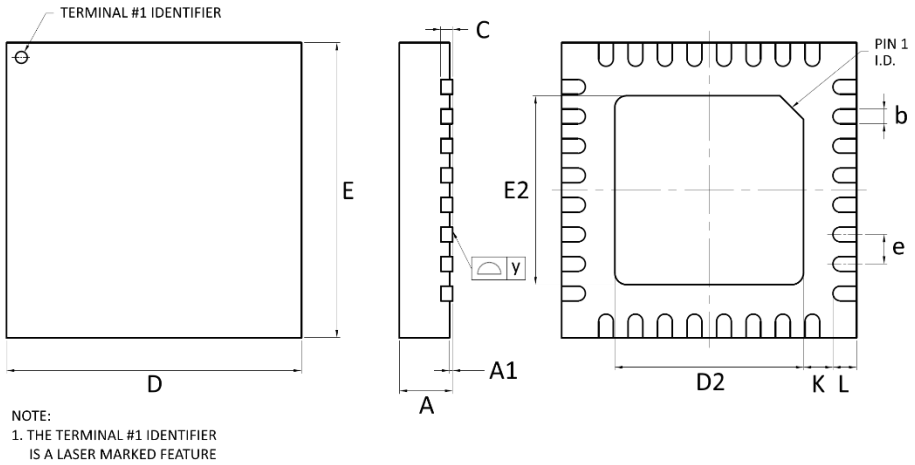
Figure 13. Flowchart for Fault

Notes:

1. The un-faulted supply continues to be monitored when a fault occurs. The FLT signal remains faulted until both supplies are above their brownout trip level.
2. VDD_IO is not monitored unless it is connected to VDD.
3. VPP is not monitored if: VPPCOMP = 1 in SPI mode OR the CP_EN pin is low In GPIO mode.

QFN Package Drawing

The 5 mm x 5 mm 32P QFN package drawing is below.



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	---	0.20 REF.	---
D	4.90	5.00	5.10
D2	3.15	3.20	3.25
E	4.90	5.00	5.10
E2	3.15	3.20	3.25
e	---	0.50	---
K	---	0.50	---
L	0.35	0.40	0.45
y	0.00	---	0.075

Figure 14. QFN Package Drawing

Footprint Details

Dimensions are given in millimeters.

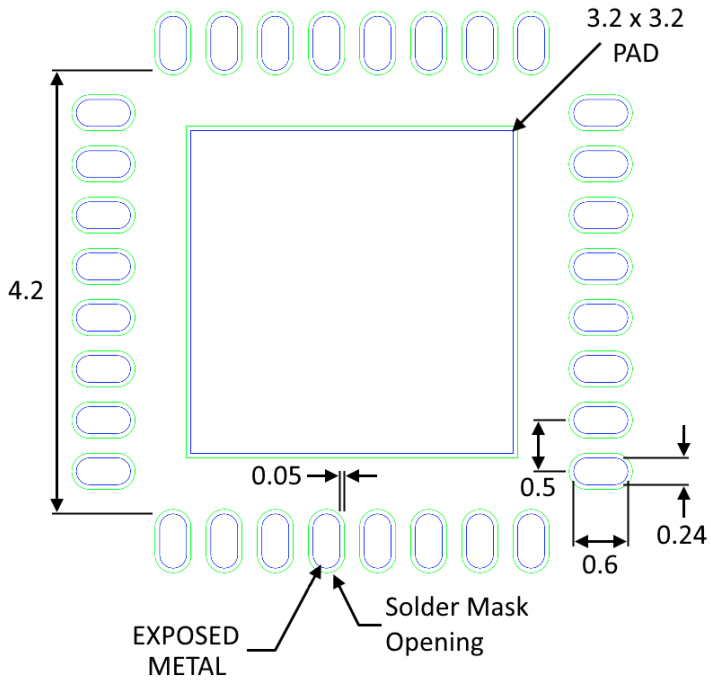
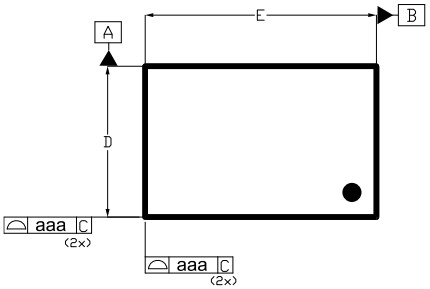


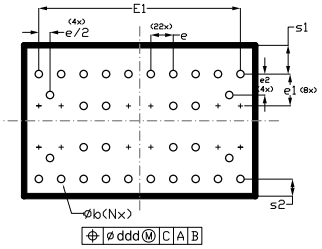
Figure 15. QFN Footprint Drawing

Flip Chip Package Drawing

The 2.37 mm x 1.58 mm WLCSP Flip Chip package drawing is below. Note dimension references **s1** and **s2**, as grid array is not symmetrical with part outline in y direction (along dimension **D**).

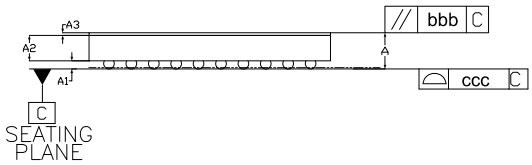


TOP VIEW



BOTTOM VIEW
(BUMP SIDE)

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.321	0.355	0.389
A1	0.074	0.080	0.086
A2	0.225	0.250	0.275
A3	0.022	0.025	0.028
D		1.580 BSC	
E		2.370 BSC	
E1		1.980 BSC	
s1		0.282 BSC	
s2		0.168 BSC	
e		0.220 BSC	
e1		0.312 BSC	
e2		0.206 BSC	
b	0.095	0.105	0.110
N		32	
	DIMENSIONAL TOLERANCES		
aaa		0.080	
bbb		0.060	
ccc		0.050	
ddd		0.015	



SIDE VIEW

1. DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994 & JEDEC PUB 95 DESIGN GUIDE 4.18
2. THE TOLERANCE 'aaa' IN THE TABLE ABOVE DOES NOT CONFORM TO JEDEC PUB 95 DESIGN GUIDE 4.18
3. DIMENSION A3 IS THE THICKNESS OF THE LASER MARK TAPE
4. N = TERMINAL COUNT / TERMINAL FINISH : SAC 305
5. CROSS HAIRS (+) INDICATE GRID DEPOPULATION

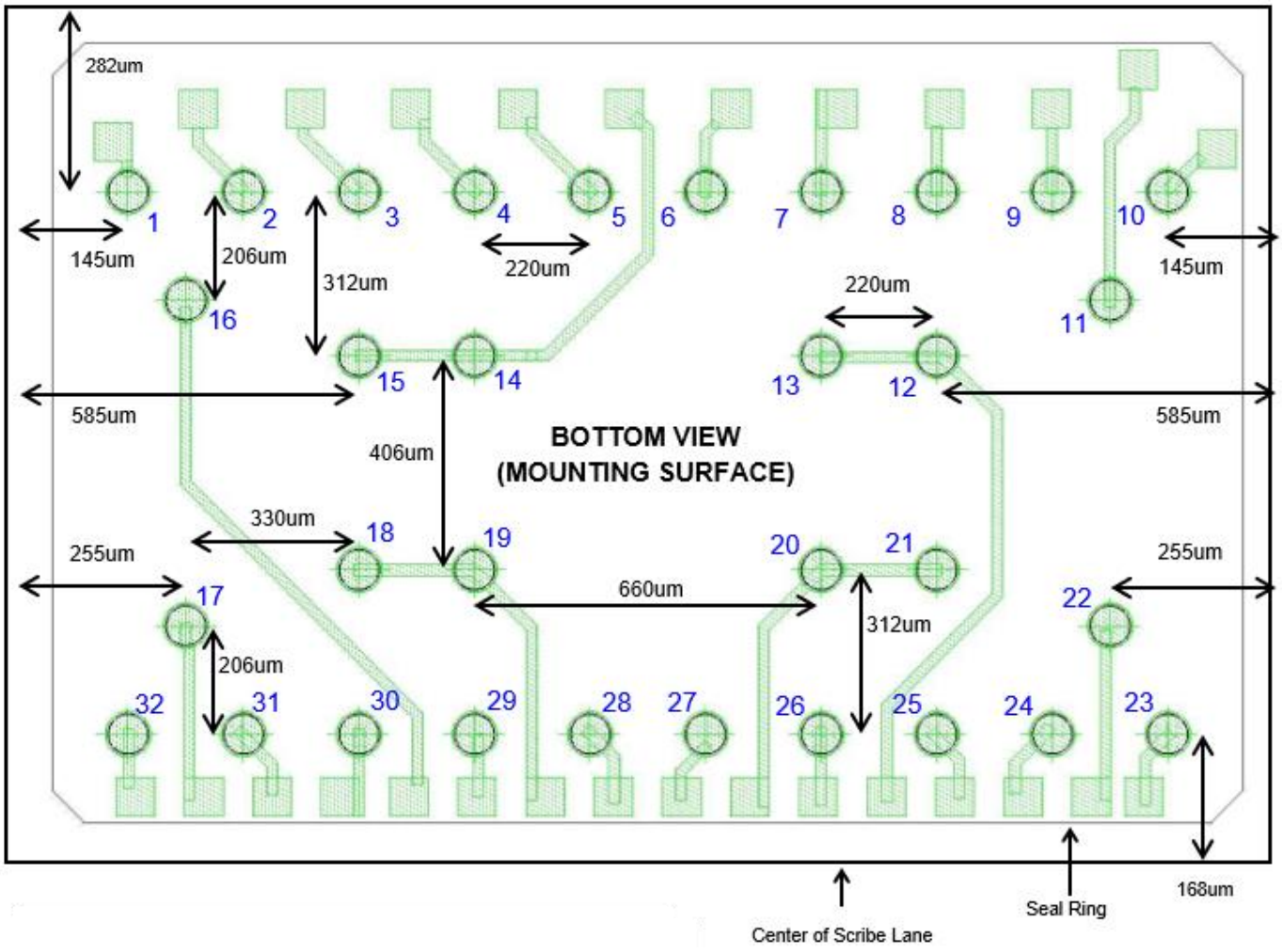


Table 9. Flip-chip SOLDER BALL Locations

Ball #	Signal Name	X (um)	Y (um)	Ball #	Signal Name	X (um)	Y (um)	Ball #	Signal Name	X (um)	Y (um)
1	VDD	-990	458	12	FLIP_BIT	550	146	23	NC	990	-572
2	HV0	-770	458	13	FLIP_BIT	330	146	24	AGND	770	-572
3	HV1	-550	458	14	VPP	-330	146	25	FLTB	550	-572
4	HV2	-330	458	15	VPP	-550	146	26	NC	330	-572
5	HV3	-110	458	16	MISO / CTL3	-880	252	27	VDD_IO	110	-572
6	HV4	110	458	17	CP_EN	-880	-366	28	MODE	-110	-572
7	HV5	330	458	18	DGND	-550	-260	29	SSB / CTL4	-330	-572
8	HV6	550	458	19	DGND	-330	-260	30	MOSI / CTL2	-550	-572
9	HV7	770	458	20	VDD	330	-260	31	SCK / CTL1	-770	-572
10	VIN	990	458	21	VDD	550	-260	32	NC	-990	-572
11	CPGND	880	252	22	FLT_MODE	880	-366	—	—	—	—

X-Y position = Ball center with respect to Die Center
Bump Diameter = 100um to 105um
Bump Height = 80um

Recommended PCB Layout and External Circuitry

For MM101-02ADA, non-solder mask defined pads are recommended. See Figure 15 on page 27.

Figure 16 below shows an example layout for the MM101 with supporting components for the following configuration: 3.3 V logic levels, GPIO mode, 90 V driver voltage, 60 µA driver current. For other configurations, reference Typical Applications and Table 7 for instructions on which pins to disconnect from VDD_IO. For SPI mode, disconnect MODE from VDD_IO and connect to GND.

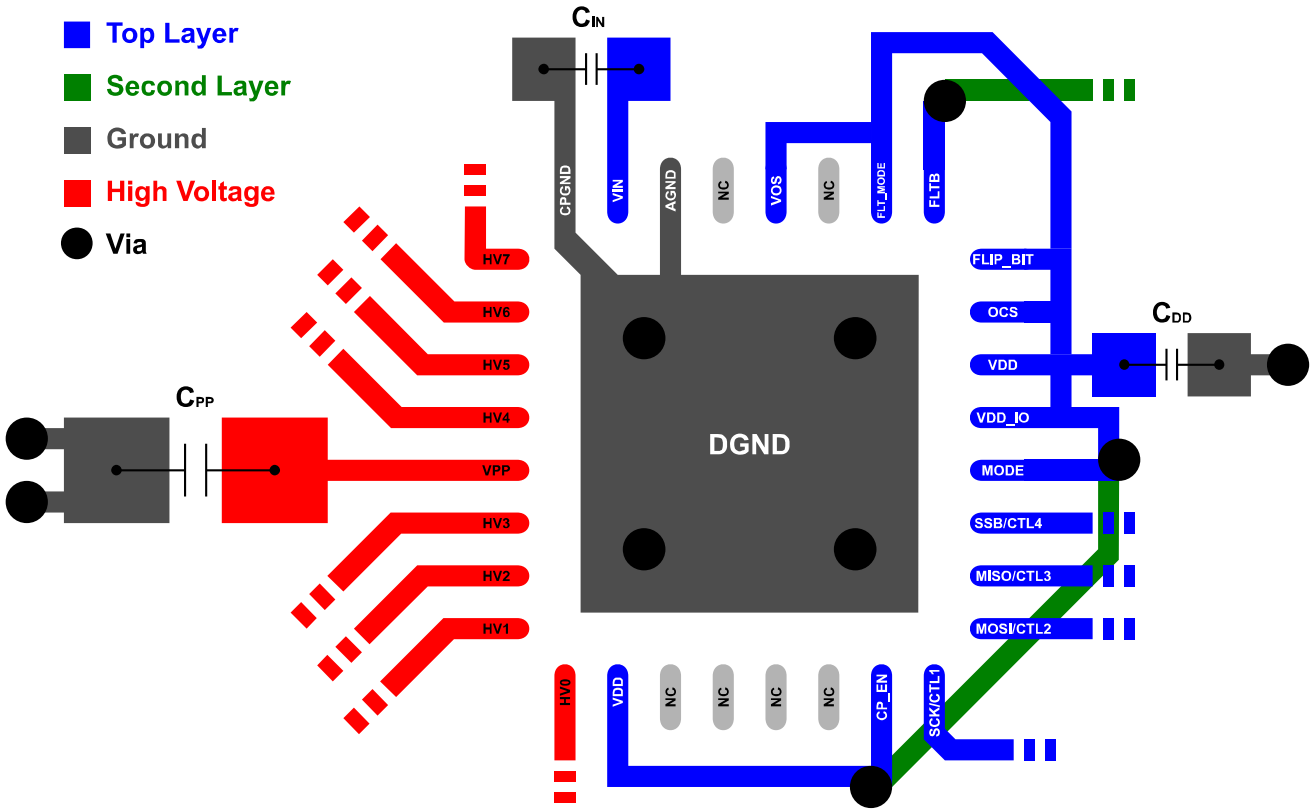


Figure 16. Example PCB Layout

Symbol	Manufacturer	Part Number
C_{IN}, C_{DD}	Samsung	CL10A105KA8NNNC
C_{PP}	KEMET	C0603Y472K2RAC7867
R_{FLT} (Not Shown)	Yageo	RC0402FR-0749K9P

Recommended Solder Reflow Profile

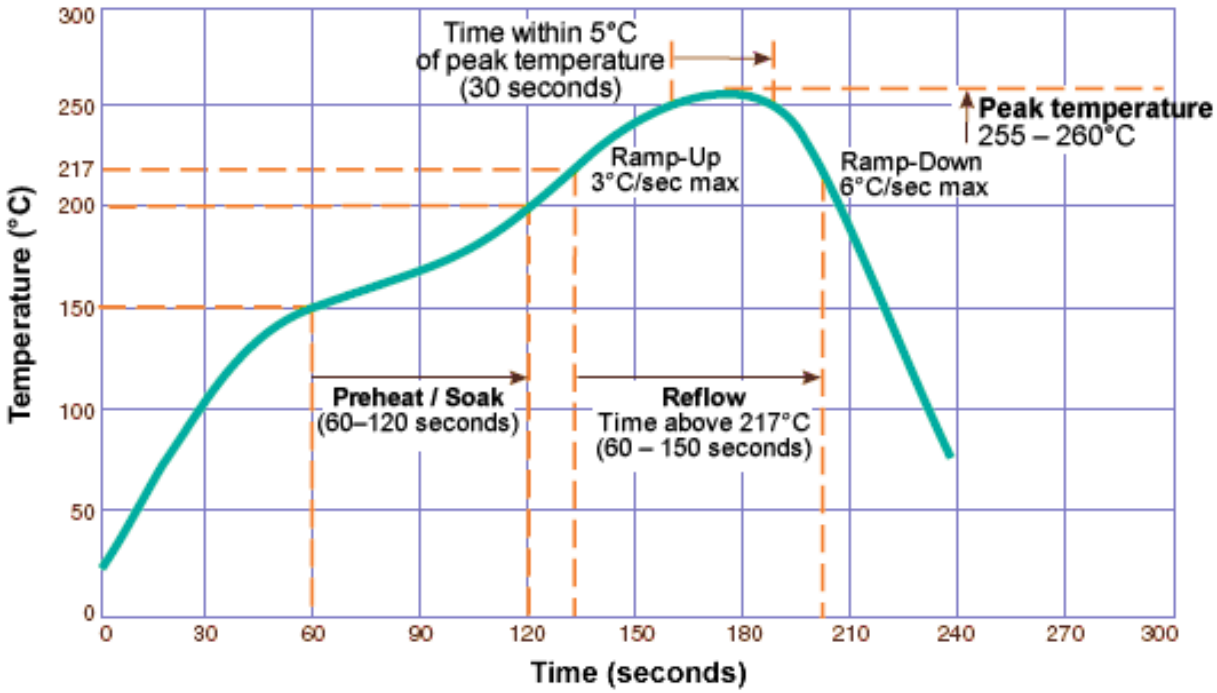


Figure 17. Reflow Profile

Reflow profiles and assembly guidelines are given for RoHS-compliant (lead-free) solder alloy.

Follow Moisture Sensitivity Level (MSL) 3 handling precautions specified in IPC/JEDEC J-STD-020.

Storage and Shelf Life

Under typical industry storage conditions (≤30 °C/60% RH) in Moisture Barrier Bags:

- Customer Shelf Life: 24 months from customer receipt date
- Extended Shelf Life: 60 months from customer receipt date if re-bagged every 24 months or less.

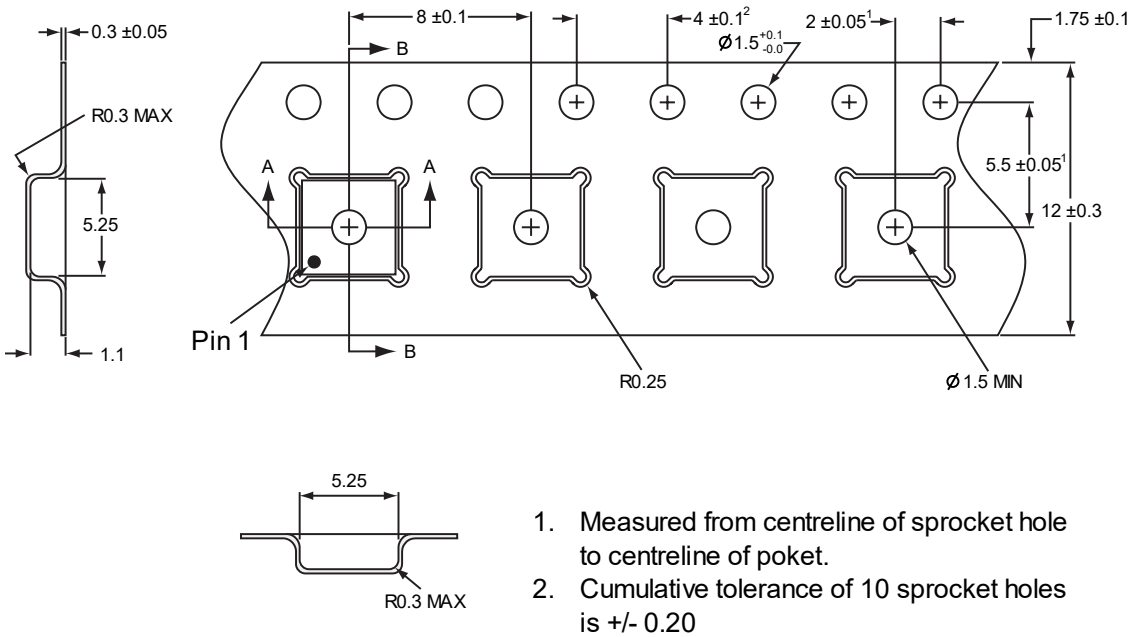
Package Marking Information

The MM101-02ADA package marking and nomenclature are illustrated in Figure 18.

Dot ● = Pin 1 Indicator
Line 1 = Part Number
Line 2 = Internal part number
Line 3 = Date Code (year/work week)

Figure 18. Package Marking Drawing

Package Materials Information



1. Measured from centreline of sprocket hole to centreline of poket.
2. Cumulative tolerance of 10 sprocket holes is +/- 0.20

Dimensions are in millimeters.

Figure 19. Tape and Reel Drawing

Package Options and Ordering Information

All Menlo Micro solutions are EAR99 compliant.

Part Number	Package Description	Temp Range	Device Marking[1]
MM101-02ADA	8ch charge pump driver IC - QFN	-40°C to +125°C	MM101-02B
MM101-02ADA-TR	8ch charge pump driver IC – QFN, Tape and Reel (Qty 250)	-40°C to +125°C	MM101-02B
MM101-03ADA	8ch charge pump driver IC - WLCSP	-40°C to +125°C	
MM101-03ADA-TR	8ch charge pump driver IC – WLCSP, Tape and Reel (Qty 250)	-40°C to +125°C	
MM101EVK1	Evaluation board for MM101 8ch charge pump driver IC - QFN		

Notes:

1. Additional markings may be present, including logo or lot trace code information. This information may be a 2D barcode or other human-readable markings. Note that ‘x’ is a placeholder for a 5-digit numerical code.

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