

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$ Max	I_D Max (A) $T_A = +25^\circ\text{C}$ (Notes 6 & 8)
Q1	40V	25mΩ @ $V_{GS} = 10\text{V}$	7.5
		40mΩ @ $V_{GS} = 4.5\text{V}$	6.2
Q2	-40V	25mΩ @ $V_{GS} = -10\text{V}$	-7.3
		45mΩ @ $V_{GS} = -4.5\text{V}$	-5.7

Description

This MOSFET is designed to ensure that $R_{DS(ON)}$ of N and P channel FET are matched to minimize losses in both arms of the bridge. The DMC4040SSD is optimized for use in a 3-phase brushless DC motor circuit (BLDC), and CCFL backlighting.

Applications

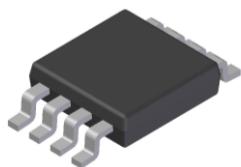
- 3-Phase BLDC Motor
- CCFL Backlighting

Features and Benefits

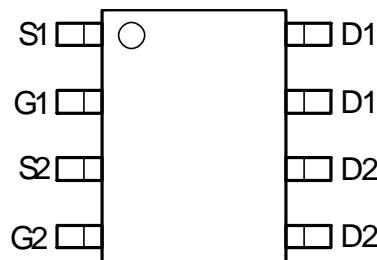
- Matched N & P $R_{DS(ON)}$ – Minimizes Power Losses
- Fast Switching – Minimizes Switching Losses
- Dual Device – Reduces PCB Area
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

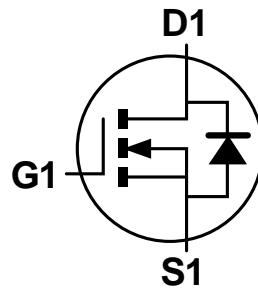
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.074 grams (Approximate)



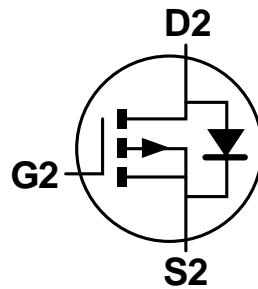
Top View



Top View



Q1 N-Channel



Q2 P-Channel

Equivalent Circuit

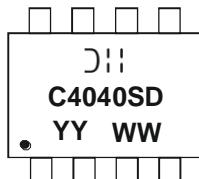
Ordering Information (Note 4)

Product	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DMC4040SSD-13	C4040SD	13	12	2,500

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



DII = Manufacturer's Marking
 C4040SD = Product Type Marking Code
 YYWW = Date Code Marking
 YY or YY = Year (ex: 10 = 2010)
 WW = Week (01 - 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Drain-Source Voltage		V_{DSS}	40	-40	V
Gate-Source Voltage		V_{GSS}	± 20	± 20	
Continuous Drain Current	$V_{GS} = 10\text{V}$	(Notes 6 & 8)	I_D	7.5	-7.5
		$T_A = +70^\circ\text{C}$ (Notes 6 & 8)		5.8	-5.8
		(Notes 5 & 8)		5.7	-5.7
		(Notes 5 & 9)		6.8	-6.8
Pulsed Drain Current	$V_{GS} = 10\text{V}$	(Notes 7 & 8)	I_{DM}	29.0	-29.0
Continuous Source Current (Body Diode)		(Notes 6 & 8)	I_S	3.0	-3.0
Pulsed Source Current (Body Diode)		(Notes 7 & 8)	I_{SM}	29.0	-29.0

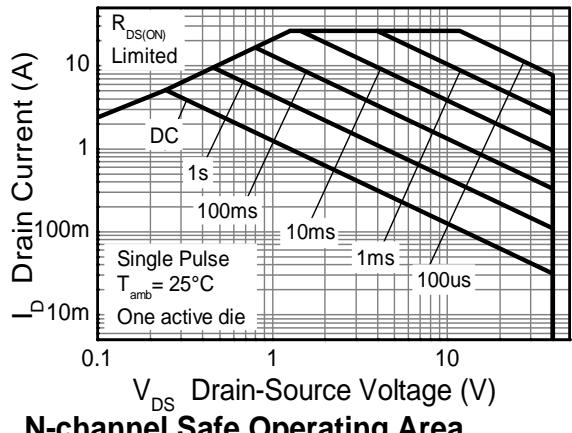
Thermal Characteristics

Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 5 & 8)	P_D	1.25		W mW/°C
			10		
	(Notes 5 & 9)		1.8		
			14.3		
	(Notes 6 & 8)		2.14		
Thermal Resistance, Junction to Ambient	(Notes 5 & 8)	$R_{\theta JA}$	100		°C/W
	(Notes 5 & 9)		70		
	(Notes 6 & 8)		58		
Thermal Resistance, Junction to Lead	(Notes 5 & 10)	$R_{\theta JL}$	51		
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150		°C

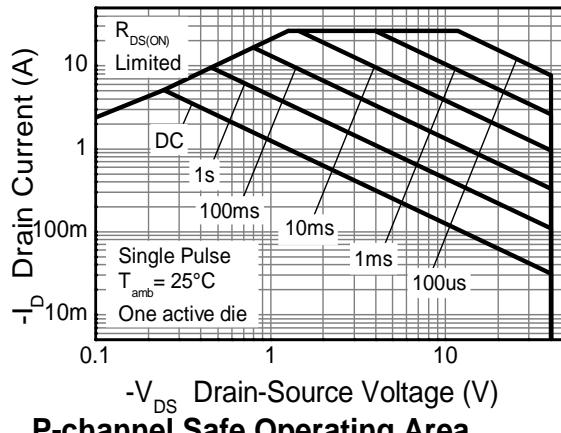
Notes:

5. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
6. Same as note (5), except the device is measured at $t \leq 10$ sec.
7. Same as note (5), except the device is pulsed with $D = 0.02$ and pulse width 300 μs .
8. For a dual device with one active die.
9. For a device with two active die running at equal power.
10. Thermal resistance from junction to solder-point (at the end of the drain lead).

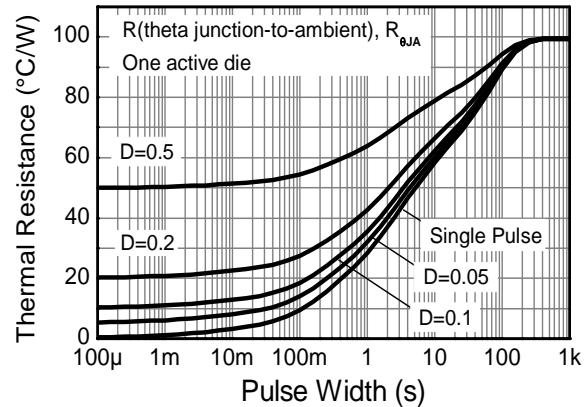
Thermal Characteristics (Continued)



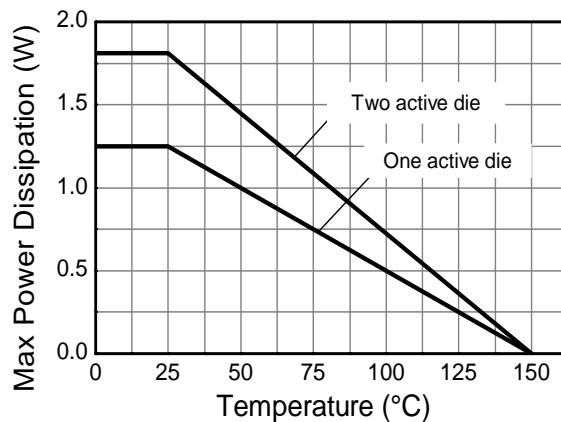
N-channel Safe Operating Area



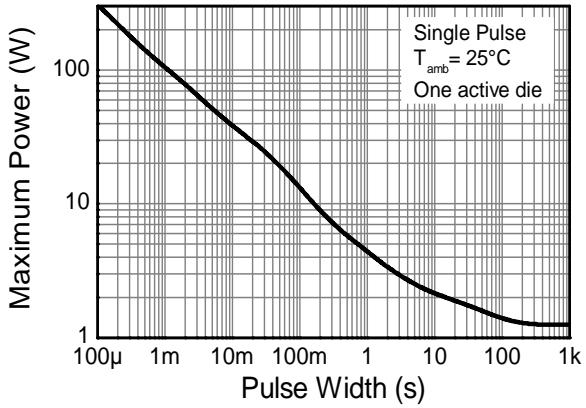
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

Electrical Characteristics (Q1 N-Channel) (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	$I_D = 250\mu\text{A}, V_{\text{GS}} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	$V_{\text{DS}} = 40\text{V}, V_{\text{GS}} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{\text{GS}} = \pm 20\text{V}, V_{\text{DS}} = 0\text{V}$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	0.8	1.3	1.8	V	$I_D = 250\mu\text{A}, V_{\text{DS}} = V_{\text{GS}}$
Static Drain-Source On-Resistance (Note 11)	$R_{\text{DS}(\text{ON})}$	—	0.013	0.025	Ω	$V_{\text{GS}} = 10\text{V}, I_D = 3\text{A}$
			0.028	0.040		$V_{\text{GS}} = 4.5\text{V}, I_D = 3\text{A}$
Forward Transconductance (Notes 11 & 12)	G_{fs}	—	12.6	—	S	$V_{\text{DS}} = 5\text{V}, I_D = 3\text{A}$
Diode Forward Voltage (Note 11)	V_{SD}	—	0.7	1.0	V	$I_S = 1\text{A}, V_{\text{GS}} = 0\text{V}$
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	—	1,790	—	pF	$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	160	—		
Reverse Transfer Capacitance	C_{rss}	—	120	—		
Gate Resistance	R_g	—	1.03	—	Ω	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge (Note 13)	Q_g	—	16.0	—	nC	$V_{\text{GS}} = 4.5\text{V}$
Total Gate Charge (Note 13)	Q_g	—	37.6	—		$V_{\text{DS}} = 20\text{V}$
Gate-Source Charge (Note 13)	Q_{gs}	—	7.8	—		$V_{\text{GS}} = 10\text{V}$
Gate-Drain Charge (Note 13)	Q_{gd}	—	6.6	—		$I_D = 3\text{A}$
Turn-On Delay Time (Note 13)	$t_{\text{D}(\text{on})}$	—	8.1	—	nS	$V_{\text{DD}} = 20\text{V}, V_{\text{GS}} = 10\text{V}$ $I_D = 3\text{A}$
Turn-On Rise Time (Note 13)	t_r	—	15.1	—		
Turn-Off Delay Time (Note 13)	$t_{\text{D}(\text{off})}$	—	24.3	—		
Turn-Off Fall Time (Note 13)	t_f	—	5.3	—		

Electrical Characteristics (Q2 P-Channel) (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

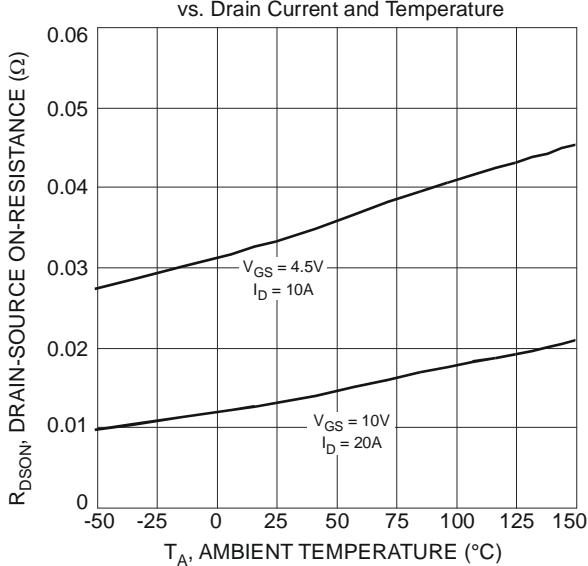
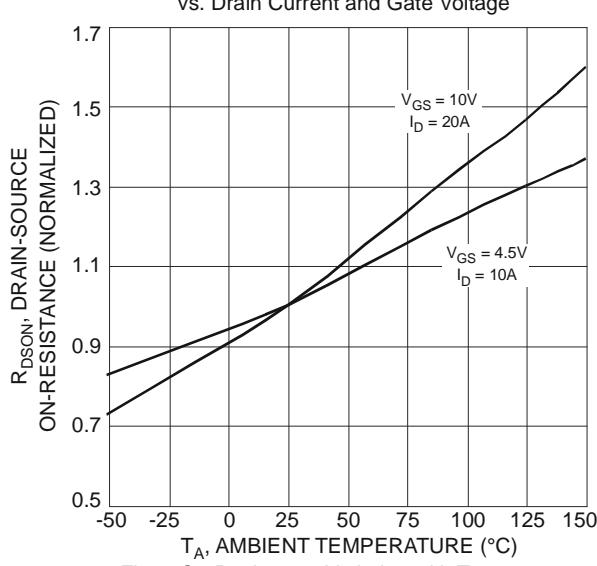
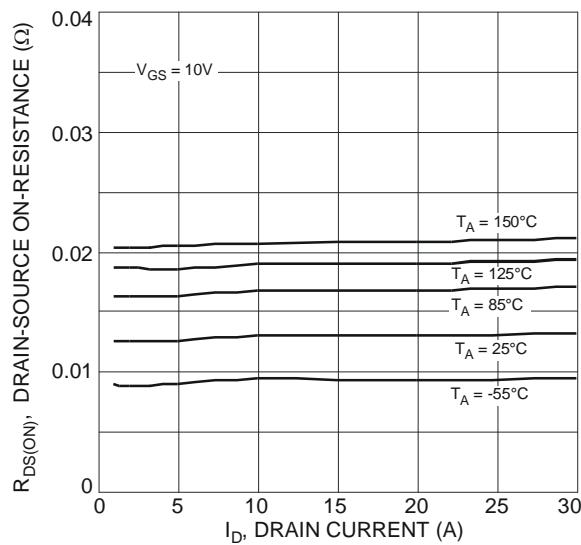
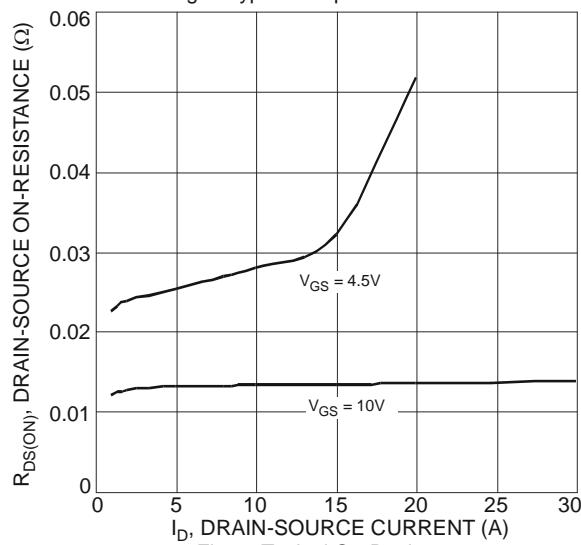
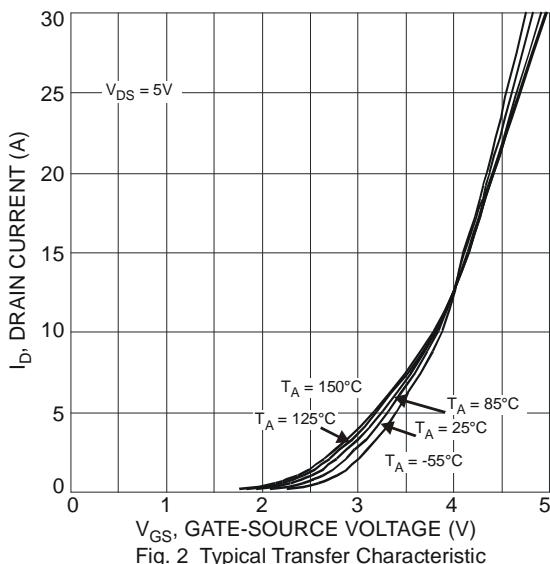
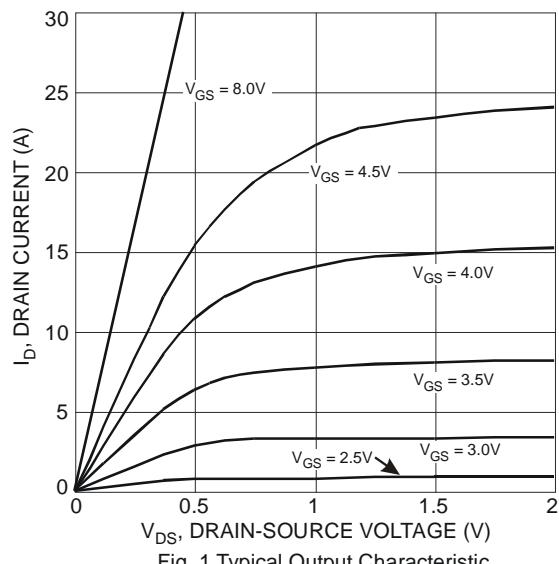
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	$I_D = -250\mu\text{A}, V_{\text{GS}} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	μA	$V_{\text{DS}} = -40\text{V}, V_{\text{GS}} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{\text{GS}} = \pm 20\text{V}, V_{\text{DS}} = 0\text{V}$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	-0.8	-1.3	-1.8	V	$I_D = -250\mu\text{A}, V_{\text{DS}} = V_{\text{GS}}$
Static Drain-Source On-Resistance (Note 11)	$R_{\text{DS}(\text{ON})}$	—	0.018	0.025	Ω	$V_{\text{GS}} = -10\text{V}, I_D = -3\text{A}$
			0.030	0.045		$V_{\text{GS}} = -4.5\text{V}, I_D = -3\text{A}$
Forward Transconductance (Notes 11 & 12)	G_{fs}	—	16.6	—	S	$V_{\text{DS}} = -5\text{V}, I_D = -3\text{A}$
Diode Forward Voltage (Note 11)	V_{SD}	—	-0.7	-1.0	V	$I_S = -1\text{A}, V_{\text{GS}} = 0\text{V}$
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	—	1,643	—	pF	$V_{\text{DS}} = -20\text{V}, V_{\text{GS}} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	179	—		
Reverse Transfer Capacitance	C_{rss}	—	128	—		
Gate Resistance	R_g	—	6.43	—	Ω	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge (Note 13)	Q_g	—	14.0	—	nC	$V_{\text{GS}} = -4.5\text{V}$
Total Gate Charge (Note 13)	Q_g	—	33.7	—		$V_{\text{DS}} = -20\text{V}$
Gate-Source Charge (Note 13)	Q_{gs}	—	5.5	—		$V_{\text{GS}} = -10\text{V}$
Gate-Drain Charge (Note 13)	Q_{gd}	—	7.3	—		$I_D = -3\text{A}$
Turn-On Delay Time (Note 13)	$t_{\text{D}(\text{on})}$	—	6.9	—	nS	$V_{\text{DD}} = -20\text{V}, V_{\text{GS}} = -10\text{V}$ $I_D = -3\text{A}$
Turn-On Rise Time (Note 13)	t_r	—	14.7	—		
Turn-Off Delay Time (Note 13)	$t_{\text{D}(\text{off})}$	—	53.7	—		
Turn-Off Fall Time (Note 13)	t_f	—	30.9	—		

Notes: 11. Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$

12. For design aid only, not subject to production testing.

13. Switching characteristics are independent of operating junction temperatures.

Typical Characteristics (Q1 N-Channel)



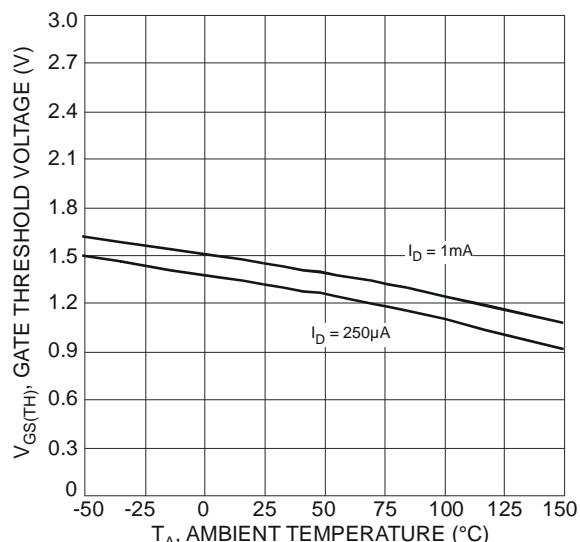


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

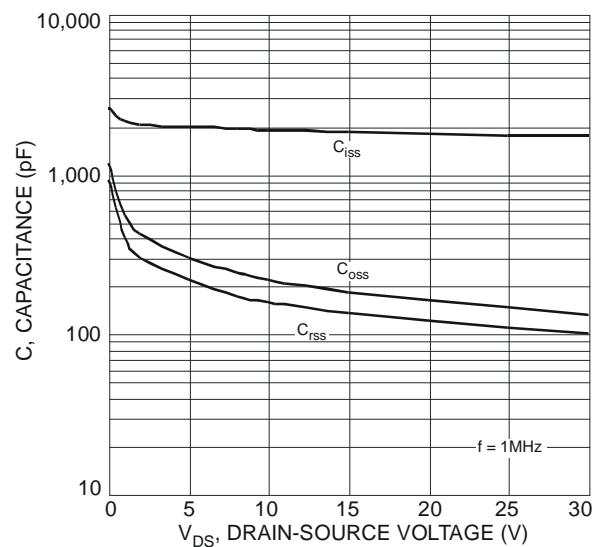


Fig. 9 Typical Total Capacitance

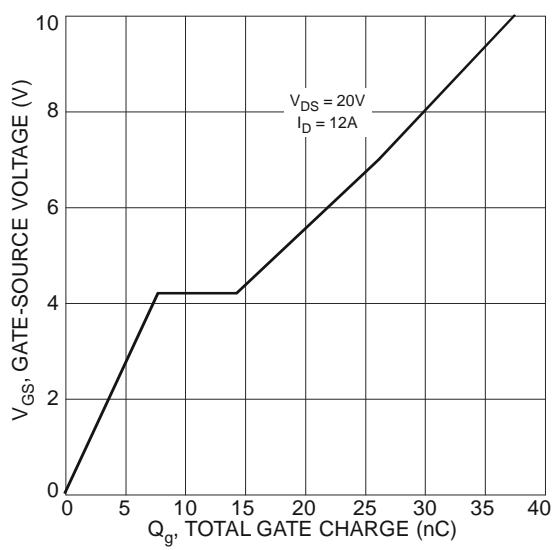


Fig. 11 Gate-Charge Characteristics

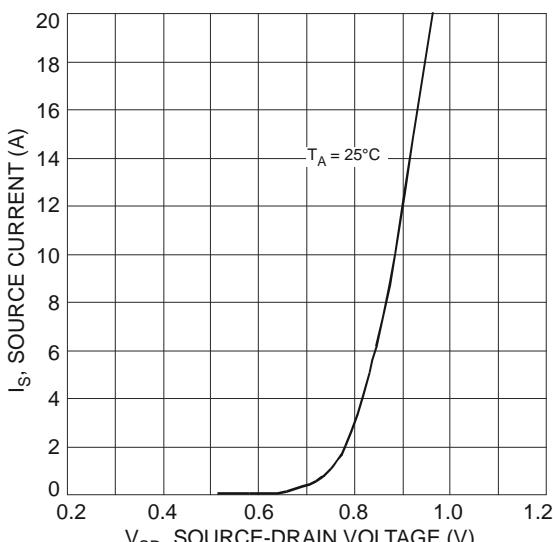


Fig. 8 Diode Forward Voltage vs. Current

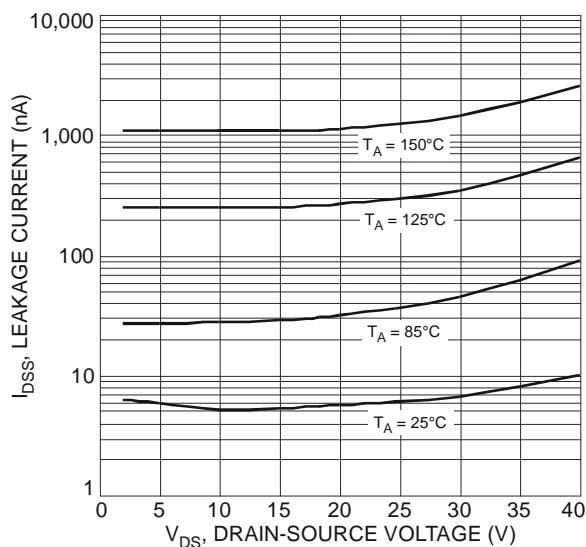


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

Typical Characteristics (Q2 P-Channel)

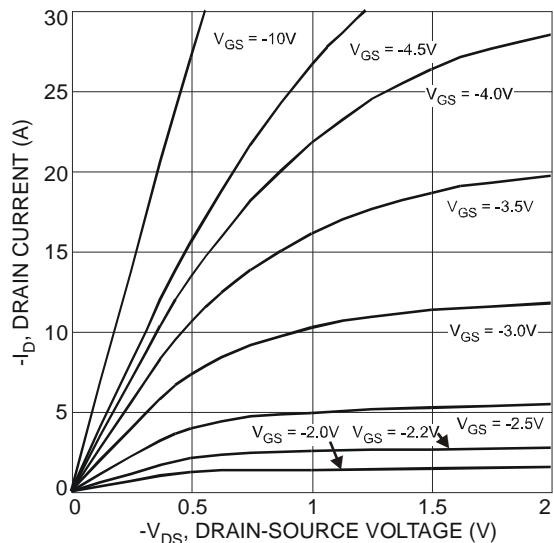


Fig. 12 Typical Output Characteristic

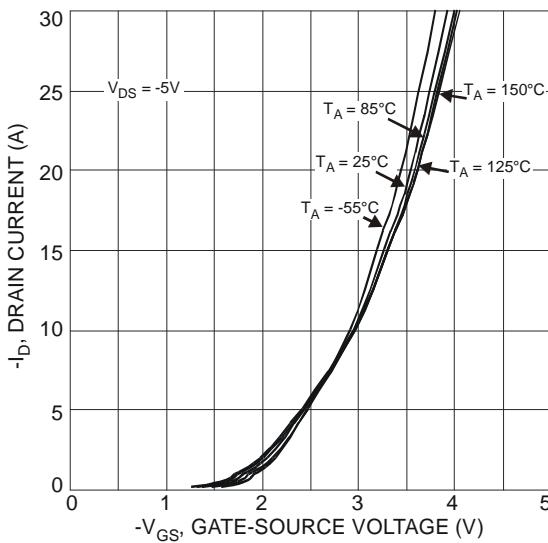


Fig. 13 Typical Transfer Characteristic

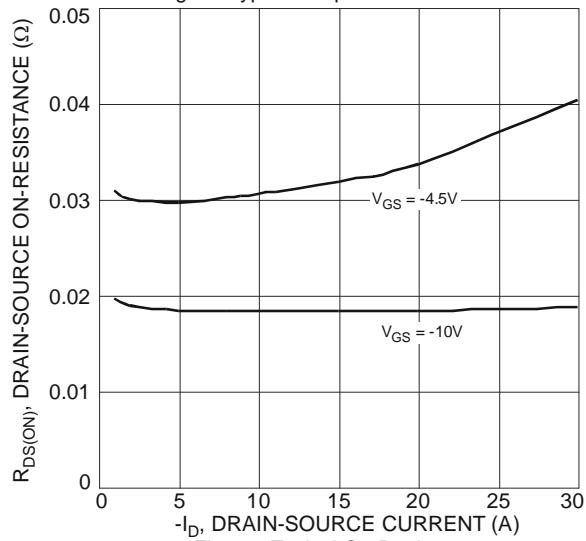


Fig. 14 Typical On-Resistance vs. Drain Current and Gate Voltage

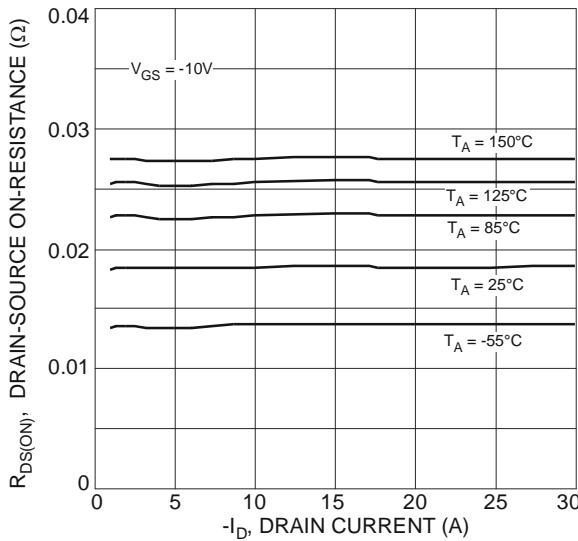


Fig. 15 Typical On-Resistance vs. Drain Current and Temperature

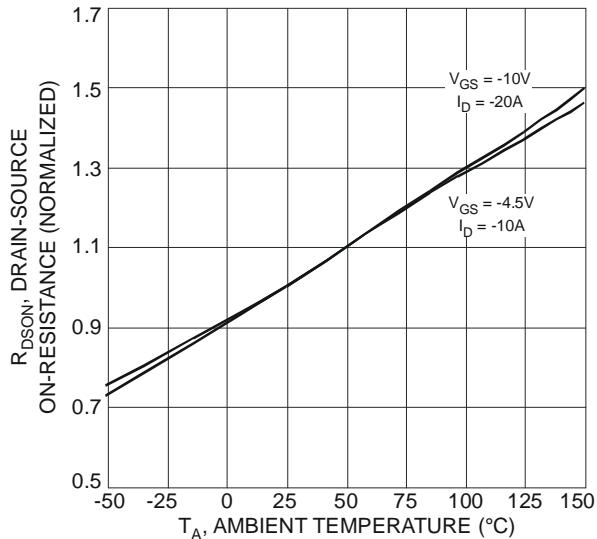


Fig. 16 On-Resistance Variation with Temperature

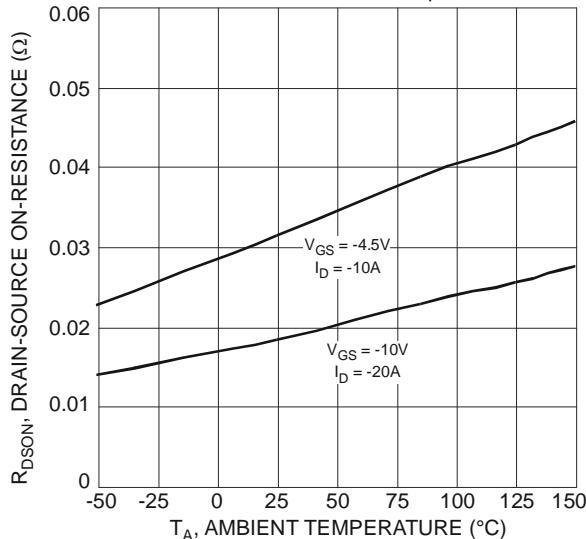


Fig. 17 On-Resistance Variation with Temperature

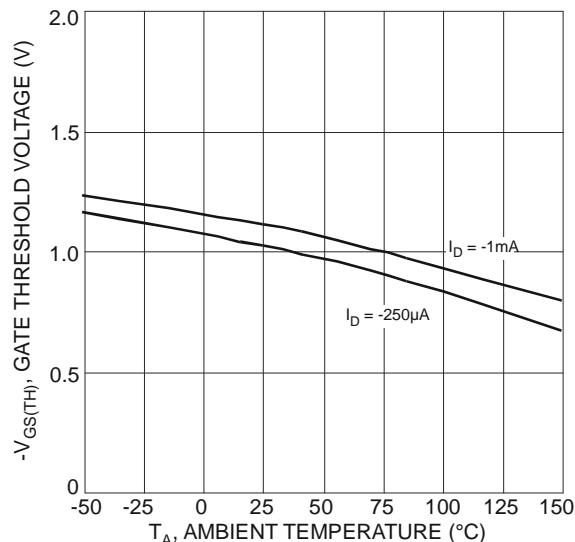


Fig. 18 Gate Threshold Variation vs. Ambient Temperature

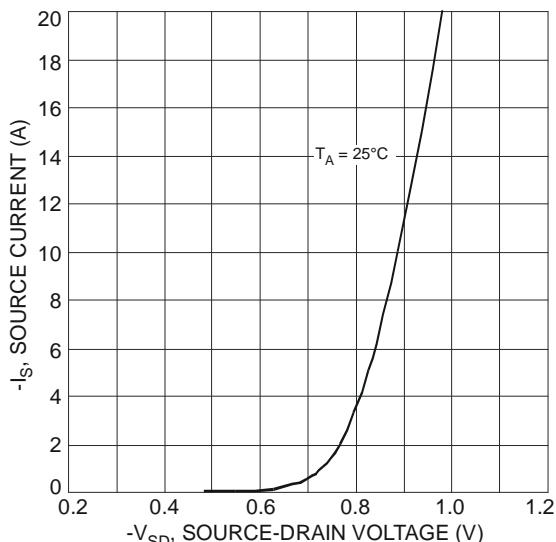


Fig. 19 Diode Forward Voltage vs. Current

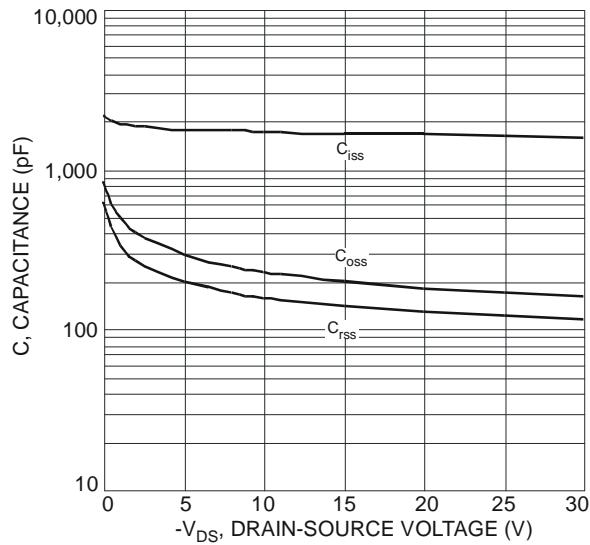


Fig. 20 Typical Total Capacitance

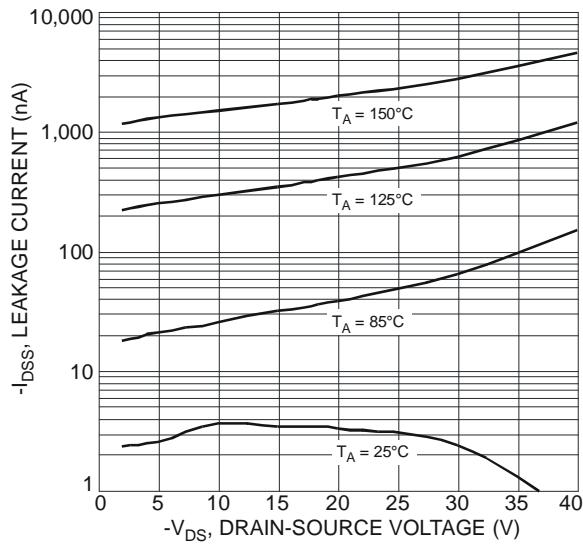


Fig. 21 Typical Leakage Current vs. Drain-Source Voltage

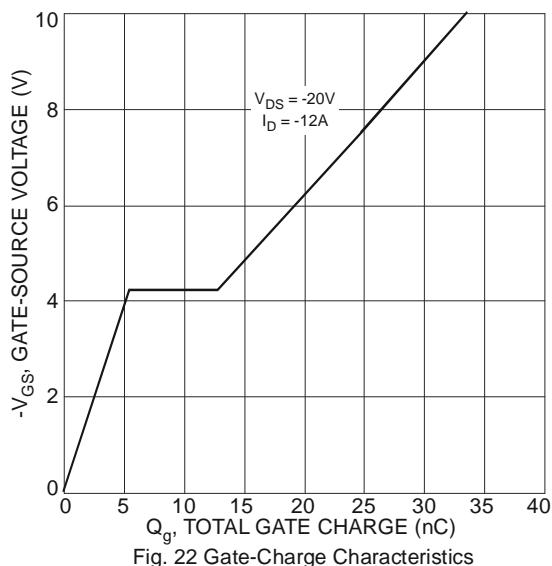
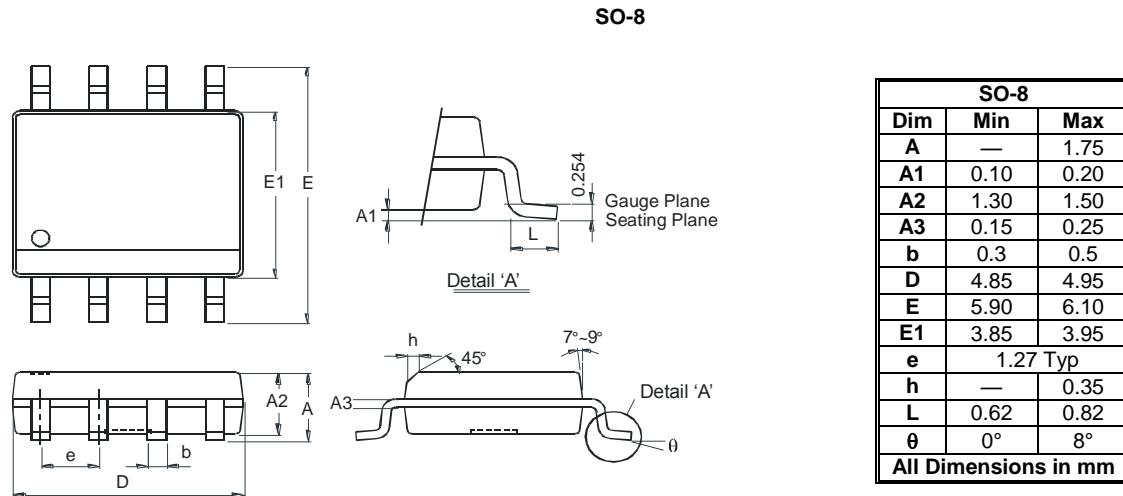


Fig. 22 Gate-Charge Characteristics

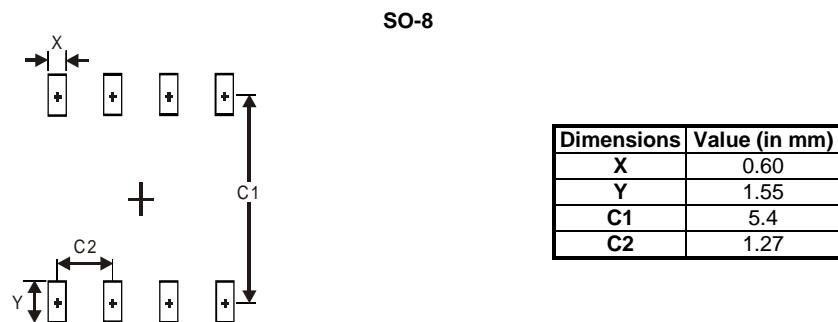
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



Suggested Pad Layout

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