

**PI3HDX1212**
**12Gbps HDMI 2.1 1:2 Signal Duplicator**

## Description

The DIODES PI3HDX1212 active-drive Signal Duplicator solution is targeted for high-resolution video networks that are based on HDMI™ 2.1 standards signal processing.

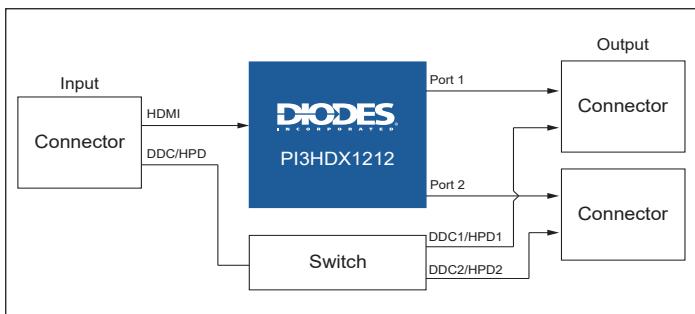
The PI3HDX1212 is an active single port to dual ports Signal Duplicator. The device drives differential signals to multiple video display units. Depending on the mode select pin, the PI-3HDX1212 provides controllable equalizer, flat gain and output swing linearity that can be manipulated through pin control or I2C control.

The maximum HDMI data rate of 12Gbps produces a 8K@60Hz resolution or 4K@120Hz, required for 8K HDTV, PC graphics products and other peripheral device. For PC graphics application, the device sits at the driver's side and fan out differential signals to multiple display units, such as a PC LCD monitor, projector, TV, etc. The CTLE equalizers are implemented at the inputs of the ReDriver to reduce the ISI jitters and compensate channel loss. The PI3HDX1212 ensures the transmittal of high bandwidth video streams from Video sources to the end-display units.

## Application(s)

- Display Peripheral Box
- Digital Signage Display
- Multi Screen Splicing

## Application Diagram



## Features

- 1-to-2 Active Signal Duplicator for 4-lane HDMI2.1 Operation
- Data Rate Support up to 12Gbps and support 8K4K pixel resolution
- Quad-level Equalizer Gain Value Selection controlled by pin strap or I2C mode programming
- Quad-level Flat Gain and Output Swing Linearity Selection controlled by pin strap or I2C mode programming
- ESD Protection on I/O Pins: 2KV HBM
- Single Power Supply: 3.3V
- Temperature Support: -40°C to +70°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.
- <https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green):
  - 40-pin, TQFN, 3 x 6 mm (0.4 mm pitch) (ZLD)

## Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX1212ZLDEX	ZLD	TQFN (W-QFN3060-40)

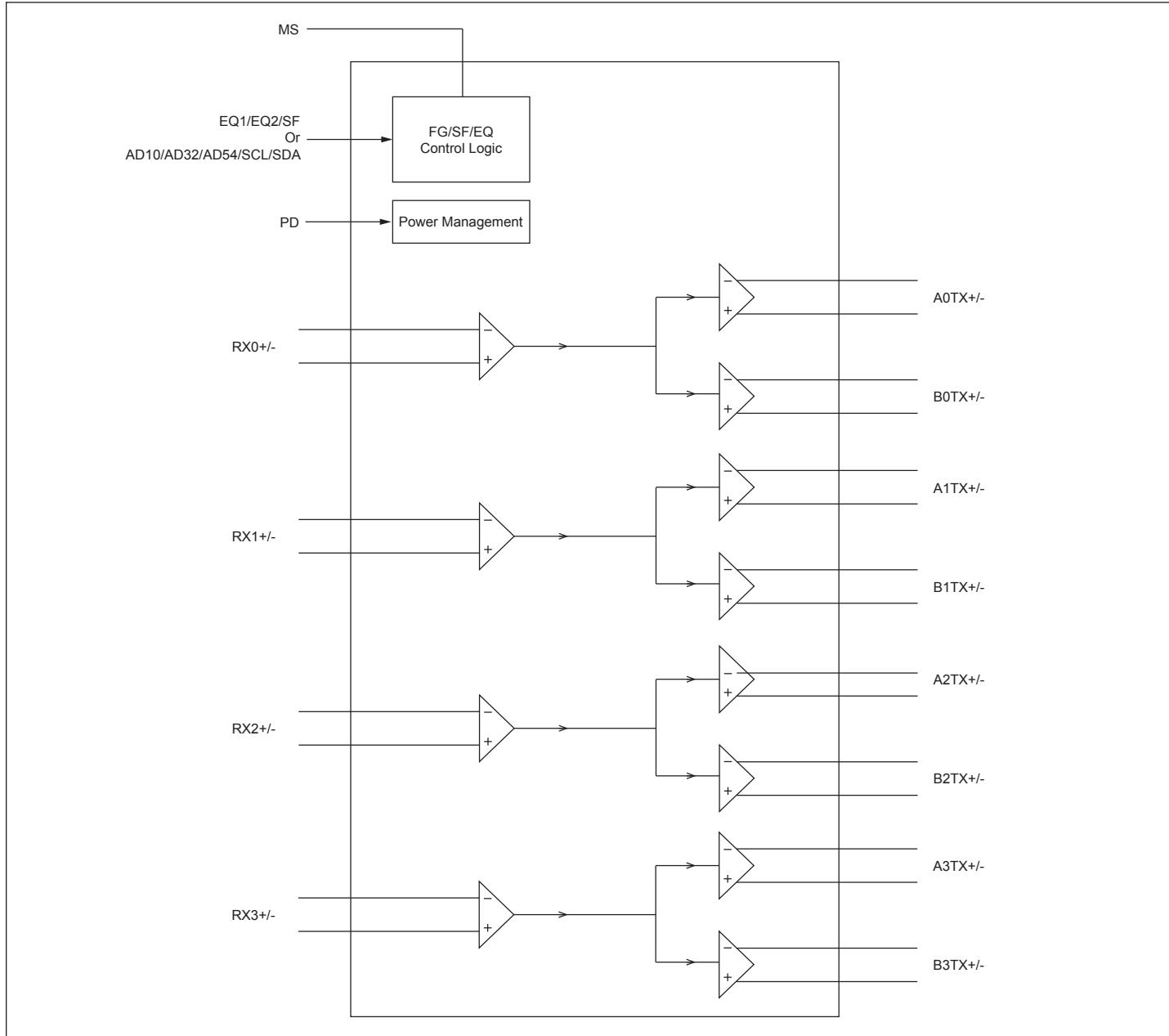
### Notes:

- E = Pb-free and Green
- X suffix = Tape/Reel

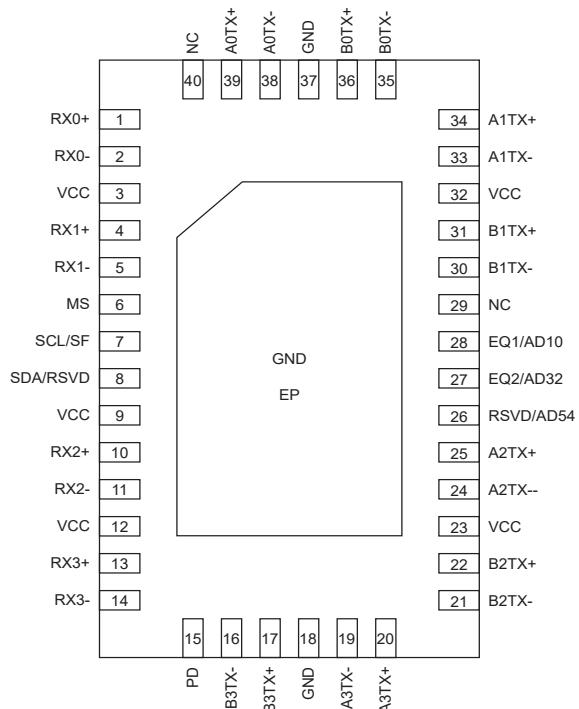
### Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Block Diagram



## Pin Configuration (Top View)



## Pin Configuration (Top View)

Pin #	Pin Name	Type	Description
<b>Data Signals</b>			
1, 2	RX0+, RX0-	I	CML Inputs for Channel 0 with internal 50Ω to Vcc or HIZ.
39, 38	A0TX+, A0TX-	O	CML Outputs for Channel A0/B0 with internal 50Ω pullup or HIZ.
36, 35	B0TX+, B0TX-		
4, 5	RX1+, RX1-	I	CML Inputs for Channel 1 with internal 50Ω to Vcc or HIZ.
34, 33	A1TX+, A1TX-	O	CML Outputs for Channel A1/B1 with internal 50Ω pullup or HIZ.
31, 30	B1TX+, B1TX-		
10, 11	RX2+, RX2-	I	CML Inputs for Channel 2 with internal 50Ω to Vcc or HIZ.
25, 24	A2TX+, A2TX-	O	CML Outputs for Channel A2/B2 with internal 50Ω pullup or HIZ.
22, 21	B2TX+, B2TX-		
13, 14	RX3+, RX3-	I	CML Inputs for Channel 3 with internal 50Ω to Vcc or HIZ.
20, 19	A3TX+, A3TX-	O	CML Outputs for Channel A3/B3 with internal 50Ω pullup or HIZ.
17, 16	B3TX+, B3TX-		

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Pin #	Pin Name	Type	Description
<b>Control Pins</b>			
28, 27, 26	EQ1, EQ2, RSVD	I	4-Level input pins with internal 100KΩ pullup and 200KΩ pulldown resistor. Sets the amount of Equalizer Boost on A & B Channel. Reserved Pin Must tie to Ground
	AD10, AD32, AD54	I	4-Level input pins with internal 100KΩ pullup and 200KΩ pulldown resistor. Sets the I <sup>2</sup> C slave address
7, 8	SF, RSVD	I	4-Level input pins with internal 100KΩ pullup and 200KΩ pulldown resistor. Sets the output swing and flat gain level on A & B Channel. Reserved Pin Must tie to Ground
	SCL, SDA	I	I <sup>2</sup> C SCL clock input and data input
6	MS	I	Input with internal 300KΩ pullup resistor. Pin mode enable pin Tie High = Pin mode Tie Low = Register access I <sup>2</sup> C slave mode
29, 40	NC		Not Connected
15	PD	I	Input with internal 300KΩ pullup resistor. When High, the device is put in Power Down Mode. When Low, the device is Enable and in Normal Operation
<b>Power Pins</b>			
3, 9, 12, 23, 32	VCC	PWR	3.3V Supply Voltage
18, 37, EP	GND	PWR	Exposed pad. Supply Ground.

## Functional Description & Circuit Block Description

### Power Enable Function

When PD is set to high, the IC goes into power down mode, both input and output termination are set to high impedance, the I2C R/W can't be executed, and the I2C registers won't be reset to default value. When PD is set to low, the chip is enable and in normal operation, and individual channel power down can be done through the I2C register programming.

### EQ Setting in Pin Mode and I2C Mode

Table 1. EQ1/EQ2 are the Selection Pins for the Equalization Setting

Equalizer Setting (dB)						
EQ1	EQ2	I <sup>2</sup> C EQ<2:0>	@1.25GHz	@1.7GHz	@3GHz	@6GHz
0	0/R	000	0.6	1.0	2.6	7.2
0	F/1	001	0.7	1.2	3.2	8.2
R	0/R	010	2.1	2.6	4.2	8.8
R	F/1	011	2.3	3.0	5.0	10.2
F	0/R	100	3.2	3.9	6.0	11.3
F	F/1	101	3.5	4.3	6.8	12.4
1	0/R	110	4.4	5.2	7.8	13.5
1	F/1	111	4.9	5.9	9.0	15.0

### Swing and Flat Gain Setting

Table 2. Swing and Flat Gain Setting for SF

SF	Swing (mVp-p)	Flat Gain (dB)
0	1000	-3.5
R	1000	-0.5
F	1200	-3.5
1	1200	-0.5

Table 3. Swing Settings in I<sup>2</sup>C Mode

SW1	SW0	Swing (mVp-p)
0	0	800
0	1	1000 (default)
1	0	1100
1	1	1200

Table 4. Flat Gain Setting in I<sup>2</sup>C Mode

FG1	FG0	Flat Gain (dB)
0	0	-3.5
0	1	-2
1	0	-0.5 (default)
1	1	1

## I<sup>2</sup>C Operation

The integrated I<sup>2</sup>C interface operates as slave device when 'MS' set to logic low. Standard mode (100Kbps) is supported with 7-bit addressing. The data byte format is 8-bit bytes and supports the format of indexing to be compatible with other bus devices. In the Slave mode (MS = LOW), the device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred.

Address bits A5 to A0 are programmable to support multiple chips environment.

## Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte must be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I<sup>2</sup>C Data Transfer diagram). The device never holds the clock line SCL LOW to force the master into a wait state.

## Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the device pulls down the SDA line during the acknowledge clock pulse, so it remains stable LOW during the HIGH period of this clock pulse as indicated in the I<sup>2</sup>C Data Transfer diagram. The device generates an acknowledge after each byte has been received.

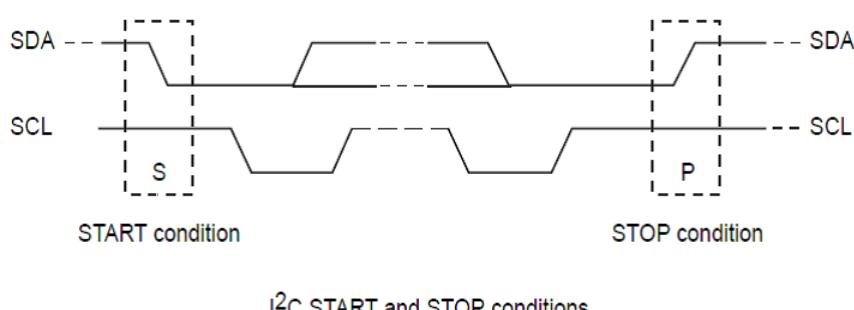
## Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the device watches the next byte of information for a match with its address setting. When a match is found it responds with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit except for the last byte of a read cycle, which ends with a stop bit. For a write cycle, the first data byte following the address byte is an index byte that is used by the device. Data is transferred with the most significant bit (MSB) first.

## I<sup>2</sup>C Data Transfer

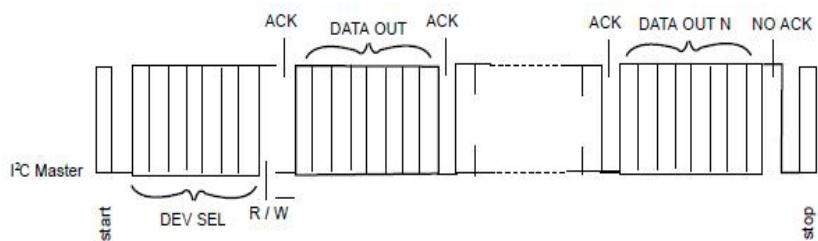
### Start & Stop Conditions

A HIGH-to-LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW-to-HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below.

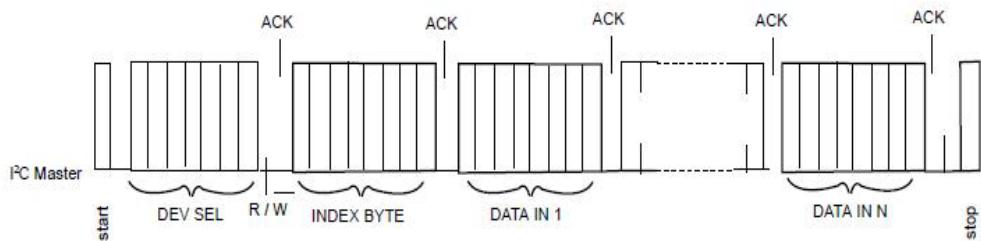


## I<sup>2</sup>C Data Transfer

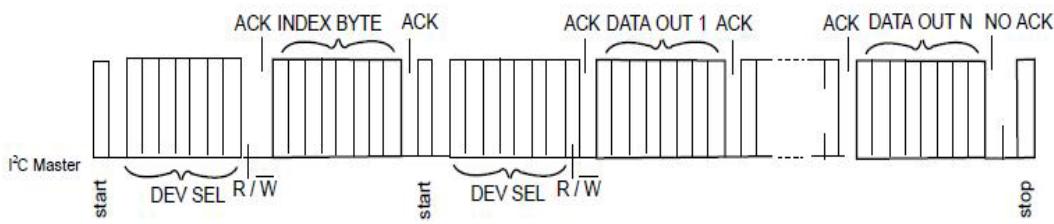
### 1. Read sequence



### 2. Write sequence



### 3. Combined sequence



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**Table 5. I<sup>2</sup>C Address Settings**

AD54	AD5	AD4
0	0	0
R	0	1
F	1	0
1	1	1

AD32	AD3	AD2
0	0	0
R	0	1
F	1	0
1	1	1

AD10	AD1	AD0
0	0	0
R	0	1
F	1	0
1	1	1

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## I<sup>2</sup>C Programming

### Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	AD5	AD4	AD3	AD2	AD1	AD0	1=R, 0=W

### BYTE 0

Bit	Type	Power up Condition	—	Control Affected	Comment
7	R	0			
6	R	0			
5	R	1			
4	R	1			
3	R	0			
2	R	0			
1	R	0			
0	R	0			

Rev. ID = 0x0

### BYTE 1

Bit	Type	Power up Condition	—	Control Affected	Comment
7	R	0			
6	R	0			
5	R	0			
4	R	0			
3	R	0			
2	R	0			
1	R	0			
0	R	0			

Reserved

**BYTE 2**

Bit	Type	Power up Condition	—	Control Affected	Comment
7	R/W	0		Channel 3 Power down	
6	R/W	0		Channel 2 Power down	
5	R/W	0		Channel 1 Power down	
4	R/W	0		Channel 0 Power down	
3	R/W	1		Reserved	
2	R/W	1		Reserved	
1	R/W	0		Demux mode Enable	Demux enable pin 0 = Signal Duplicator mode 1 = Demux mode
0	R/W	1		Demux mode selection	1 = Ch A 0 = Ch B

**BYTE 3**

Bit	Type	Power up Condition	—	Control Affected	Comment
7	R/W	0	Channel 0 configuration		Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	1		FG1	Flat Gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	1		SW0	

**BYTE 4**

Bit	Type	Power up Condition	—	Control Affected	Comment
7	R/W	0	Channel 1 configuration		Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	1		FG1	Flat Gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	1		SW0	

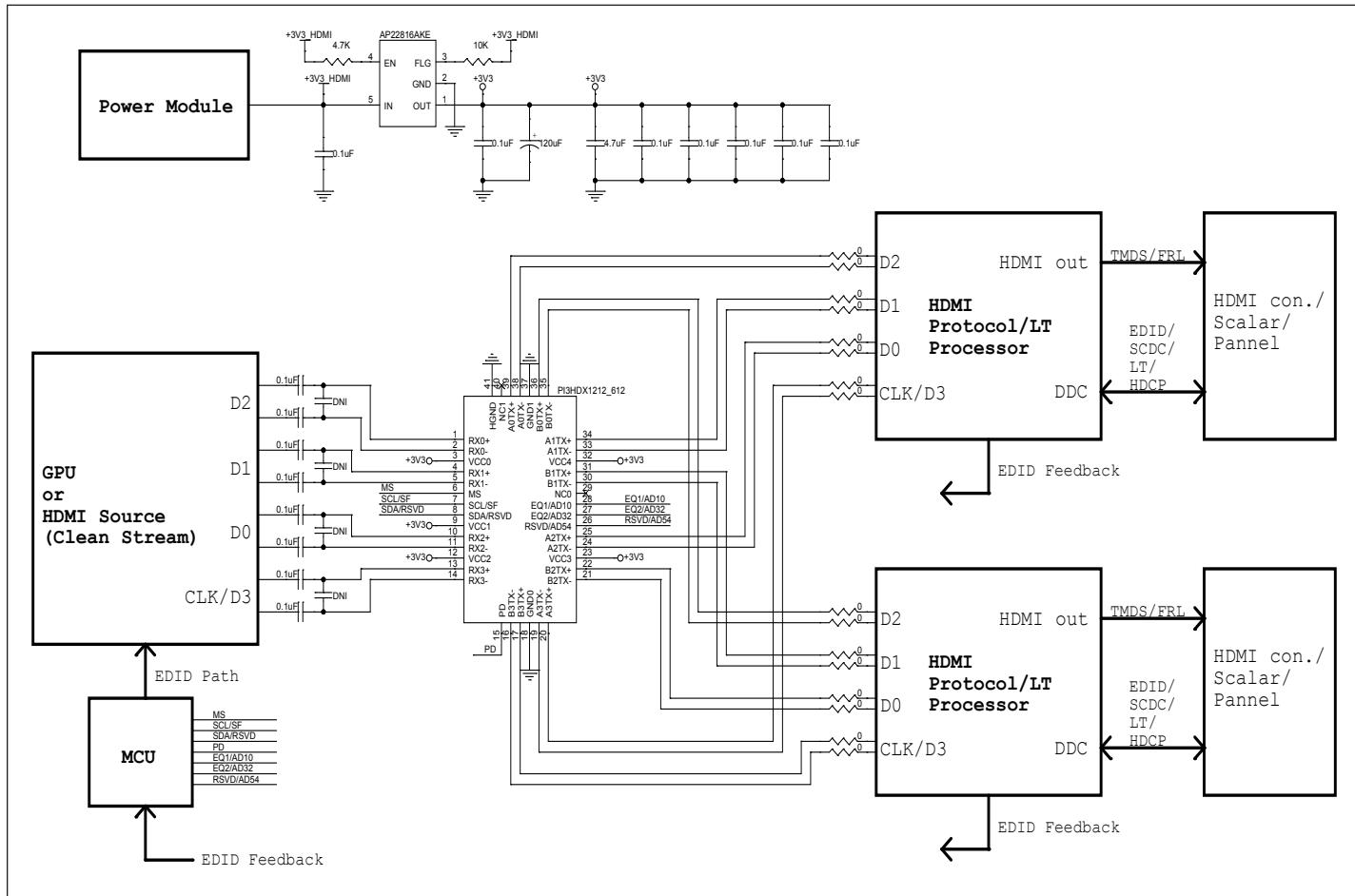
**PI3HDX1212**
**BYTE 5**

Bit	Type	Power up Condition	—	Control Affected	Comment
7	R/W	0	Channel 2 configuration		Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	1		FG1	Flat Gain
2	R/W	0		FG0	
1	R/W	0		SW1	
0	R/W	1		SW0	Swing

**BYTE 6**

Bit	Type	Power up Condition	—	Control Affected	Comment
7	R/W	0	Channel 3 configuration		Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	1		FG1	Flat Gain
2	R/W	0		FG0	
1	R/W	0		SW1	
0	R/W	1		SW0	Swing

## Application Schematics



## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Supply Voltage to Ground Potential .....	-0.5V to +3.8V
DC SIG Voltage .....	-0.5V to V <sub>CC</sub> +0.5V
ESD, HBM .....	2KV

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Thermal Information

Symbol	Parameter	40-TQFN (ZLD) Package	Units
Theta JA	Junction to ambient thermal resistance	17.91	°C/W

## Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD	Supply Voltage	2.97	3.3	3.63	V
TA	Ambient Temperature	-40		+70	°C

## Electrical Characteristics - LVCMOS I/O DC Specifications

V<sub>CC</sub> = 3.3 ± 0.3V, T<sub>A</sub> = -40°C to 70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>IH</sub>	DC Input Logic High		0.44 VCC		VCC+0.3	V
V <sub>IL</sub>	DC Input Logic Low		-0.3		0.1 VCC	V

### 4-Level Control Pins

V <sub>IH</sub>	DC Input Logic "High"		0.92×VCC	VCC		V
V <sub>IF</sub>	DC Input Logic "Float"		0.59×VCC	0.67×VCC	0.75×VCC	V
V <sub>IR</sub>	DC Input Logic "With Rext to GND"		0.25×VCC	0.33×VCC	0.41×VCC	V
V <sub>IL</sub>	DC Input Logic "Low"			GND	0.08×VCC	V
I <sub>IH</sub>	Input High Current				50	µA
I <sub>IL</sub>	Input Low Current		-50			µA
Rext	External Resistance Connects to GND (±5%)		64.6	68	71.4	kΩ

## Electrical Characteristics - SDA and SCL I/O for I2C-bus

$V_{CC} = 3.3 \pm 0.3V$ ,  $T_A = -40^\circ C$  to  $70^\circ C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{IH}$	DC input logic high		$V_{CC}/2+0.7$		$V_{CC}+0.3$	V
$V_{IL}$	DC input logic low		-0.3		$V_{CC}/2-0.7$	V
$V_{OL}$	DC output logic low	$I_{OL} = 3mA$			0.4	V
$V_{hys}$	Hysteresis of Schmitt trigger input		0.8			V
$t_{of}$	Output fall time from $V_{IH\min}$ to $V_{IL\max}$ with bus cap. 10-400pF				250	ns
$f_{SCLK}$	SCLK clock frequency				100	kHz

## Electrical Characteristics - High Speed I/O AC/DC Specifications

$V_{CC} = 3.3 \pm 0.3V$ ,  $T_A = -40^\circ C$  to  $70^\circ C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$C_{RX}$	RX AC Coupling Capacitance			220		nF
$S_{11}$	Input Return Loss	10MHz to 6GHz Differential		-12		dB
		1GHz to 6GHz Common Mode		-5		
$S_{22}$	Output Return Loss	10MHz to 6GHz Differential		-12		dB
		1GHz to 6GHz Common Mode		-8		
$R_{IN}$	DC Single-Ended Input Impedance			50		$\Omega$
	DC Differential Input Impedance			100		
$R_{OUT}$	DC Single-Ended Output Impedance			50		$\Omega$
	DC Differential Output Impedance			100		
$Z_{RX-HIZ}$	DC Input CM Input Impedance During Reset or Power Down			78		k $\Omega$
$V_{RX-DIFF-PP}$	Differential Input Peak-to-Peak Voltage	Operational			1.2	V <sub>ppd</sub>
	Input Source Common-Mode Noise	DC - 200MHz			150	mV <sub>pp</sub>
$V_{cc}$	Power Supply Voltage		3	3.3	3.6	V
$P_{active}$	Supply power @ Active mode, with signal	PD = 0			1660	mW
$I_{active}$	Supply current @ Active mode, with signal				461	mA
$I_{standby}$	Supply current @ Standby mode	PD = 1			110	uA
$t_{pd}$	Latency	From Input to Output		0.5		ns

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
G <sub>P</sub>	Peaking Gain (Compensation at 6GHz, Relative to 100MHz, 100mVp-p Sine Wave Input)	EQ<2:0> = 111 EQ<2:0> = 000		15 7.2		dB
		Variation Around Typical	-3		+3	dB
G <sub>F</sub>	Flat gain (100MHz)	SF = R/1		-0.5		dB
		SF = 0/F		-3.5		dB
		Variation Around Typical	-3		+3	dB
V <sub>1dB_100M</sub>	-1dB Compression Point of Output Swing (at 100MHz)	SF = 1, EQ<2:0> = 111 SF = R, EQ<2:0> = 111		1200 1100		mVppd
V <sub>1dB_8G</sub>	-1dB Compression Point of Output Swing (at 6GHz)	SF = 1, EQ<2:0> = 111 SF = R, EQ<2:0> = 111		1100 900		mVppd
V <sub>Coup</sub>	Channel Isolation	100MHz to 6GHz, at EQ = 000 Figure 1 (Note 1)		-35		dB
V <sub>noise_input</sub>	Input-Referred Noise	100MHz to 6GHz, SF = 1, EQ<2:0> = 000, Figure 2		0.8		mVRMS
		100MHz to 6GHz, SF = 1, EQ<2:0> = 111, Figure 2		0.5		
V <sub>noise_output</sub>	Output-Referred Noise <sup>(2)</sup>	100MHz to 6GHz, SF = 1, EQ<2:0> = 000, Figure 2		0.7		mVRMS
		100MHz to 6GHz, SF = 1, EQ<2:0> = 111, Figure 2		1.0		

**Note:**

1. Measured using a vector-network analyzer (VNA) with -30dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Guaranteed by design and characterization.

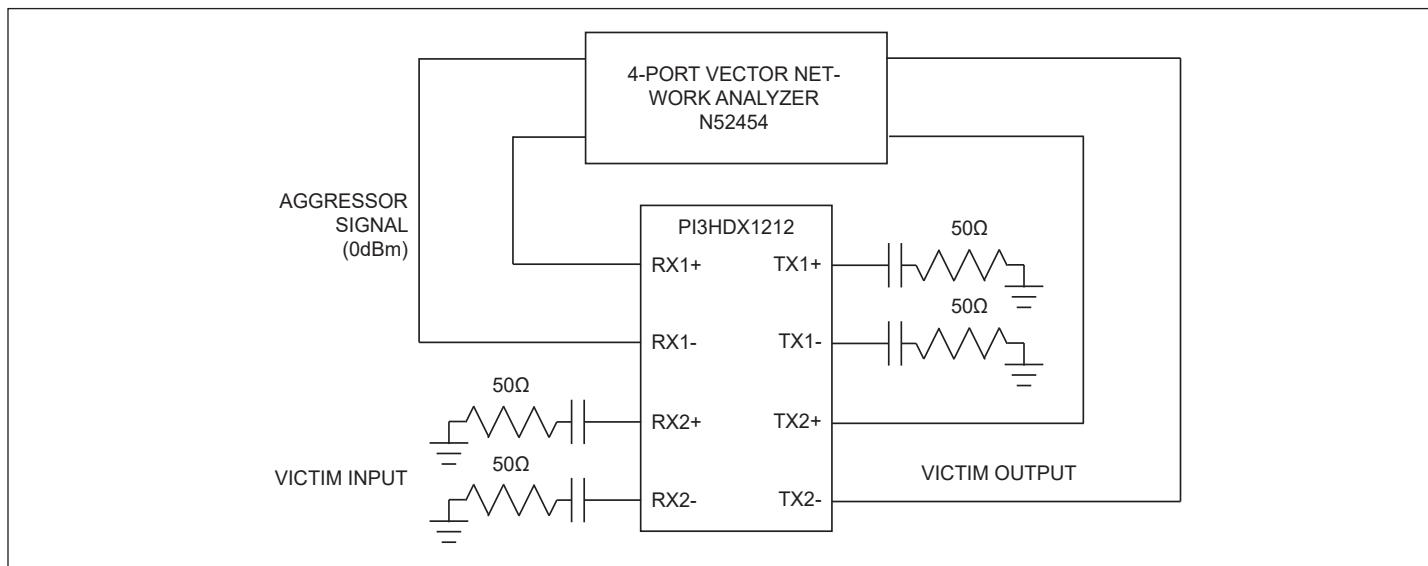


Figure 1. Channel-Isolation Test Configuration

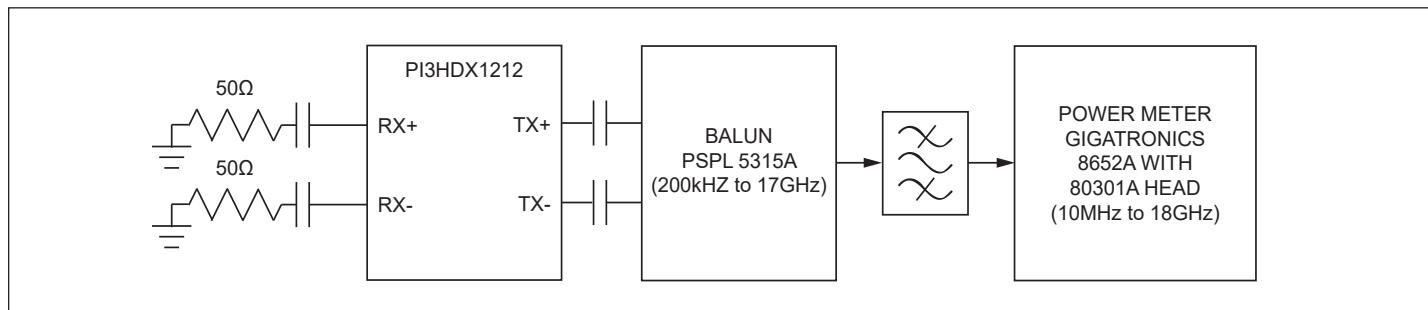


Figure 2. Noise Test Configuration

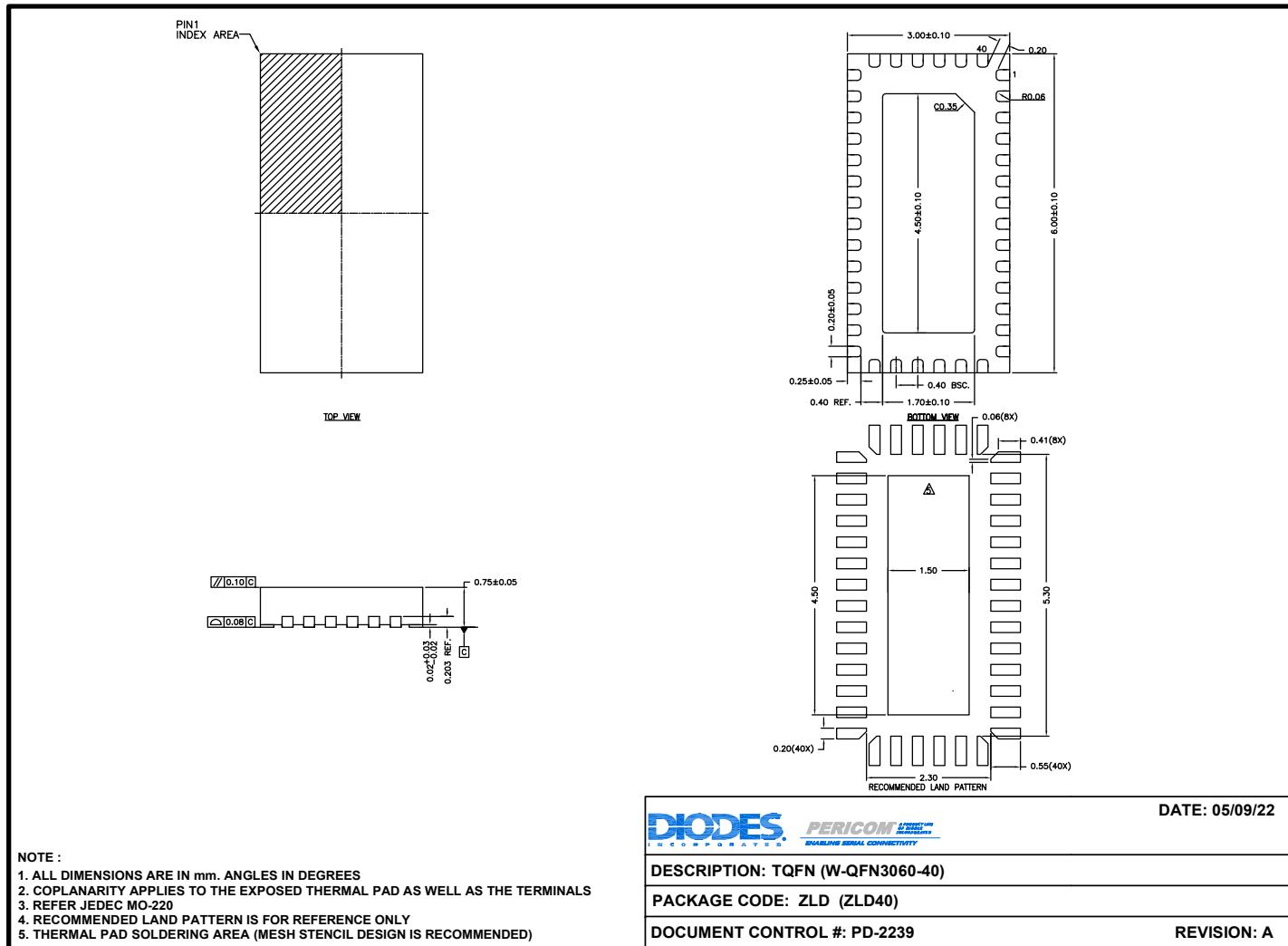
**PI3HDX1212****Part Marking**

PI3HDX12  
12ZLDE  
ZYYWWXX

Z: Die Rev  
YY: Year  
WW: Workweek  
1st X: Assembly Code  
2nd X: Fab Code

## Packaging Mechanical

### 40-TQFN (ZLD)



For latest package info.

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