LOW IQ REVERSE-BATTERY PROTECTION IDEAL DIODE CONTROLLER WITH BUILT-IN VDS CLAMP

Description

The AP74701Q is an automotive AEC-Q100 qualified ideal diode controller, which operates in conjunction with an external n-channel MOSFET as an ideal diode for minimum loss reverse-polarity protection with a 20mV forward voltage drop. The AP74701Q is suitable for input protection of 12V automotive systems. The 3.2V input-voltage support is particularly well suited for severe cold crank requirements in automotive systems.

The device controls the GATE of the MOSFET to regulate the forward voltage drop at 20mV. The regulation scheme enables immediate turn-off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. Immediate response (< 0.75µs) to reverse current blocking makes the device suitable for systems with output voltage hold-up requirements during ISO7637 pulse testing as well as power fail and input micro-short conditions. The AP74701Q has a built-in V_{DS} clamp feature which enables users to achieve "TVS Less" input polarity protection solution and save on average a typical 60% of PCB space in constrained automotive systems.

The AP74701Q controller provides a charge pump gate drive for an external n-channel MOSFET. With the enable pin low, the controller is off and draws approximately 1µA of current.

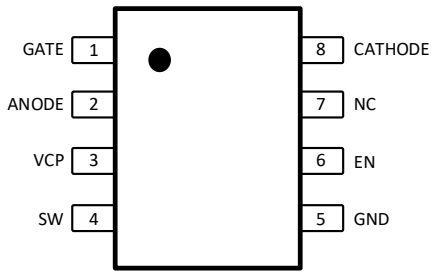
The AP74701Q is available in the SOT28 package.

Applications

- Automotive infotainment systems – head units, telematics, control units
- Automotive ADAS systems - cameras
- Active power ORing for redundant power
- Power of industrial automation such as PLC
- Enterprise power supplies

Pin Assignments

(Top View)



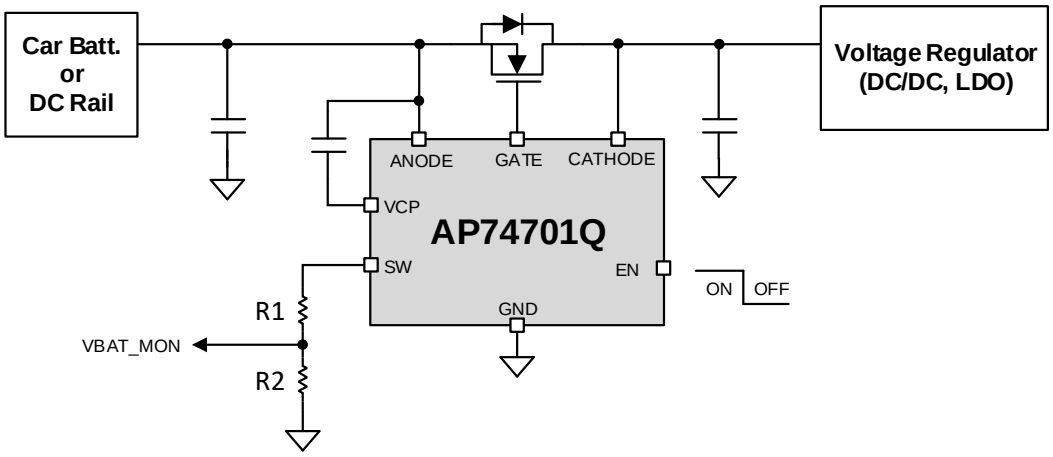
SOT28

Features

- Input Voltage Ranges from 3.2V to 65V (3.9V Startup)
- -33V Reverse-Battery Voltage
- Charge Pump for External N-Channel Power MOSFET
- 20mV ANODE to CATHODE Forward Voltage Drop Control
- Low Shutdown Current of 1µA when Disabled
- Low Quiescent Current of 80µA when Enabled
- Fast Reverse Current Block Response Time of < 0.75µs
- 2.3A Peak Gate Turn-Off Current
- Active High Operation
- Integrated Battery Voltage Monitoring Switch (SW)
- Meet Automotive ISO7637 Transient Requirements Without Additional Input TVS Diodes (TVS Less)
- ESD Protection: 2kV of HBM and 750V of CDM
- AEC-Q100 Qualification Compliance with Device Temperature Grade 1 (-40°C to +125°C Ambient Operating Temperature Range)
- 8-Pin SOT28 Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP74701Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

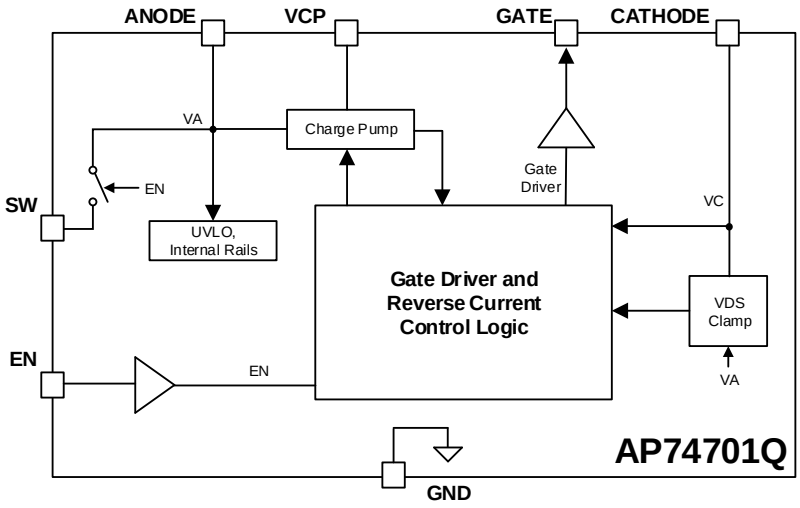
Typical Applications Circuit



Pin Descriptions

Pin Name	Pin Number	Function
GATE	1	Gate driver out pin. Connects to gate of external nMOSFET
ANODE	2	Input supply and ANODE of Ideal diode. Connects to the source of external nMOSFET
VCP	3	Charge pump voltage output pin. Connect to external capacitor.
SW	4	Voltage sensing switch terminal. Internal switch is ON connecting ANODE to SW when EN is high. A resistor divider from this pin to GND can be used to for adjustment for ADC full-scale range. When EN is low, the switch is OFF disconnecting the resistor divider from the battery line thereby eliminating the leakage current.
GND	5	Ground pin
EN	6	Enable pin. Active high
NC	7	No Connect. Leave this pin float
CATHODE	8	CATHODE pin. Connects to the drain of external nMOSFET

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body ESD Protection	±2	kV
ESD CDM	Charged Device Model ESD Protection	±750	V
ANODE to GND	Input Voltage at ANODE	-(V_{CLAMP} - 1) to +65	V
SW and EN to GND	Voltage at SW and EN, V_{ANODE} > 0V	-0.3 to +65	V
EN to GND	Voltage at EN, V_{ANODE} ≤ 0V	V_{ANODE} to (V_{ANODE} + 65)	V
SW to GND	Voltage at SW, V_{ANODE} ≤ 0V	V_{ANODE} to (V_{ANODE} + 0.3)	V
I_{SW}	SW Switch Current	-1 to 3mA	A
GATE to ANODE	Gate to Anode Voltage	-0.3 to +15	V
VCP to ANODE	Charge Pump Voltage	-0.3 to +15	V
CATHODE to ANODE	CATHODE to ANODE Voltage	-5 to V_{CLAMP}	V
$T_{J(max)}$	Maximum Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-40 to +150	°C
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (Note 5)	176.9	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance (Note 5)	122.0	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance (Note 5)	46.0	°C/W
Ψ_{JT}	Junction-to-Top Characterization Parameter (Note 5)	10.2	°C/W
Ψ_{JB}	Junction-to-Board Characterization Parameter (Note 5)	44.9	°C/W

Notes: 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.

5. $R_{\theta JA}$ and $R_{\theta JC}$ are measured at T_A = +25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
ANODE to GND	Input Voltage at ANODE	-33	+60	V
CATHODE to GND	Input Voltage at CATHODE	—	+60	V
EN to GND	Voltage at Enable Pin	-33	+60	V
ANODE to CATHODE	ANODE to CATHODE Voltage	-V_{CLAMP}	5	V
GATE to ANODE	Gate to Anode Voltage	0	+15	V
VCP to ANODE	Charge Pump Voltage	0	+15	V
CATHODE to ANODE	CATHODE to ANODE Voltage	—	70	V
Anode Cap	Input Capacitor (Note 6)	0.1	1	µF
VCP to Anode Cap	Charge Pump Cap (Note 6)	0.1	—	µF
External MOSFET V_{GS} max	Gate to Anode (Note 6)	15	—	V
T_J	Operating Junction Temperature Range	-40	+125	°C

Note: 6. Refer to the typical application circuit.

Electrical Characteristics (T_J = -40°C to +125°C, V_{ANODE} = 12V, C_{VCP} = 0.1µF, V_{EN} = 3.3V, typical values are at T_J = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VANODE Supply						
V_{CLAMP}	$V_{CATHODE}$ – V_{ANODE} Clamp Voltage	—	34	—	43	V
V_{ANODE}	Operating Input Voltage	—	4	—	60	V
V_{UVLO_ANODE}	ANODE UVLO Rising Threshold	—	—	—	3.9	V
	ANODE UVLO Falling Threshold	—	2.2	2.8	3.1	V
$V_{UVLO\_ANODE\_HYS}$	ANODE UVLO Hysteresis	—	440	—	800	mV
I_{ANODE_OFF}	Shutdown Supply Current	V_{EN} = 0V	—	0.6	1.5	µA
I_{ANODE_Q}	Operating Quiescent Current	—	—	65	100	µA
EN Input						
V_{IL_EN}	Enable Input Low Threshold	—	0.5	0.9	1.22	V
V_{IH_EN}	Enable Input High Threshold	—	1.06	2	2.6	V
V_{hys_EN}	Enable Hysteresis	—	0.52	—	1.35	V
I_{EN}	Enable Sink Current	V_{EN} = 12V	—	3	5	µA
VANODE and VCATHODE by Operation Modes						
V_{ACTIVE_REG}	Regulated Forward Threshold	—	13	24	34	mV
V_{ACTIVE_FULL}	Threshold for Full Conduction Mode	—	40	55	67	mV
V_{ACTIVE_REV}	Threshold for Reverse Current Blocking	—	-17	-11	-2	mV
Gm	Regulation Error AMP Transconductance (Note 7)	—	1200	1800	3100	µA/V
SW Switch						
R_{SW}	Resistance of Battery Sensing Isolation Switch	4V < VANODE ≤ 60V	25	46	90	Ω
Gate Drive						
I_{GATE}	Peak Source Current	V_{ANODE} – $V_{CATHODE}$ = 100mV, V_{GATE} – V_{ANODE} = 5V	3	11	—	mA
	Peak Sink Current	V_{ANODE} – $V_{CATHODE}$) = -20mV, V_{GATE} – V_{ANODE} = 5V	—	2370	—	mA
	Regulation Max Sink Current	V_{ANODE} – $V_{CATHODE}$ = 0V, V_{GATE} – V_{ANODE} = 5V	2	16	—	µA
R_{DIS}	Discharge Switch Resistance	V_{ANODE} – $V_{CATHODE}$ = -20mV, V_{GATE} – V_{ANODE} = 100mV	0.4	—	2	Ω

Note: 7. Parameter guaranteed by design and characterization

Electrical Characteristics (T_J = -40°C to +125°C, V_{ANODE} = 12V, C_{VCP} = 0.1µF, V_{EN} = 3.3V, typical values are at T_J = +25°C, unless otherwise specified.) (continued)

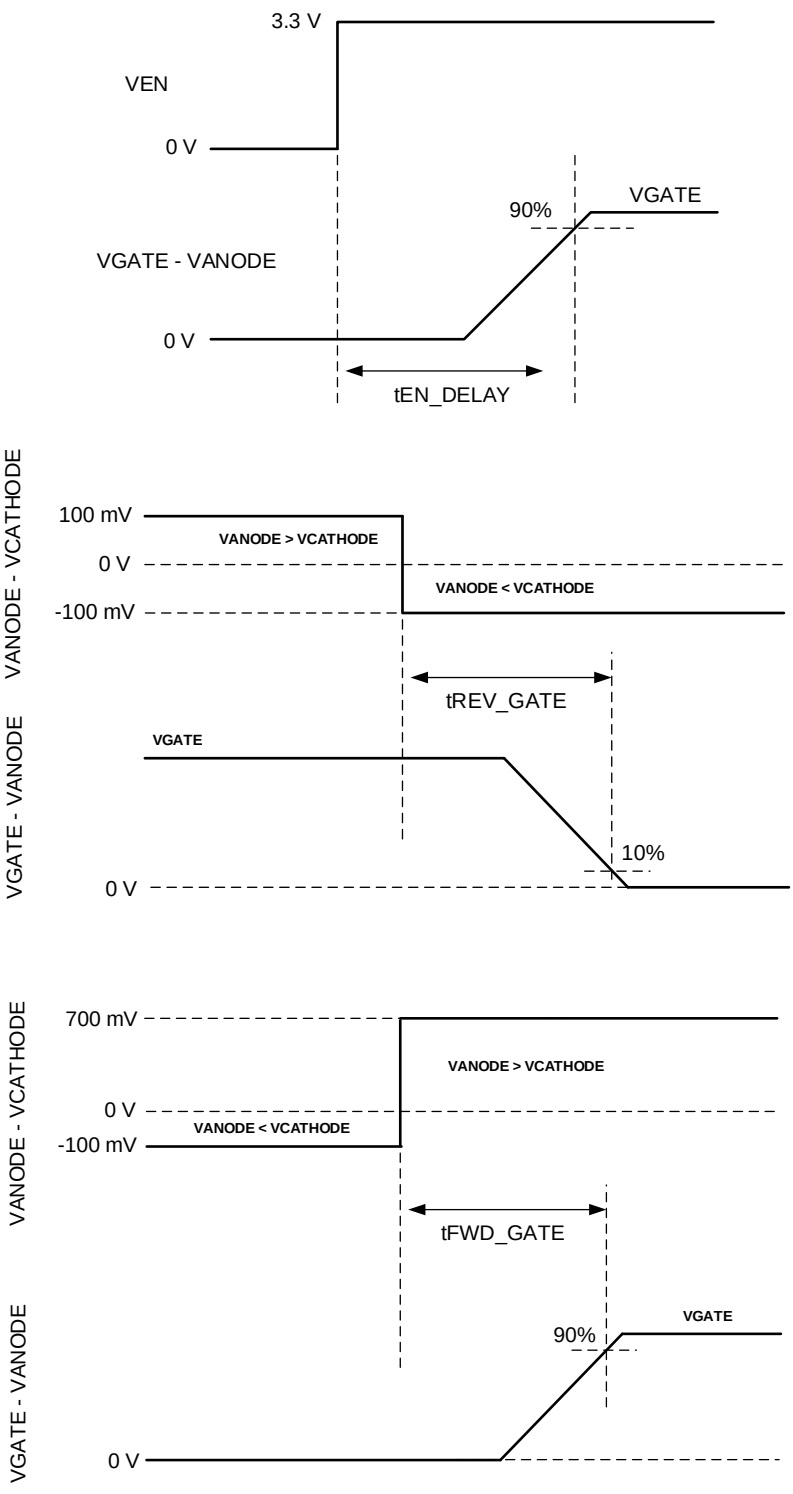
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Charge Pump						
I_{VCP}	Charge Pump Source Current (Charge Pump On)	$V_{VCP} - V_{ANODE}$ = 7V	160	220	600	µA
	Charge Pump Sink Current (Charge Pump Off)	$V_{VCP} - V_{ANODE}$ = 14V	—	5	10	µA
$V_{VCP} - V_{ANODE}$	Charge Pump Voltage at V_{ANODE} = 3.2V	$I_{VCP} \leq$ 30µA	8	—	—	V
	Charge Pump Turn-On Voltage	—	10.3	11.6	13	V
	Charge Pump Turn-Off Voltage	—	11	13	14	V
	Charge Pump Enable Comparator Hysteresis	—	0.4	1	1.8	V
V_{VCP_UVLO}	$V_{VCP} - V_{ANODE}$ UV Release at Rising Edge	$V_{ANODE} - V_{CATHODE}$ = 100mV	5.41	6.5	7.5	V
	$V_{VCP} - V_{ANODE}$ UV Threshold at Falling Edge	$V_{ANODE} - V_{CATHODE}$ = 100mV	4.21	5.3	6	V
CATHODE						
$I_{CATHODE}$	CATHODE Sink Current	V_{ANODE} = 12V, $V_{ANODE} - V_{CATHODE}$ = -100mV	—	1.7	2	µA
		$V_{ANODE} - V_{CATHODE}$ = 100mV	—	1.2	2.5	µA
		V_{ANODE} = -14V, V_{DRAIN} = 0V	—	—	2	µA
		V_{ANODE} = -16V, $V_{CATHODE}$ = 16V	—	—	24	µA

Switching Characteristics (T_J = -40°C to +125°C, V_{ANODE} = 12V, C_{VCP} = 0.1µF, V_{EN} = 3.3V, typical values are at T_J = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Switching Characteristics						
t_{EN_DELAY}	Delay from Enable Switching High to Gate Turn On	$V_{VCP} > V_{VCP\_UVLO}$	—	75	110	µs
t_{REV_GATE}	Gate Turn-Off Time when Reverse Voltage is Detected (Note 8)	$V_{ANODE} - V_{CATHODE}$ = 100mV to -100mV	—	0.45	0.75	µs
t_{FWD_GATE}	Gate Turn-On Time when Forward Conducting Voltage Detected (Note 8)	$V_{ANODE} - V_{CATHODE}$ = -100mV to 700mV	—	1.4	2.6	µs

Note: 8. Parameter guaranteed by bench characterization

Switching Waveforms



Detailed Description

Overview

The AP74701Q ideal diode controller has all the features necessary to implement an efficient and fast reverse-polarity protection circuit while minimizing the number of external components. This ideal diode controller is paired with an external n-channel MOSFET to replace other reverse-polarity schemes such as a p-channel MOSFET or a Schottky diode. An internal charge pump is used to drive the external n-channel MOSFET to a maximum gate drive voltage of approximately 12V. The voltage drop across the MOSFET is continuously monitored between the ANODE and CATHODE pins, and the GATE to ANODE voltage is adjusted as needed to regulate the forward voltage drop at 20mV. This closed loop regulation scheme enables graceful turn-off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. A fast reverse current condition is detected when the voltage across ANODE and CATHODE pins reduces below -11mV, resulting in the GATE pin being internally connected to the ANODE pin turning off the external n-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin, EN, is available to place the AP74701Q in shutdown mode disabling the n-channel MOSFET and minimizing the quiescent current. When the device is enabled, an internal switch between SW and ANODE pin enables input-voltage monitoring using an external resistor divider connected to SW pin. The device integrates V_{DS} clamp feature which enables input "TVS Less" reverse-polarity protection.

Input Voltage

The ANODE pin is used to power the AP74701Q's internal circuitry, typically drawing 80µA when enabled and 1µA when disabled. If the ANODE pin voltage is greater than the POR rising threshold, then AP74701Q operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from 65V to -33V, allowing the AP74701Q to withstand negative voltage input.

Charge Pump

The charge pump supplies the voltage necessary to drive the external n-channel MOSFET. An external charge pump capacitor is placed between VCAP and ANODE pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor the EN pin voltage must be above the specified input high threshold, V(EN_IH). When enabled, the charge pump sources a charging current of 300µA typical. If EN pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to ANODE voltage must be above the undervoltage lockout threshold, typically 6.5V, before the internal gate driver is enabled. The initial gate driver enable delay can be calculated by following equation:

$$T_{DRV\_EN} = 75\mu s + C_{VCP}\ X\ \frac{V_{VCP\_UVLO}}{300\mu A}$$

where,

C_{VCP} is the charge pump capacitance connected across ANODE and VCP pins

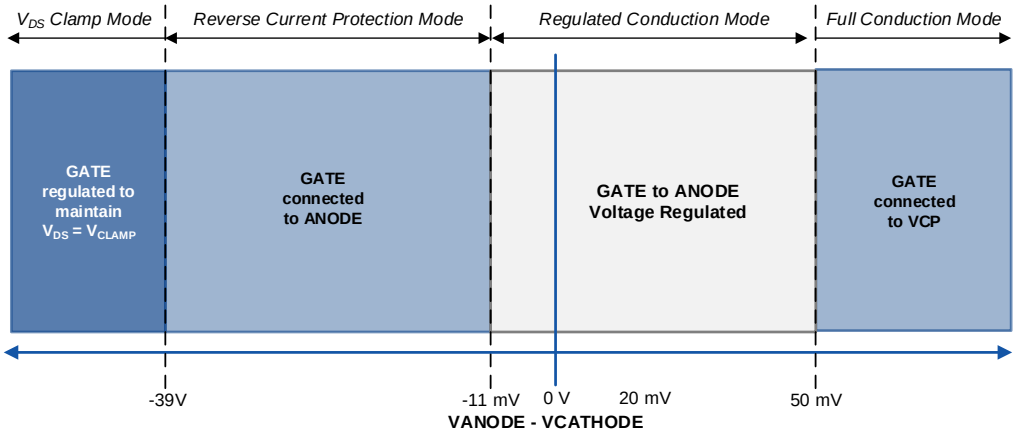
V_{VCP_UVLO} = 6.5V (typical)

To remove any chatter on the gate drive, approximately 800mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to ANODE voltage reaches 12.4V, typically, at which point the charge pump is disabled decreasing the current draw on the ANODE pin. The charge pump remains disabled until the VCAP to ANODE voltage is below to 11.6V typically at which point the charge pump is enabled. The voltage between VCAP and ANODE continue to charge and discharge between 11.6V and 12.4V. By enabling and disabling the charge pump, the operating quiescent current of the AP4701Q is reduced. When the charge pump is disabled, it sinks 5µA typically.

Detailed Description (continued)

Gate Driver

The gate driver is used to control the external n-channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. There are four defined modes of operation that the gate driver operates under forward regulation, full conduction mode, reverse current protection and V_{DS} clamp mode according to the ANODE to CATHODE voltage. The following figure depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the AP74701Q. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE voltage is -11mV. The threshold between reverse current protection mode and V_{DS} clamp mode is when the ANODE to CATHODE voltage is -39V typical.



Before the gate driver is enabled following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP to ANODE voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than VANODE POR rising threshold.

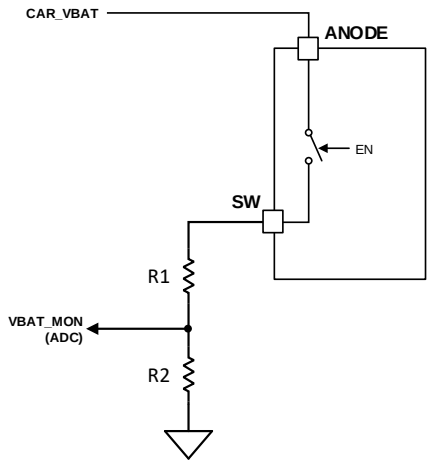
If the above conditions are not achieved, then the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. Once these conditions are achieved the gate driver operates in the correct mode depending on the ANODE to CATHODE voltage.

Enable

The AP74701Q has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Gate Driver* and *Charge Pump* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the AP74701Q in shutdown mode. The EN pin can withstand a voltage as large as 65V and as low as -33V. This allows for the EN pin to be connected directly to the ANODE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 1µA pulls EN pin low and disables the device.

SW Switch

The AP74701Q has "SW" pin to enable battery voltage monitoring in automotive systems. When the device is enabled, an internal switch connects SW pin to ANODE. This enables monitoring battery voltage using an external resistor divider connected from SW pin to GND. When AP74701Q is put in shutdown mode by pulling down the EN pin to ground, an internal switch between SW and ANODE pin is disconnected. This eliminates leakage current by the resistor divider when system is in shutdown state. When not used, "SW" pin should be left floating.



Detailed Description (continued)

Operations

The AP74701Q has shutdown, regulated conduction, full conduction, reverse current protection mode and V_{DS} clamping mode in operation. Details are as follows.

V_{ANODE}	EN	V_{CP} - V_{ANODE}	V_{ANODE} - $V_{CATHODE}$	VCP	V_{GATE}	AP74701Q Mode
< -39V	Don't Care	Don't Care	< -39V	OFF	Regulated	V_{DS} Clamping Mode
-39V to 0V			Reverse Voltage	OFF	NA	OFF (No Power)
0V to UVLO			Forward Voltage			Shutdown
UVLO to 60V	< VEN_IL				ANODE	
	> VEN_IH	< VCP_UVLO		ON		VCP Charging
		> VCP_UVLO	< -39V		Regulated	V_{DS} Clamping Mode
			-39V to -11mV		ANODE	Reverse Current Protection
			-11mV to 50mV		Regulated	Regulated Conduction (Light Load)
			> 50mV		VCP	Full Conduction (Heavy Load)

Shutdown Mode

The AP74701Q enters shutdown mode when the EN pin voltage is below the specified input low threshold VIL_EN. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the AP74701Q enters low IQ operation with the ANODE pin only sinking 1µA. When the AP74701Q is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET's body diode.

Regulated Conduction Mode

For the AP74701Q to operate in regulated conduction mode, the gate driver must be enabled and the current from source to drain of the external MOSFET must be within the range to result in an ANODE to CATHODE voltage drop of -11mV (typ) to 50mV (typ). During forward regulation mode the ANODE to CATHODE voltage is regulated to 20mV (typ) by adjusting the GATE to ANODE voltage. This regulation enables turn-off of the MOSFET at very light loads and ensures no DC reverse current flow.

Full Conduction Mode

For the AP74701Q to operate in full conduction mode, the gate driver must be enabled and the current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE voltage drop of greater than 50mV (typ). If these conditions are achieved the GATE pin is internally connected to the VCP pin resulting in the GATE to ANODE voltage being approximately the same as the VCP to ANODE voltage. By connecting VCP to GATE, the external MOSFET's $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

V_{DS} Clamping mode

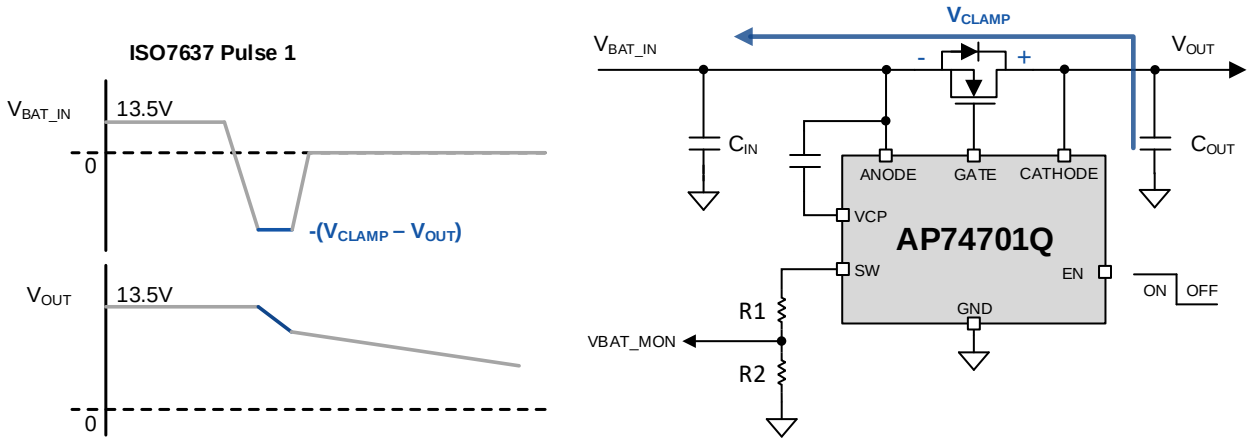
The AP74701Q features an integrated V_{DS} clamp that operates the external MOSFET as an active clamp element to dissipate automotive EMC transients such as ISO7637-2 pulse 1 transient where there is no output voltage hold-up requirement and system is allowed to turn off during such EMC transients. V_{DS} clamp threshold is selected such that the AP74701Q does not engage into V_{DS} clamp operation, thereby ensuring the FET remains OFF during the RCB state for the system level EMC tests where output voltage hold-up is required such as input short interruptions/micro cuts (LV124 E-10, ISO16750-2).

When the ISO7637 pulse 1 is applied at the input of AP74701Q:

1. Device GATE goes low and turns OFF the MOSFET once the voltage drop across ANODE to CATHODE reaches V_{ACTIVE_REV} threshold.
2. Once the voltage across drain and source of the MOSFET reaches V_{CLAMP} level (34V min), GATE is turned ON back in the saturation region, operating external MOSFET as an active clamp and dissipates the ISO7637 pulse 1 energy.

Note that the reverse current flows from V_{OUT} back to input during the ISO7637 pulse 1 transient event, thus discharging VOUT capacitor. The AP74701Q CATHODE pin can handle negative voltage. However, if application circuit connected to the output of AP74701Q cannot handle negative voltage, then the output filter should be designed to ensure that VOUT does not go negative during ISO7637 pulse 1 test. For all the other ISO7637 pulses (i.e. pulse 2a, 2b, 3a, 3b), which are short duration transients, the input and output filter components filtering effect suppresses these pulses.

Detailed Description (continued)



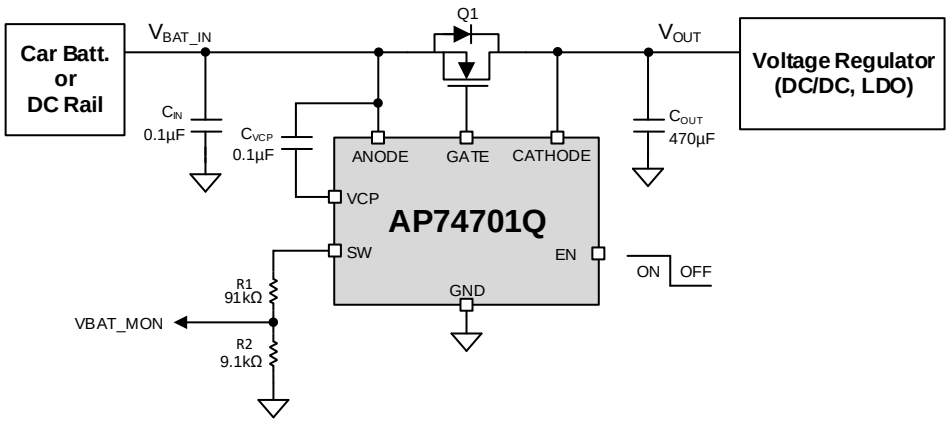
The Typical Circuit Operation of AP74701Q During V_{DS} Clamp at ISO7637 Pulse 1

Reverse Current Protection Mode

For the AP74701Q to operate in reverse current protection mode, the gate driver must be enabled and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE voltage is less than -11mV (typ), reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

Application Information

The AP74701Q is used with n-channel MOSFET to achieve a typical reverse-polarity protection solution. The schematic for the 12V battery protection application is shown below where the AP74701Q is used to drive n-channel MOSFET Q1 in series with a battery. The V_{DS} clamp feature integrated into AP74701Q enables input TVS-less operation. The output capacitor C_{OUT} is recommended to protect the immediate output voltage collapse as a result of line disturbance, and to make sure output remains positive during all system EMC transient tests.



Design Example

Design Parameter	Example Value
V_{VBAT_IN} Range	12V car battery, 12V nominal with 3.2V cold crank and 35V load dump
V_{OUT}	3.2V during cold crank to 35V load dump
I_{OUT}	3A nominal and 5A maximum
C_{OUT}	1µF min, 470µF typical hold-up cap
Automotive EMC Compliance	ISO 7637-2 (-100V, Pulse 1, Pulse 2a, Pulse 2b), ISO 16750-2 (Suppressed load dump 35V), LV124, E-10 (Input Micro Short)

Application Information (continued)

MOSFET Selection

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current ID, the maximum drain-to-source voltage V_{DS_MAX}, the maximum drain-to-source voltage V_{GS_MAX}, safe operating area (SOA), the maximum source current through body diode and the drain-to-source ON resistance $R_{DS(ON)}$.

The maximum continuous drain current (ID) rating must exceed the maximum continuous load current.

To reduce the MOSFET conduction losses, MOSFET with the lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not be beneficial always. Higher $R_{DS(ON)}$ will provide increased voltage information to AP74701Q's reverse current comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with forward voltage drop of less than 50mV at maximum current is a good starting point.

The maximum drain-to-source voltage, V_{DS_MAX}, must be high enough to withstand the highest differential voltage seen in the application. With AP74701Q, the maximum differential voltage across the MOSFET is V_{CLAMP_MAX} of 43V. A minimum of 60V V_{DS} rated is recommended. This would include all the automotive transient events and any anticipated fault conditions.

During the ISO7637 Pulse 1, the maximum V_{DS} seen by the external MOSFET Q1 is $V_{DSCLAMP\_MAX}$ that is 43V. The peak current during ISO7637-2 pulse 1 can be calculated following equation:

$$I_{ISO\_PEAK} = (V_{ISO} + V_{OUT} – V_{DSCLAMP\_MAX}) / R_S$$

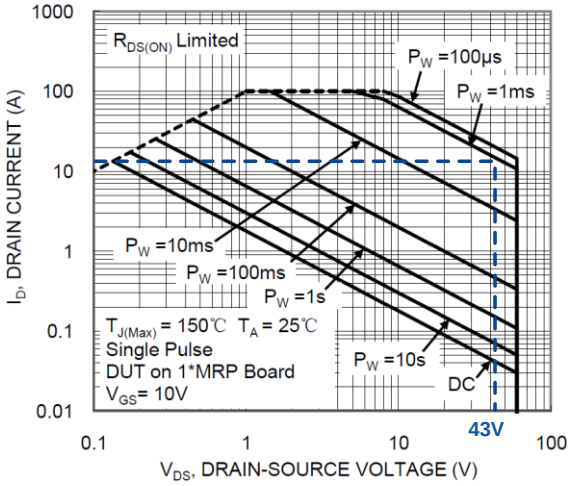
Where

- V_{ISO} is the negative peak of the ISO7637-2 pulse 1
- V_{OUT} is the initial level of the VBAT before ISO pulse is applied
- $V_{DSCLAMP}$ is maximum V_{CLAMP} threshold of AP74701Q
- R_S is the ISO7637 pulse generator input impedance (10Ω)

For ISO7637-2 pulse 1 with amplitude of -100V, V_{OUT} nominal voltage of 13.5V the peak current seen by MOSFET Q1 comes around 7A.

The current profile tapers down from 7A to 0A from the peak of 7A as shown in response to ISO 7637-2 Pulse 1. The resulting average current (I_{ISO_AVG}) can be approximated as one third of the peak current that is around 2.4A. The V_{DS} clamp operation lasts for about 1msec (max). Selecting a MOSFET with SOA characteristics covering the load line of 43V which can support drain current greater than (I_{ISO_PEAK}/2) for 1 msec is a good starting point. For this particular design example, MOSFET which can support greater than 3.5A of drain current at 43V V_{DS} on SOA curve is suitable.

The following curve shows typical SOA characteristics plot of Diodes Incorporated's DMT6007LFGQ highlighting maximum drain current supported by the MOSFET for the duration of 1msec. MOSFET datasheet SOA curves are typically plotted at ambient temperature, so consider sufficient margin over MOSFET parameters calculated values to ensure safe operation over desired operating temperature range.



Safe Operation Area of DMT6007LFGQ, N-CHANNEL ENHANCEMENT MODE MOSFET

Application Information (continued)

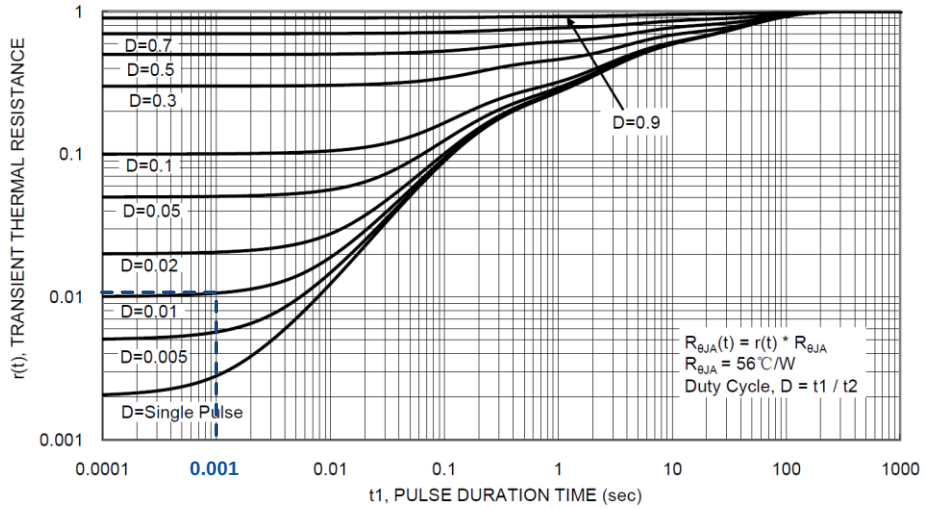
As external MOSFET dissipates ISO7637-2 pulse 1 energy, a special attention should be given while calculating maximum power dissipation and effective temperature rise. An average power dissipation across the MOSFET can be calculated by following equation:

$$P_{D\_AVG} = V_{DSCLAMP\_MAX} \times I_{ISO\_AVG}$$

For given design example, average power dissipation comes around.

$$P_{D\_AVG} = 43V \times 2.4A = 103.2W$$

Typical ISO7637-2 pulse 1 transient lasts for 2ms with total time period of 200ms between two consecutive pulses (duty cycle of 1%). The effective temperature rise due to power dissipation across MOSFET during ISO7637-2 pulse 1 event can be calculated by looking at transient thermal impedance curve in a MOSFET datasheet. The following curve shows an example of how to estimate transient thermal impedance of a MOSFET for ISO7637-2 pulse 1 event.



Transient Thermal Resistance of DMT6007LFGQ, N-CHANNEL ENHANCEMENT MODE MOSFET

The maximum V_{GS} AP74701Q can drive is 13.9V, so a MOSFET with 15V minimum V_{GS} rating should be selected.

Charge Pump C_CP and Input Capacitance CIN

Minimum required capacitance for charge pump VCP and input/output capacitance are:

- C_{VCP}: Minimum 0.1µF is required; recommended value of V_{CP} [µF] ≥ 10 x C_{ISS_MOSFET} [µF]
- C_{IN}: Minimum 0.1µF of input capacitance is required, recommended to place close to ANODE pin

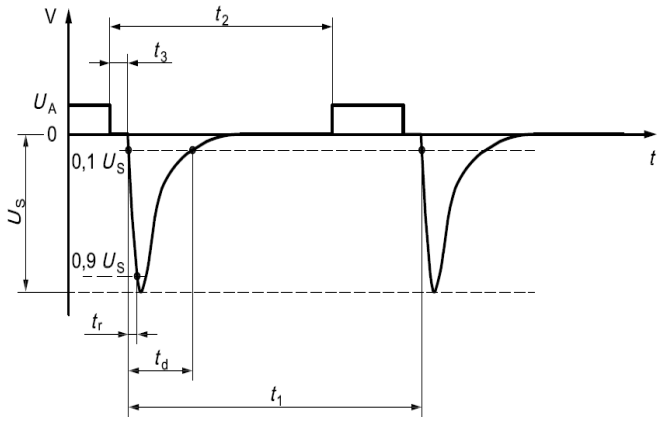
Output Capacitance COUT

The AP74701Q CATHODE pin is capable of handling negative voltage. However, if applications connected to AP74701Q output are not capable of handling negative voltage, then sufficient output capacitor is required to ensure output does not swing negative during ISO7637-2 pulse 1 operation. The required output capacitor during ISO7637-2 pulse 1 to ensure output does not swing negative can be calculated using following equation:

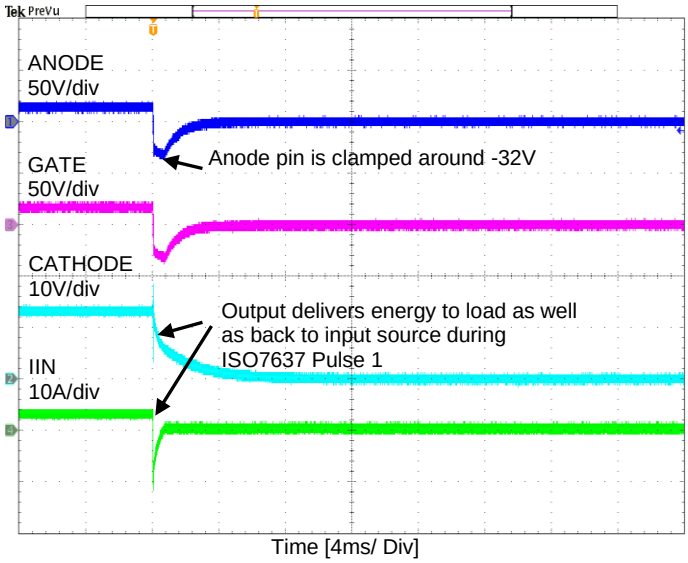
$$C_{OUT} = (I_{LOAD} + I_{ISO\_AVG}) \times 1ms / \Delta V_{OUT} \quad (5)$$

Where ΔV_{OUT} is difference between V_{OUT} at the start and the end of ISO7637-2 pulse 1.

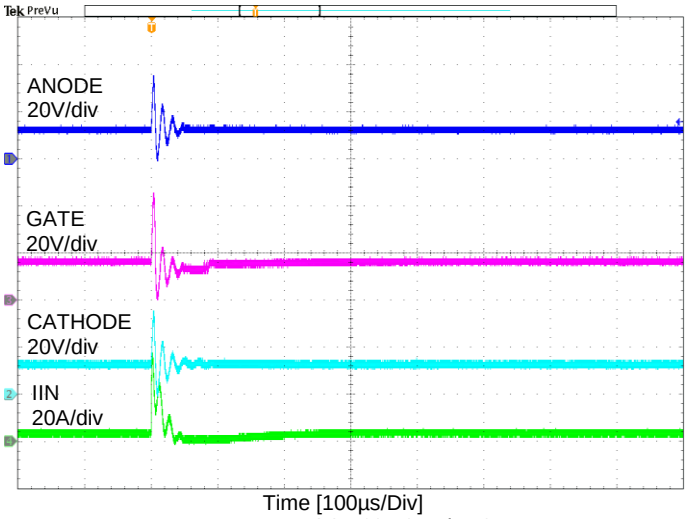
Application Curves



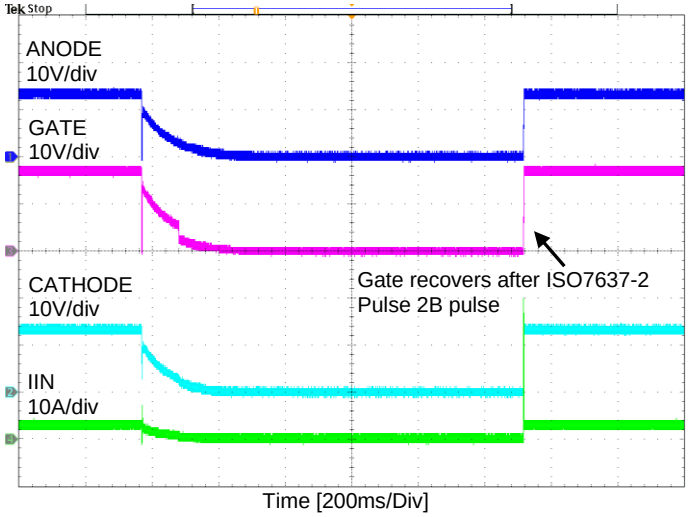
ISO 7637-2 Pulse 1



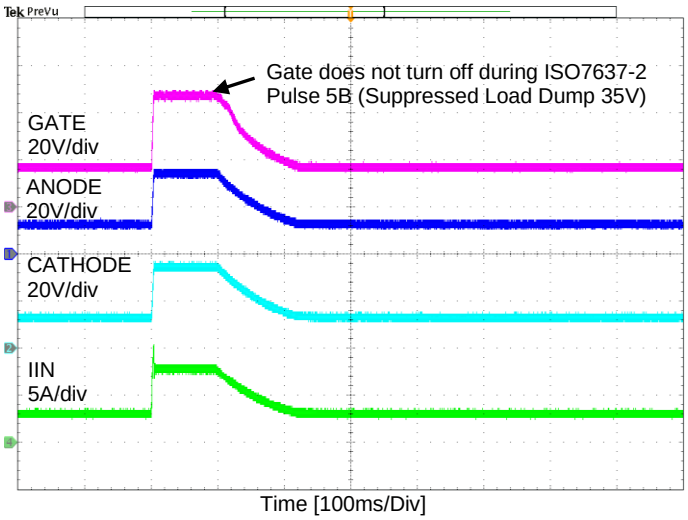
Time [4ms/ Div]
Response to ISO 7637-2 Pulse 1



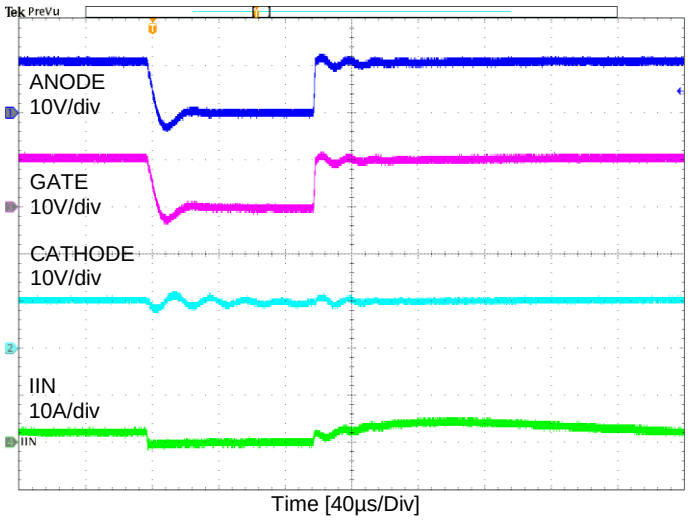
Time [100µs/Div]
Response to ISO 7637-2 Pulse 2A



Time [200ms/Div]
Response to ISO 7637-2 Pulse 2B

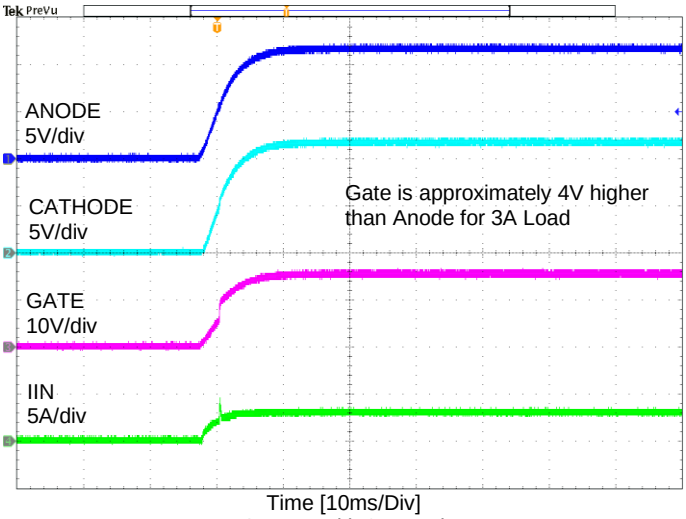


Time [100ms/Div]
Response to ISO 16750-2 Pulse 5B

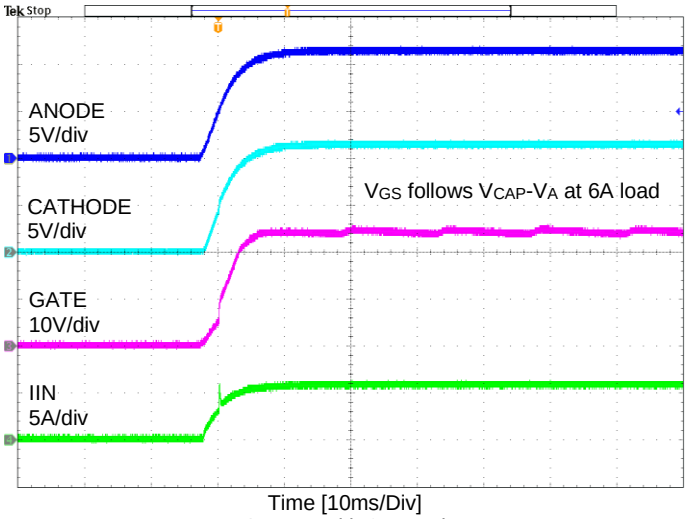


Time [40µs/Div]
Response to LV124 E10, Input micro short for 100µs

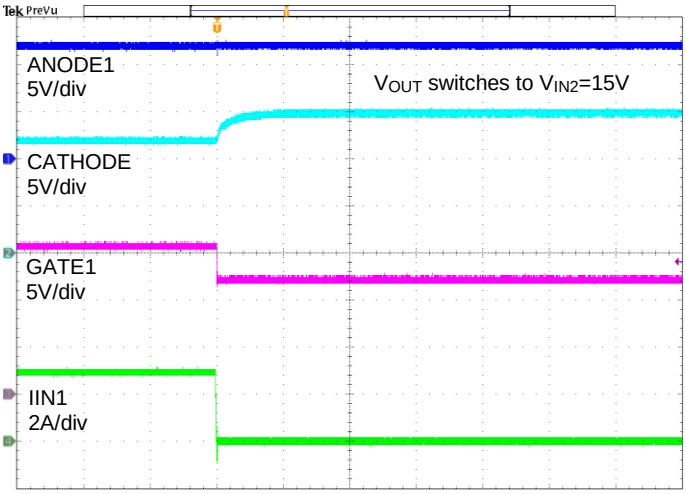
Application Curves (continued)



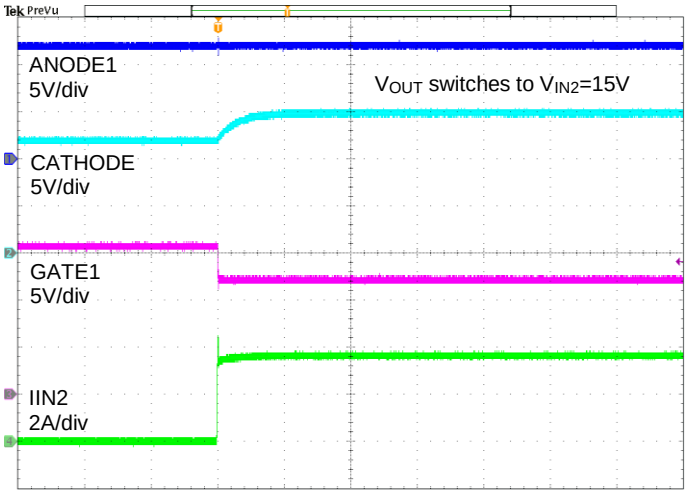
Time [10ms/Div]
Startup With 3A Load



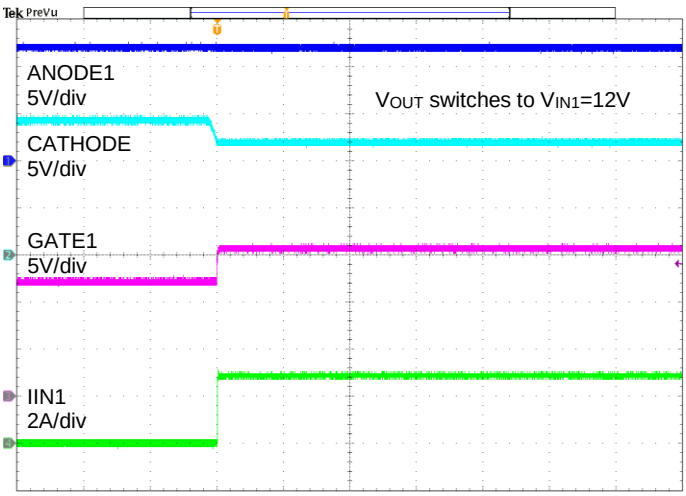
Time [10ms/Div]
Startup With 6A Load



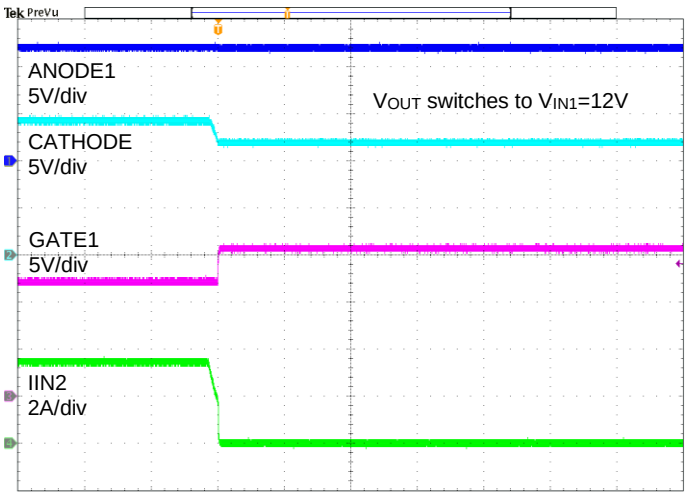
Time [10ms/Div]
ORing VIN1 to VIN2 Switch Over



Time [10ms/Div]
ORing VIN1 to VIN2 Switch Over

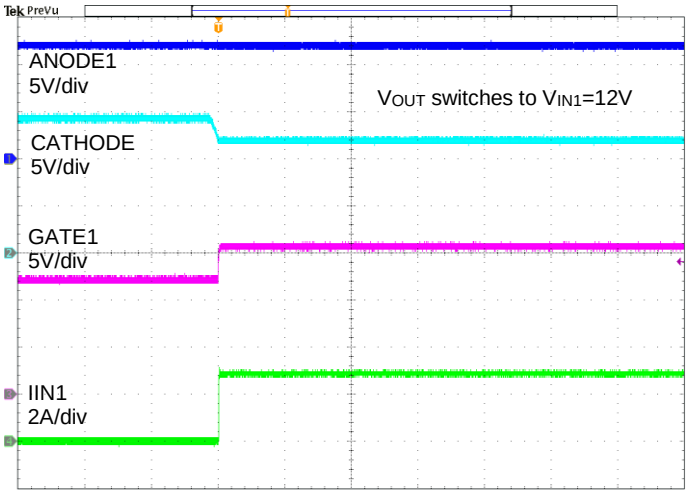


Time [10ms/Div]
ORing VIN2 to VIN1 Switch Over

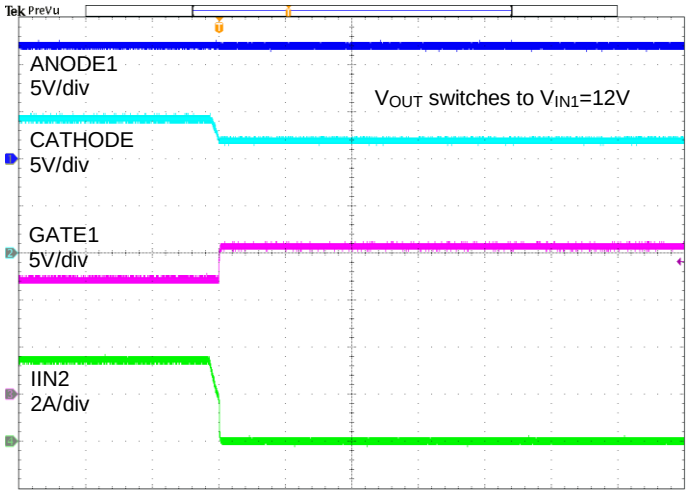


Time [10ms/Div]
ORing VIN2 to VIN1 Switch Over

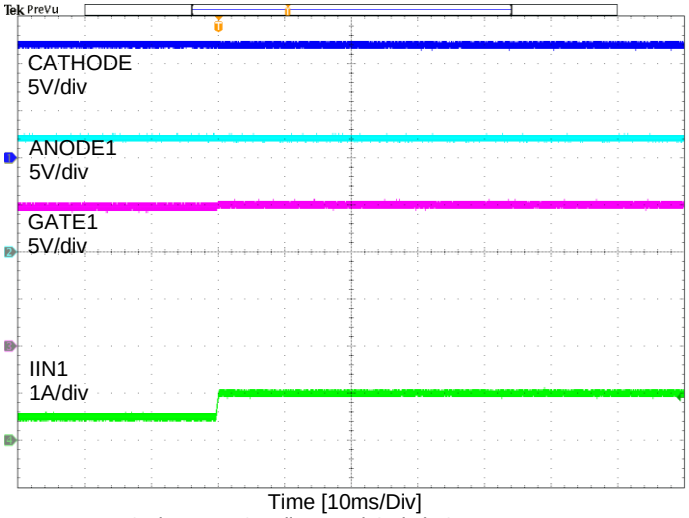
Application Curves (continued)



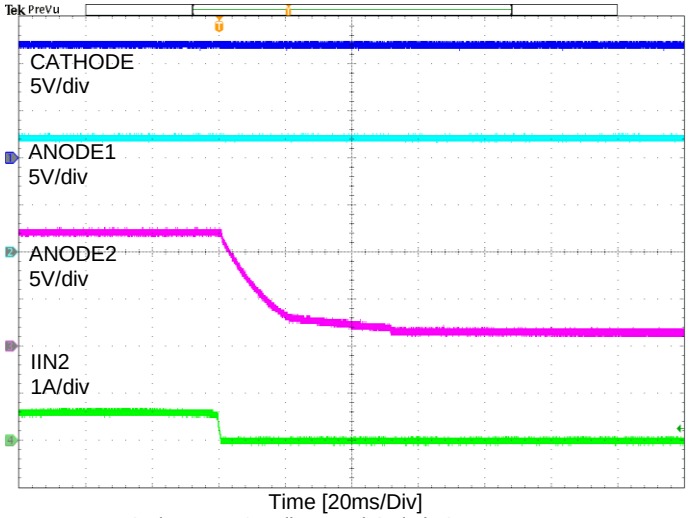
Time [10ms/Div]
ORing VIN2 to VIN1 Switch Over



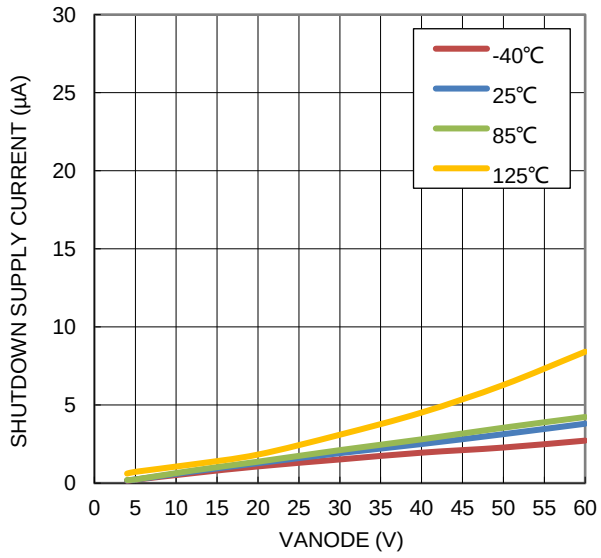
Time [10ms/Div]
ORing VIN2 to VIN1 Switch Over



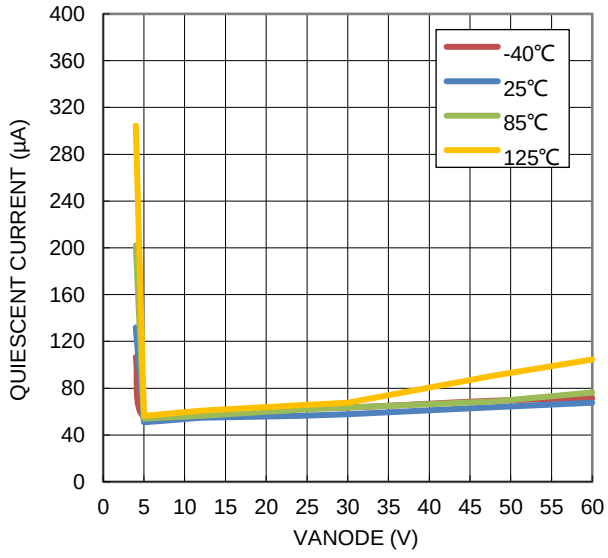
Time [10ms/Div]
ORing - VIN2 Failure and Switch Over to VIN1



Time [20ms/Div]
ORing - VIN2 Failure and Switch Over to VIN1

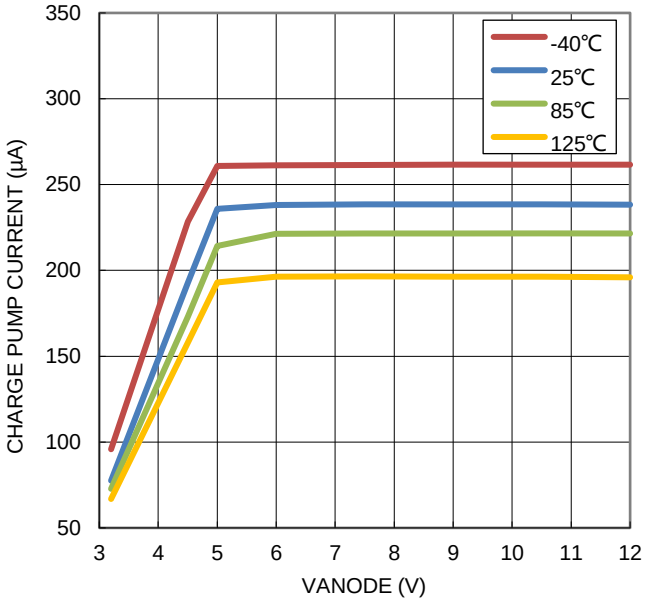


Shutdown Supply Current vs. Supply Voltage

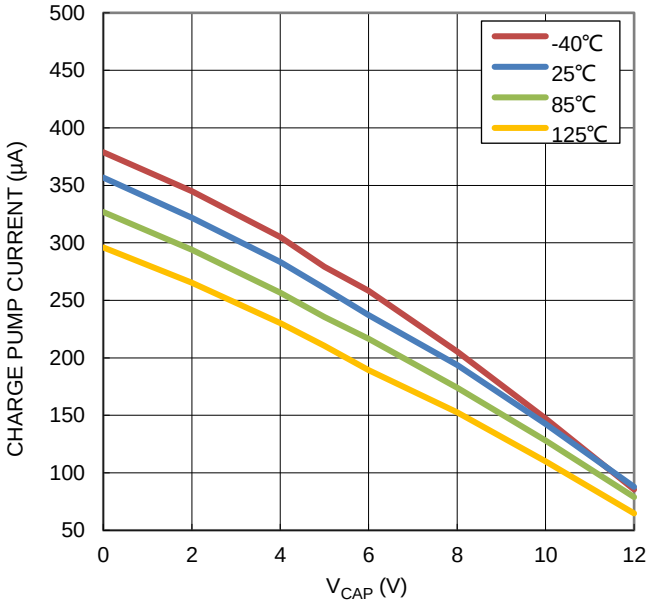


Operating Quiescent Current vs. Supply Voltage

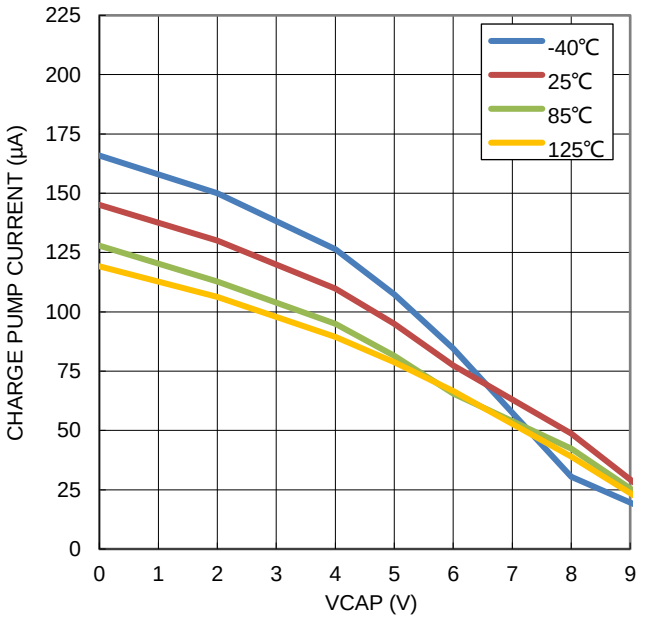
Application Curves (continued)



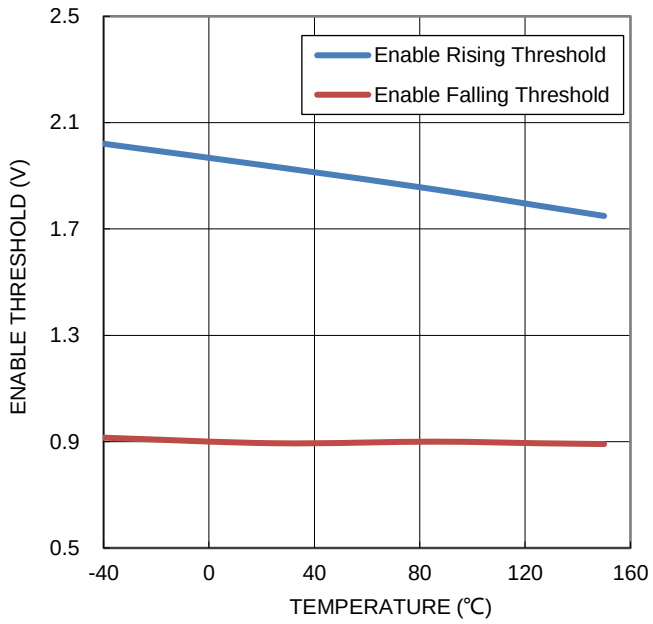
Charge Pump Current vs. Supply Voltage at VCAP = 6V



Charge Pump V-I Characteristics at VANODE > = 12V

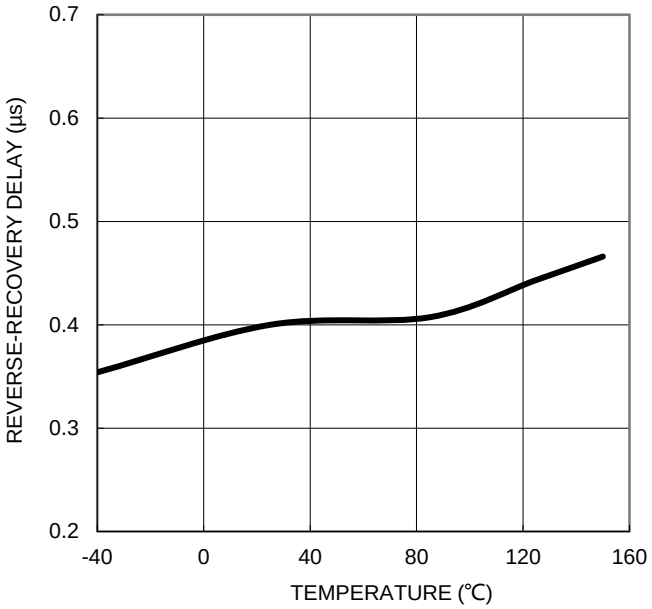


Charge Pump V-I Characteristics at VANODE = 3.2V

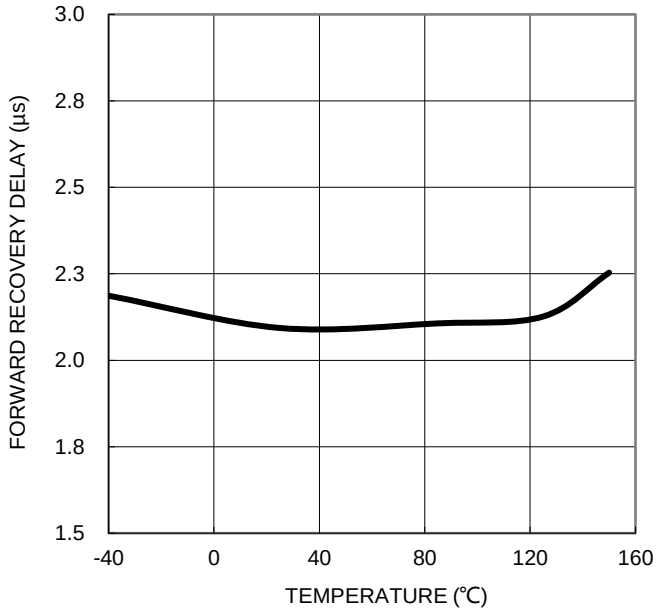


Enable Threshold vs. Temperature

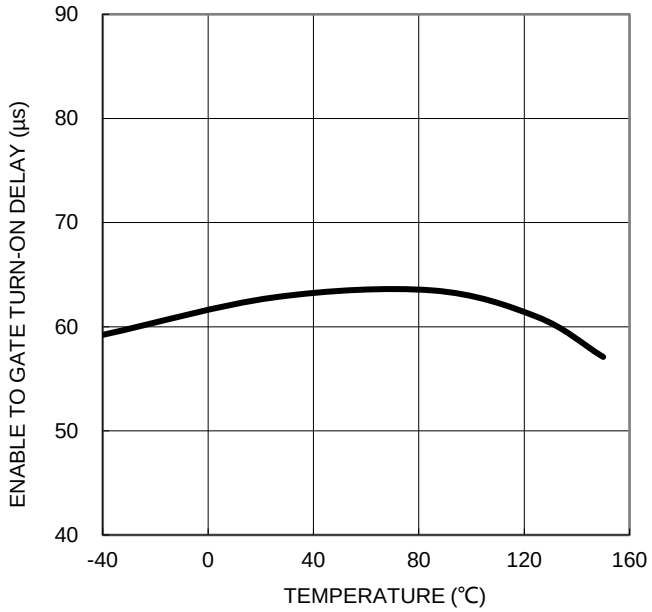
Application Curves (continued)



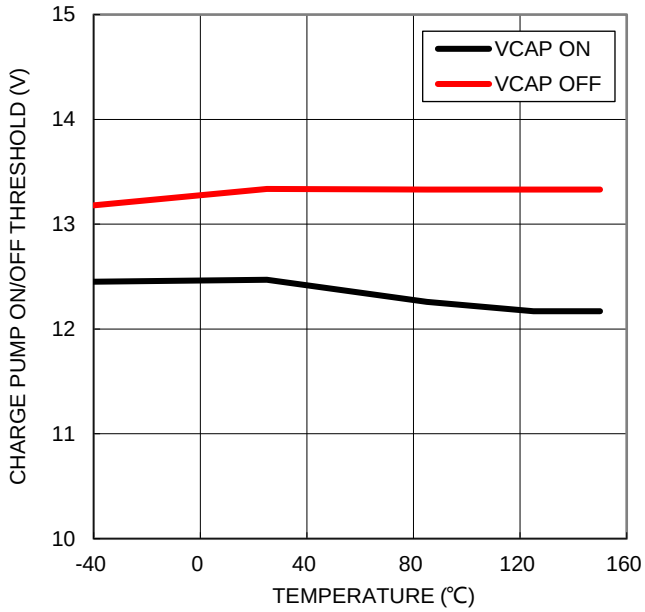
Reverse Current Blocking Delay vs. Temperature



Forward Recovery Delay vs. Temperature

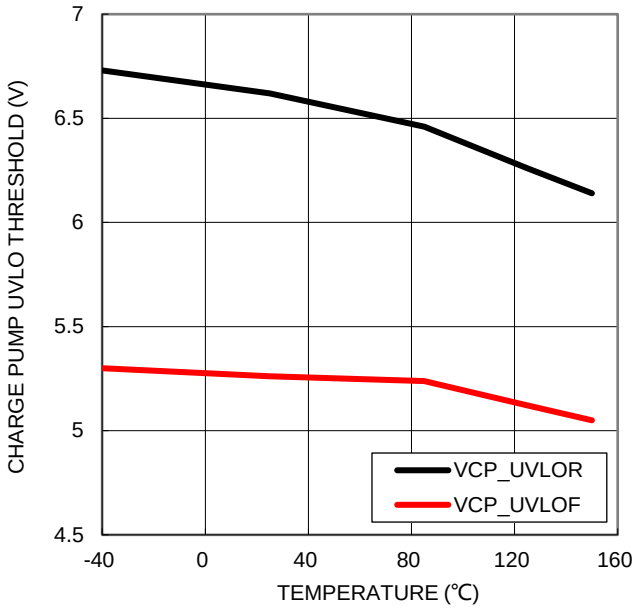


Enable to Gate Delay vs. Temperature

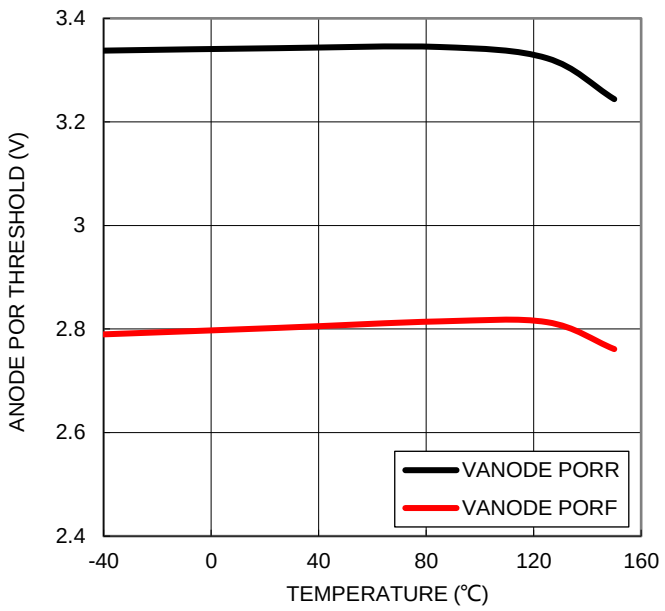


Charge Pump ON and OFF Threshold vs. Temperature

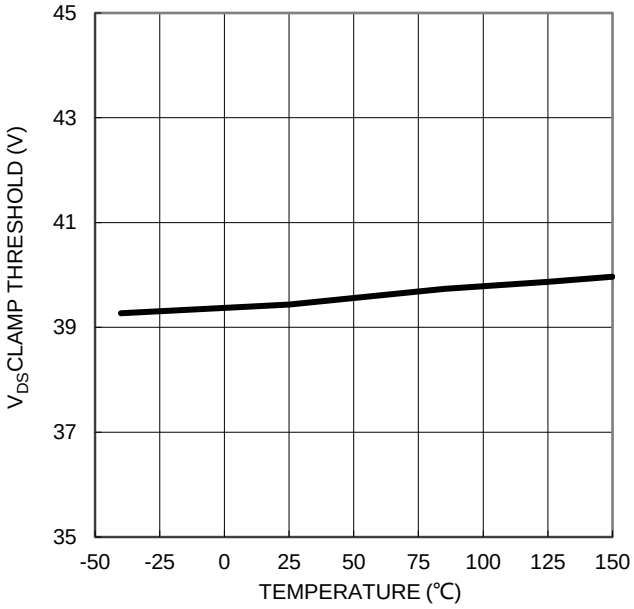
Application Curves (continued)



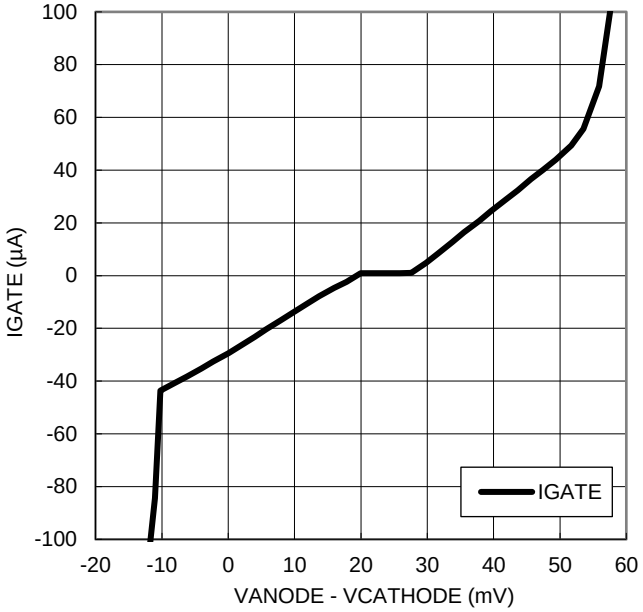
Charge Pump UVLO Threshold vs. Temperature



V_{ANODE} POR Threshold vs. Temperature

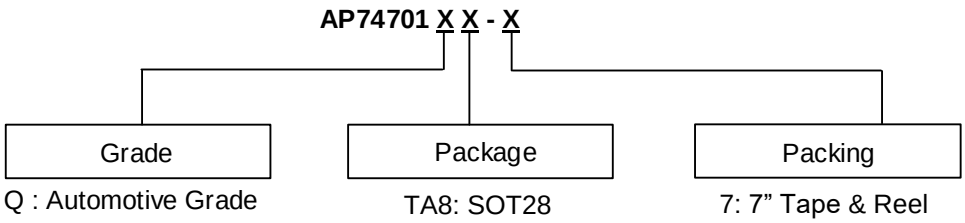


V_{DS}CLAMP Threshold vs. Temperature



Gate Current vs. Forward Voltage Drop

Ordering Information

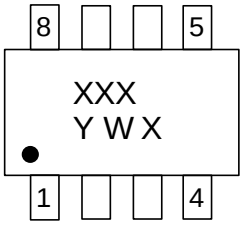


Orderable Part Number	Enable Active	Package Code	Package	Packing	
				Qty.	Carrier
AP74701QTA8-7	High	TA8	SOT28	3000	7" Tape and Reel

Marking Information

SOT28

(Top View)



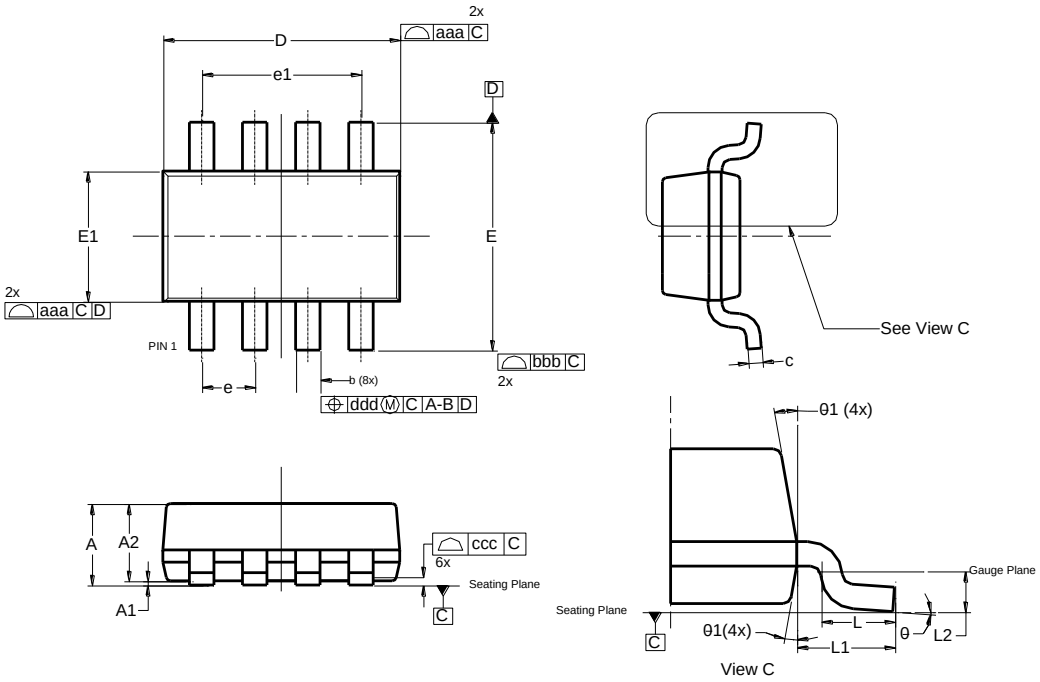
XXX : Identification Code
Y : Year 0 to 9
W : Week : A to Z : 1 to 26 week;
a to z : 27 to 52 week; z represents 52 and 53 week
X : Internal Code

Orderable Part Number	Package	Identification Code
AP74701QTA8-7	SOT28	T9Q

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT28

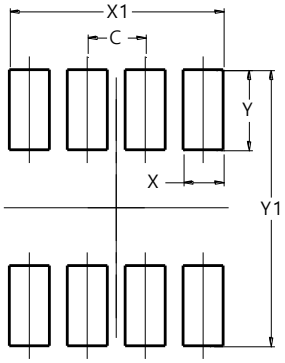


SOT28			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.10	--
A2	--	--	0.95
b	0.20	0.40	0.30
c	0.08	0.20	--
D	2.85	2.95	2.90
E	2.65	2.95	2.80
E1	1.55	1.65	1.60
e	0.65 BSC		
e1	1.95 BSC		
L	0.30	0.60	0.45
L1	0.60 REF		
L2	0.25 BSC		
θ	0°	8°	--
θ1	9°	11°	10°
aaa	0.15		
bbb	0.25		
ccc	0.10		
ddd	0.20		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT28



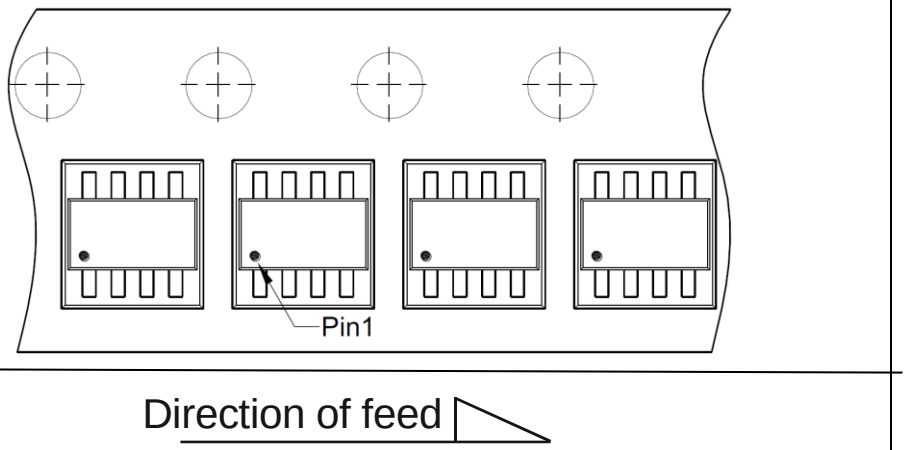
Dimensions	Value (in mm)
C	0.950
G	1.600
X	0.700
Y	0.900
Y1	3.400

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These dimensions may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the 'Z' dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for International grid details, please see document IEC, Publication 97.

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

Device Taping Orientation

Package Type: SOT28

Tape Width	Part Number Suffix	Tape Orientation
8mm	-7	

Note: For part marking, refer to *Marking Information*.
Note: Tape and package drawings are not to scale and are shown for device tape orientation only.
Note: The taping orientation of the other package type can be found on our website at https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf.

Mechanical Data

- Surface-Mount Package
- Moisture Sensitivity: Level 1 per J-STD-020
- Package Material: Molded Plastic, UL Flammability Classification Rating 94V-0
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.016 grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

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