

Description

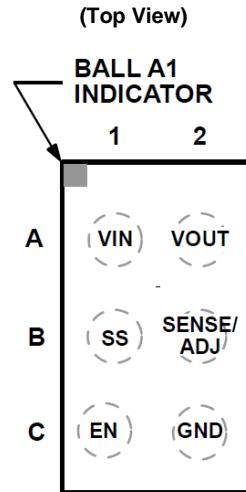
The AP7372 is a low-dropout linear regulator that operates from 2.7V to 20V and delivers 200mA output current. The wide input voltage LDO is suitable for the regulation of high-performance analog and mixed-signal circuits operating from 19.5V to 1.2V rails.

The AP7372 features high power supply rejection, low noise, and achieves excellent line and load transient response with a small 2.2 μ F ceramic output capacitor. The output noise is 8 μ Vrms, independent of the output voltage for the fixed options of 5V or less.

The AP7372 has 1.8V, 2.5V, 3.3V and 5.0V fixed output voltage. Each fixed output voltage can be adjusted above the initial set point with an external feedback divider. This allows the AP7372 to provide an output voltage from 1.2V to VIN – VDO with high PSRR and low noise.

A programmable soft-start with an external capacitor is available in the AP7372. The AP7372 is available in U-WLB1012-6 (Type A1) package.

Pin Assignments



U-WLB1012-6 (Type A1)

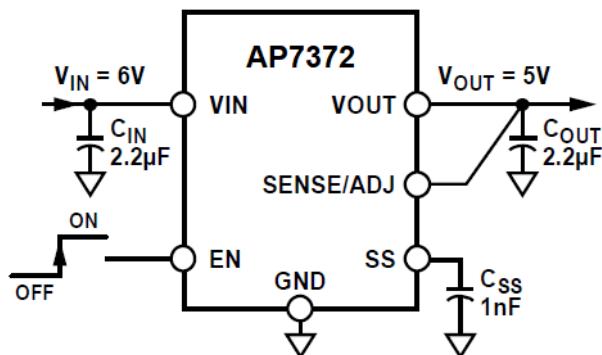
Features

- Low noise: 8 μ Vrms independent of fixed output voltage
- High PSRR: 90dB @ 10kHz, 70dB @ 100kHz, 52dB @ 1MHz
- Input voltage range: 2.7V to 20V
- Maximum output current: 200mA
- High output voltage accuracy: $\pm 0.8\%$
- Accuracy over line, load, and temperature $\pm 1.8\%$, $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
- Low dropout voltage: 120mV @ $I_{\text{OUT}} = 200\text{mA}$ (typ)
- User-programmable soft-start
- Low quiescent current, $I_{\text{GND}} = 66\mu\text{A}$ (typ)
- Low shutdown current:
 - 3.1 μA @ $V_{\text{IN}} = 5\text{V}$
 - 3.3 μA @ $V_{\text{IN}} = 20\text{V}$
- Stable with a 2.2 μF ceramic output capacitor
- Adjustable output from 1.2V to VIN – VDO, output can be adjusted above initial set point
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.**

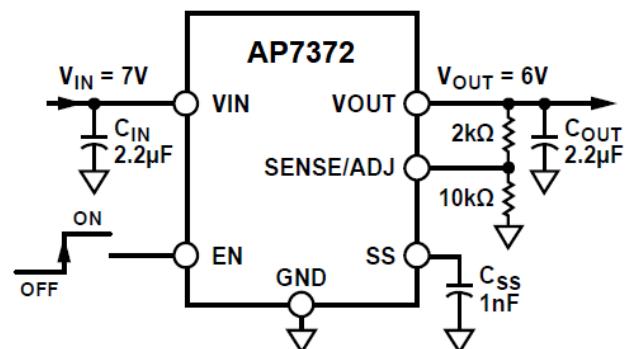
<https://www.diodes.com/quality/product-definitions/>

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



AP7372 with Fixed Output Voltage, 5V

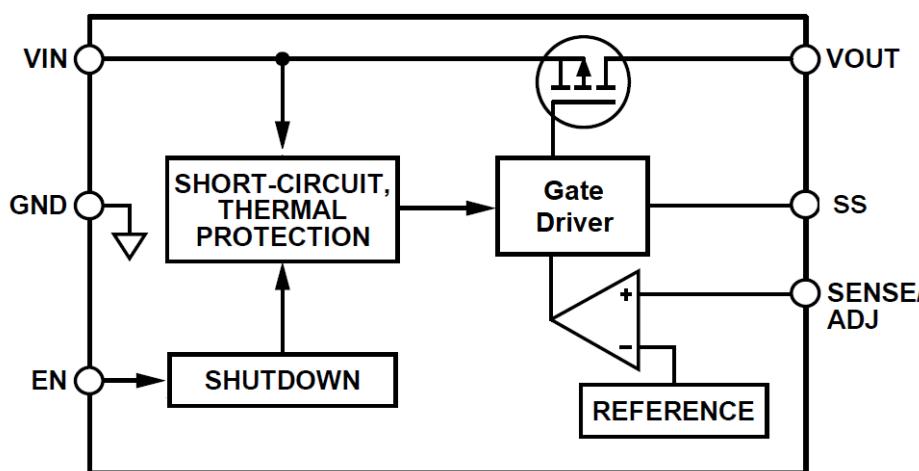


AP7372 with 5V Output Adjusted to 6V

Pin Descriptions

Pin Number	Pin Name	Function
A1	VIN	Input voltage
B1	SS	Soft-start. An external capacitor connected to this pin determines the soft-start time. Leave this pin open for a typical 340µs startup time. Do not ground this pin.
C1	EN	The enable pin controls the operation of the LDO. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
A2	VOUT	Regulated output voltage
B2	SENSE/ADJ	Sense input (SENSE). Connect to load. Adjustable model (ADJ). The adjustable model has a fixed output set to 1.2V. The output can be set to a voltage higher than 1.2V by connecting an external resistor divider to the ADJ pin.
C2	GND	Ground

Functional Block Diagram



Absolute Maximum Ratings (Note 4) (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Input Voltage	-0.3 to 24	V
V_{OUT}	Regulated Output Voltage	-0.3 to V_{IN}	V
V_{EN}	Enable Pin Voltage	-0.3 to 26	V
$V_{SENSE/ADJ}$	Sense and Adjustable Voltage	-0.3 to 6	V
V_{SS}	Soft-Start Voltage	-0.3V to V_{IN} or +6V (whichever is less)	V
I_{OUT}	Output Current	Internally limited	mA
T_{LEAD}	Lead Temperature (Soldering, 10sec)	+260	°C
T_J	Operating Junction Temperature	+150	°C
T_A	Operating Ambient Temperature	-40 to +85	°C
θ_{JA}	Thermal Resistance Junction to Air	163.76	°C/W
θ_{JC}	Thermal Resistance Junction to Case	46.8	°C/W
T_{STG}	Storage Temperature Range	-40 to +150	°C
HBM	ESD (Human Body Model)	2000	V
CDM	ESD (Change Device Model)	1000	V

Note: 4. a). Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
 b). Ratings apply to ambient temperature at $+25^\circ\text{C}$. The JEDEC STD.51 High-K board design used to derive this data was a 3inch x 3inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Input Voltage	2.7	20	V
V_{EN}	Enable Pin Voltage	0	20	V
V_{OUT}	Supply Output Voltage	1.2	$V_{IN} - V_{DO}$	V
I_{OUT}	Output Current	0	200	mA
T_J	Operating Junction Temperature	-40	+125	°C

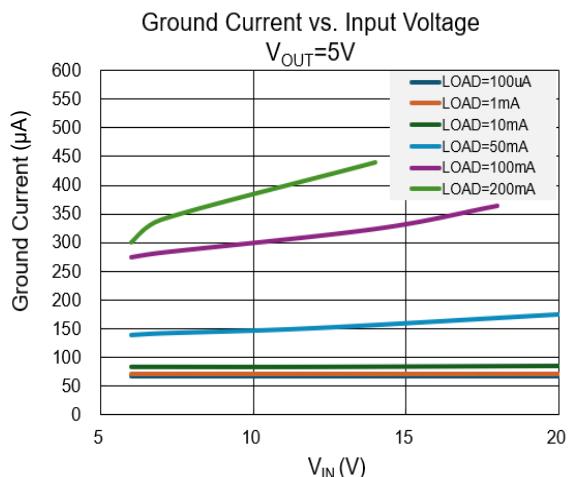
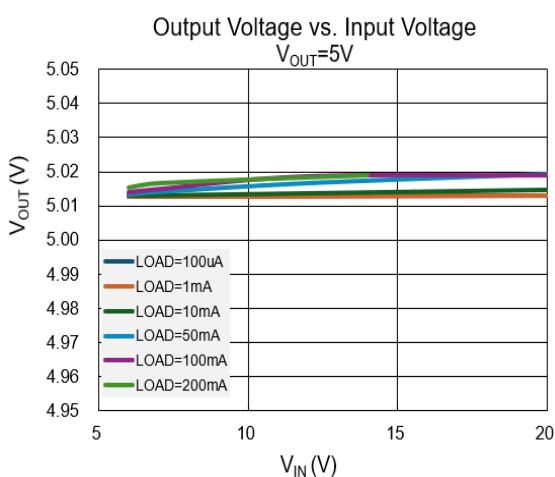
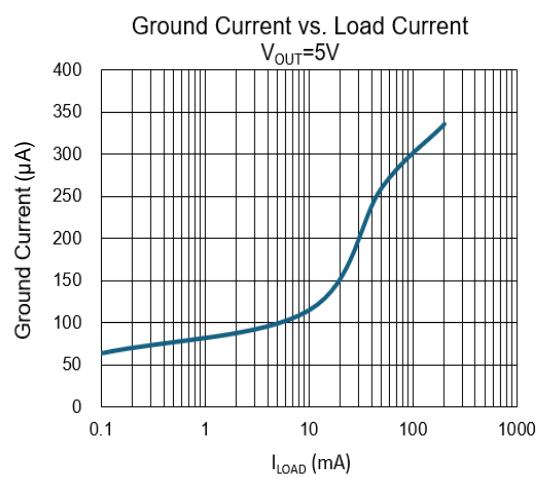
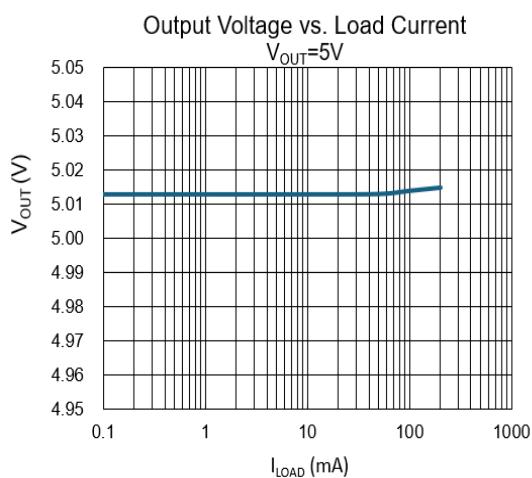
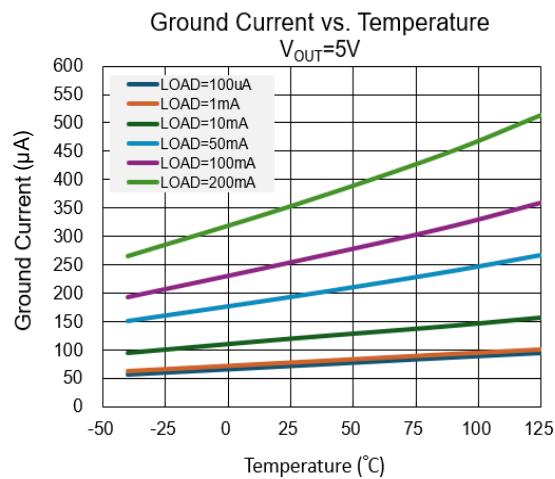
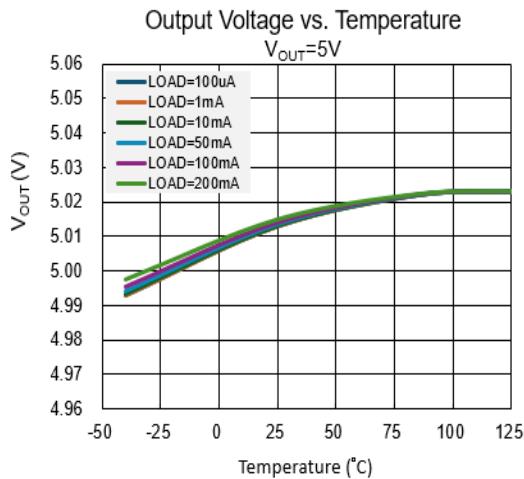
Electrical Characteristics

$V_{IN} = V_{OUT} + 1V$ or $2.7V$, whichever is greater, $V_{OUT} = 5V$, $EN = V_{IN}$, $I_{OUT} = 10mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{SS} = 0pF$, $T_A = +25^\circ C$ for typical specifications, $T_J = -40^\circ C$ to $+125^\circ C$ for minimum/maximum specifications, unless otherwise noted.

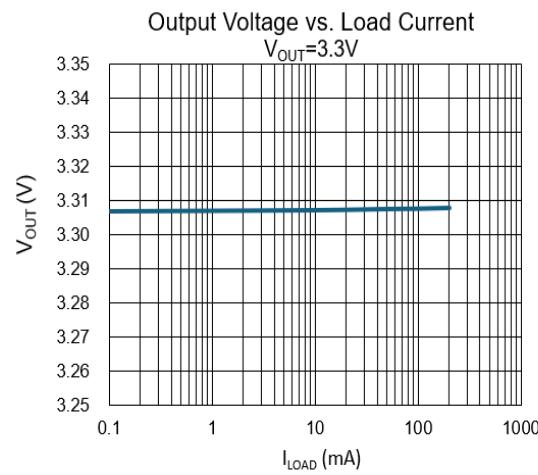
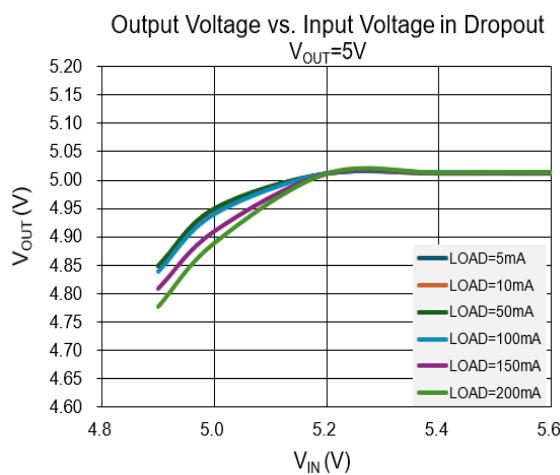
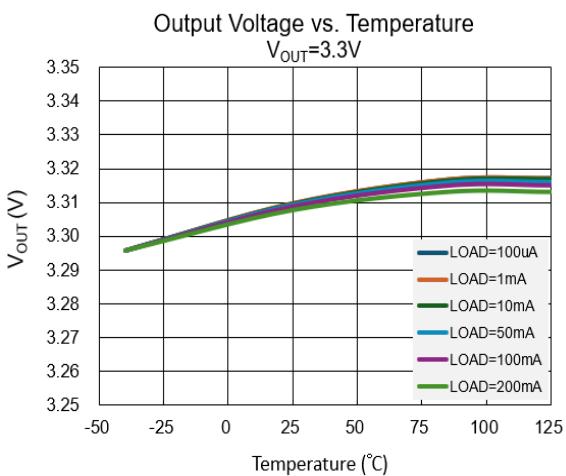
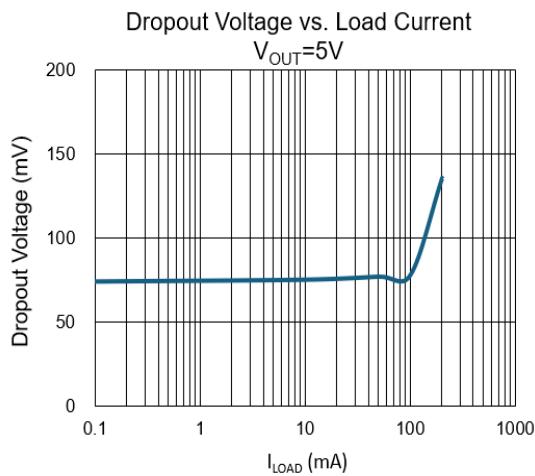
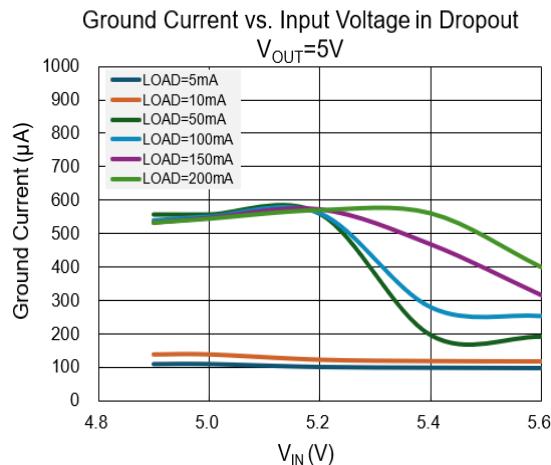
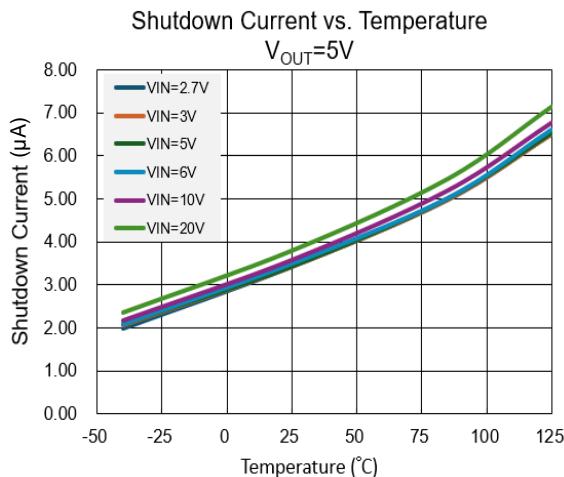
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	—	2.7	—	20	V
I_{LOAD_MAX}	Maximum Output Current	—	—	200	—	mA
I_{GND}	Ground Current	$I_{OUT} = 0\mu A$	—	66	110	μA
		$I_{OUT} = 10mA$	—	110	185	μA
		$I_{OUT} = 200mA$	—	280	500	μA
I_{SHDN}	Shutdown Current	$EN = GND$	—	3.1	—	μA
		$EN = GND, V_{IN} = 20V$	—	3.5	11	μA
V_{OUT}	Output Voltage Accuracy	$I_{OUT} = 10mA, T_J = +25^\circ C$	-0.8	—	0.8	%
		$100\mu A < I_{OUT} < 200mA, V_{IN} = (V_{OUT} + 1V) \text{ to } 20V$	-1.8	—	1.8	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$V_{IN} = (V_{OUT} + 1V) \text{ to } 20V$	-0.01	—	0.01	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	$I_{OUT} = 100\mu A \text{ to } 200mA$	—	0.001	0.003	%/mA
$SENSE_{I-BIAS}$	Sense Input Bias Current	$100\mu A < I_{OUT} < 200mA, V_{IN} = (V_{OUT} + 1V) \text{ to } 20V$	—	10	1000	nA
V_{DO}	Dropout Voltage	$I_{OUT} = 10mA$	—	60	100	mV
		$I_{OUT} = 200mA$	—	120	280	mV
$t_{STARTUP}$	Startup Time	$V_{OUT} = 5V$	—	340	—	μs
$SS_{I-SOURCE}$	Soft-Start Source Current	$SS = GND$	—	1	—	μA
I_{CL}	Output Current Limit	—	245	360	500	mA
T_{SSD}	Thermal Shutdown Threshold	T_J rising	—	+155	—	$^\circ C$
$T_{SSD-HYS}$	Thermal Shutdown Hysteresis		—	+20	—	$^\circ C$
V_{UVLO}	UVLO Threshold	V_{IN} rising	—	—	2.65	V
		V_{IN} falling	2.1	—	—	
		Hysteresis	—	0.24	—	
EN INPUT STANDBY						
$EN_{STBY-HIGH}$	EN Input Logic High	$2.7V \leq V_{IN} \leq 20V$	1.0	—	—	V
$EN_{STBY-LOW}$	EN Input Logic Low		—	—	0.4	V
$EN_{STBY-HYS}$	EN Input Logic Hysteresis		—	0.11	—	V
EN INPUT PRECISION						
EN_{HIGH}	EN Input Logic High	$2.7V \leq V_{IN} \leq 20V$	1.0	1.24	1.45	V
EN_{LOW}	EN Input Logic Low		0.9	1.13	1.3	V
EN_{HYS}	EN Input Logic Hysteresis		—	110	—	mV
I_{EN-LKG}	EN Input Leakage Current	$EN = V_{IN}$ or GND	—	0.01	0.1	μA
t_{EN-DLY}	EN Input Delay Time	From EN rising from $0V$ to V_{IN} to $0.1 \times V_{OUT}$	—	140	—	μs
V_n	Output Noise Voltage	$BW = 10Hz \text{ to } 100kHz$, all output voltage options	—	8	—	μV_{rms}
$PSRR$	Power-Supply Rejection Ratio	$f = 1MHz, V_{IN} = 7V, V_{OUT} = 5V$	—	52	—	dB
		$f = 100kHz, V_{IN} = 7V, V_{OUT} = 5V$	—	70	—	dB
		$f = 10kHz, V_{IN} = 7V, V_{OUT} = 5V$	—	90	—	dB

Performance Characteristics

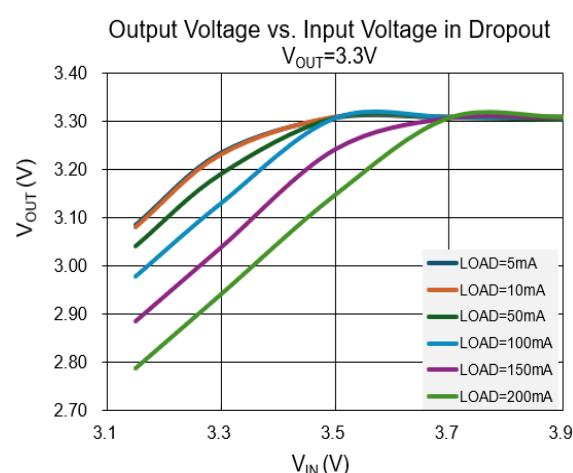
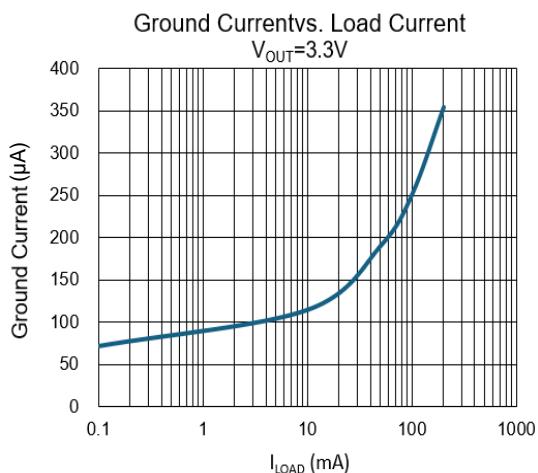
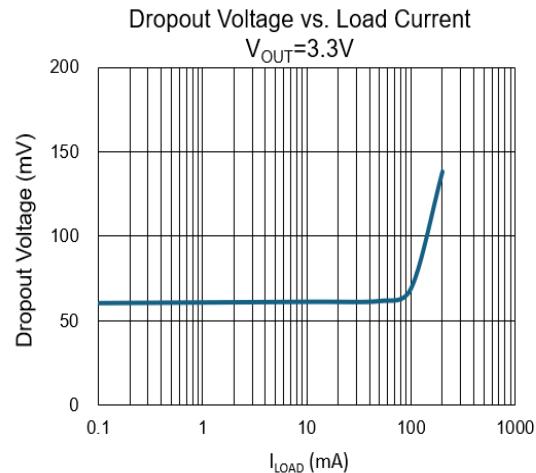
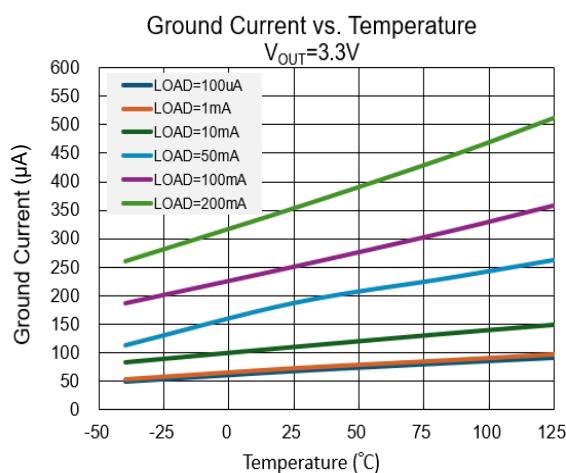
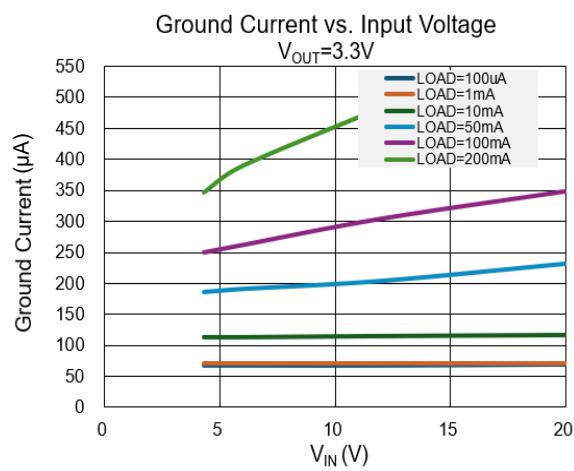
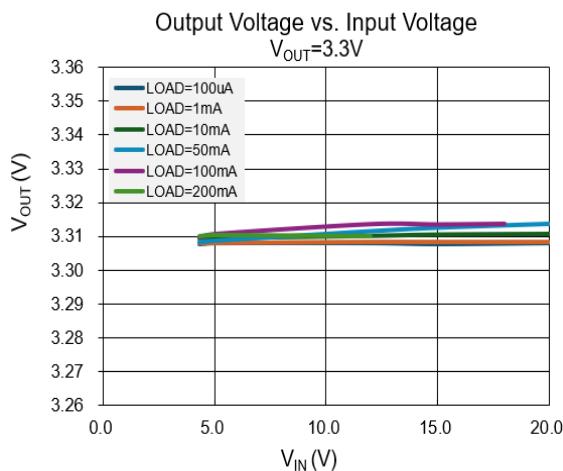
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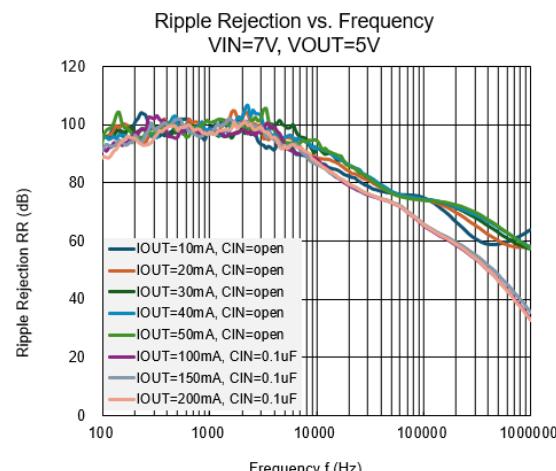
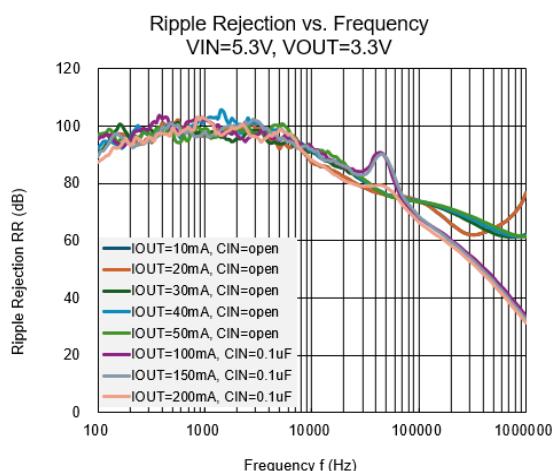
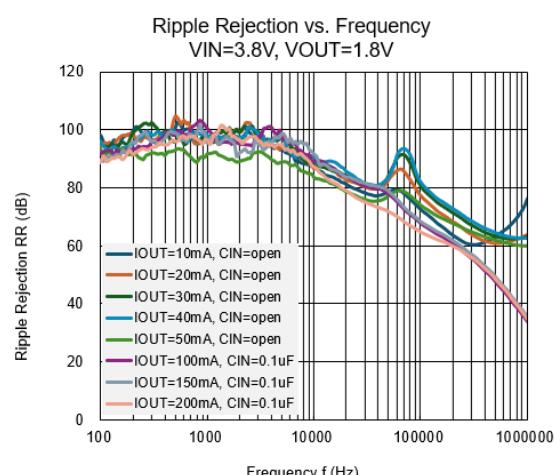
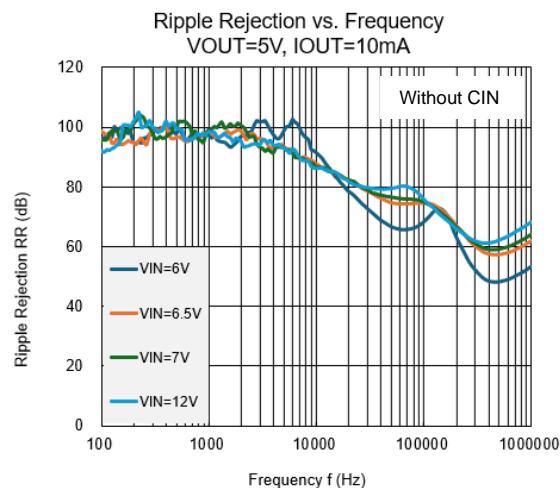
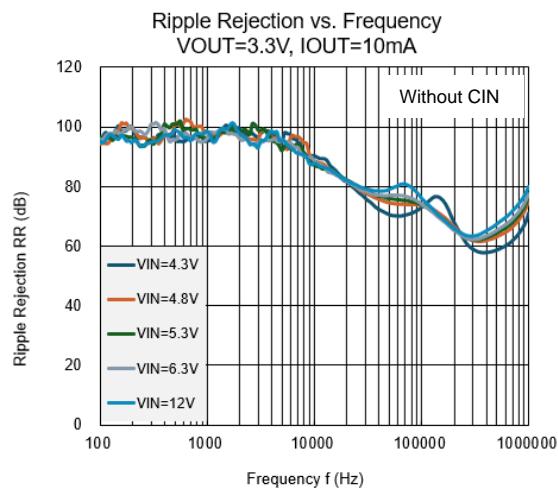
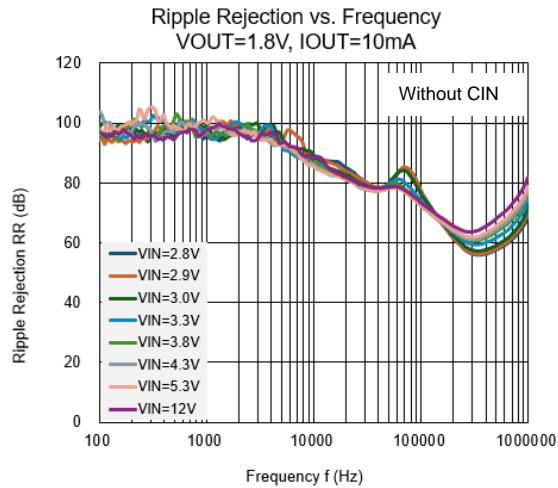
Performance Characteristics (continued)



Performance Characteristics (continued)

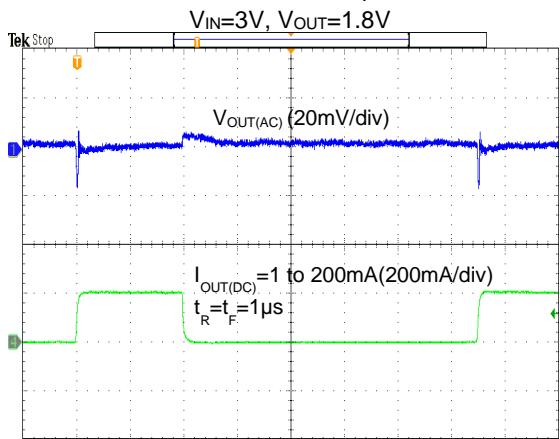


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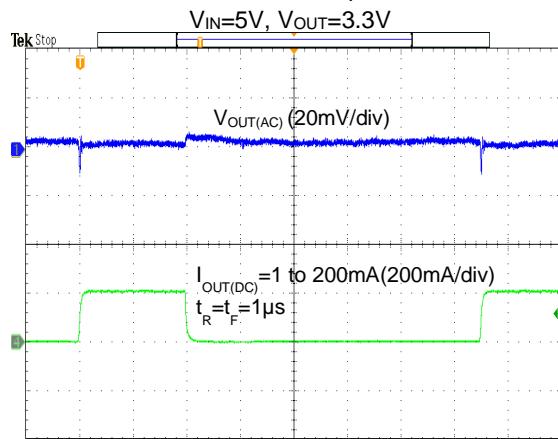


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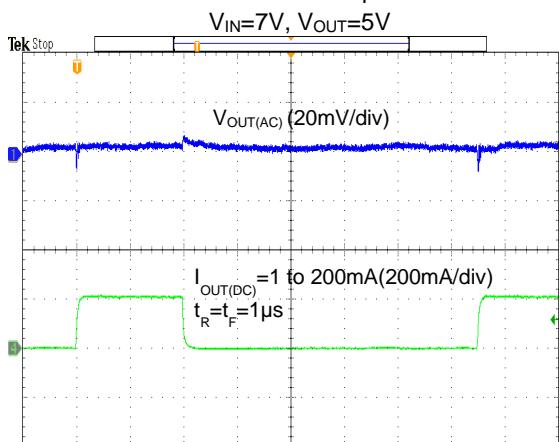
Load Transient Response



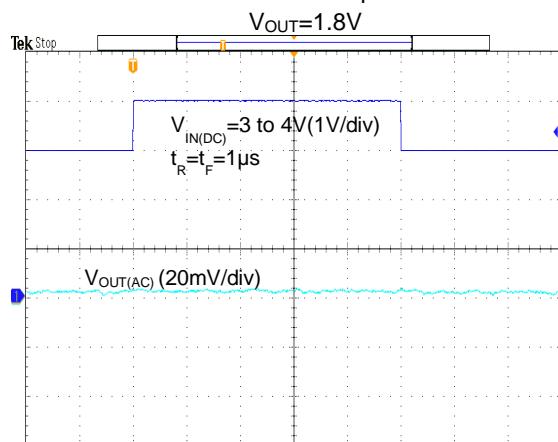
Load Transient Response



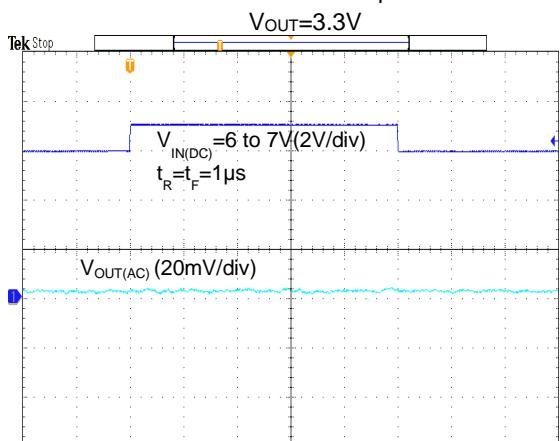
Load Transient Response



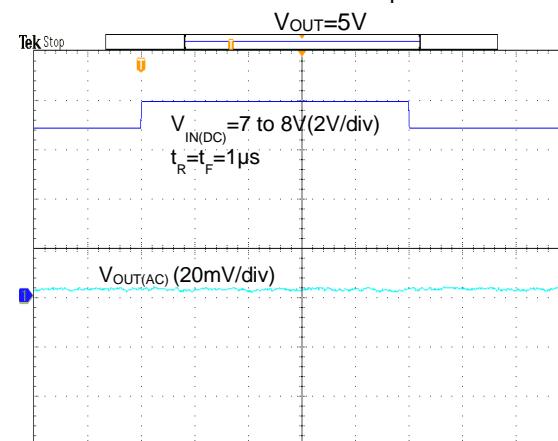
Line Transient Response



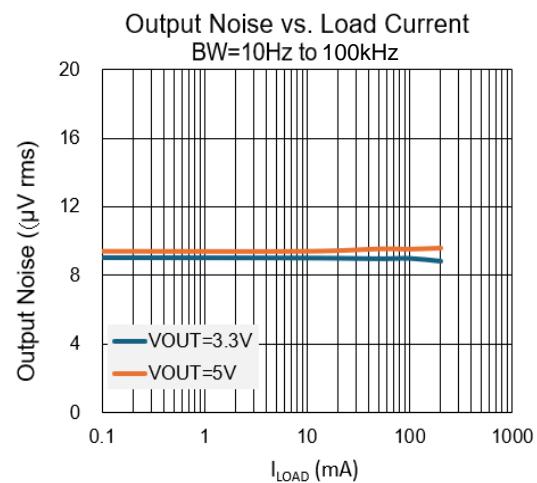
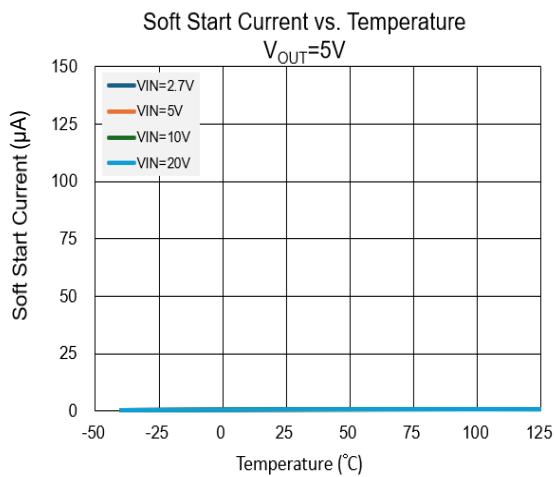
Line Transient Response



Line Transient Response



Performance Characteristics (continued)



Application Information

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is $2.2\mu\text{F}$. A ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place the output capacitor as close as possible to VOUT and GND pins.

Input Capacitor

A $2.2\mu\text{F}$ ceramic capacitor is recommended to connect VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to ensure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Current-Limit and Short-Circuit Protection

When output current at VOUT pin is higher than the current-limit threshold or the VOUT pin directly shorts to GND, current-limit protection will be triggered and clamp the output current at a pre-designed level to prevent overcurrent and thermal damage.

Soft-Start

Soft start the AP7372 uses an internal soft-start (SS pin open) to limit the inrush current when the output is enabled. The startup time for the 5V option is approximately $340\mu\text{s}$ from the time the EN active threshold is crossed to when the output reaches 90% of the final value.

Thermal Protection

The AP7372 has internal thermal sense and protection circuits. When excessive power dissipation happens on the device, such as short circuit at the output pin or very heavy load current with a large voltage drop across the device, the internal thermal protection circuit will be triggered, shutting down the power MOSFET to prevent the LDO from damage. As soon as the excessive thermal condition is removed and the temperature of the device drops down, the thermal protection circuit will release the control of the power MOSFET, and the LDO device returns to normal operation.

Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from VIN to VOUT, and load circuit.

Adjustable Output Voltage

The AP7372 is available in 4 fixed output voltage options, ranging from 1.8V to 5.0V. The AP7372 architecture allows any fixed output voltage to be set to a higher voltage with an external voltage divider. For example, a fixed 5V output can be set to a 6V output according to the following equation: $V_{\text{OUT}} = 5\text{V}(1 + R_1/R_2)$ where R1 and R2 are the resistors in the output voltage divider shown in Figure 1.

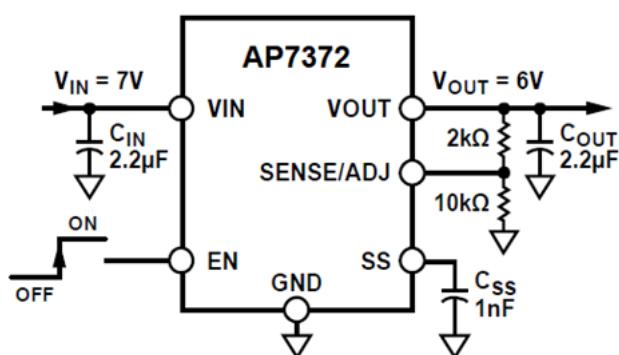
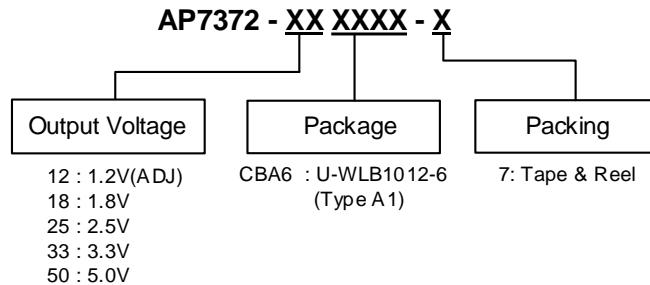


Figure 1. Typical Adjustable Output Voltage Application Schematic

Ordering Information

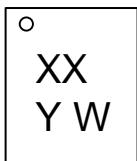


Orderable Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AP7372-XXCBA6-X	CBA6	U-WLB1012-6 (Type A1)	3,000	7" Tape and Reel

Marking Information

U-WLB1012-6 (Type A1)

(Top View)



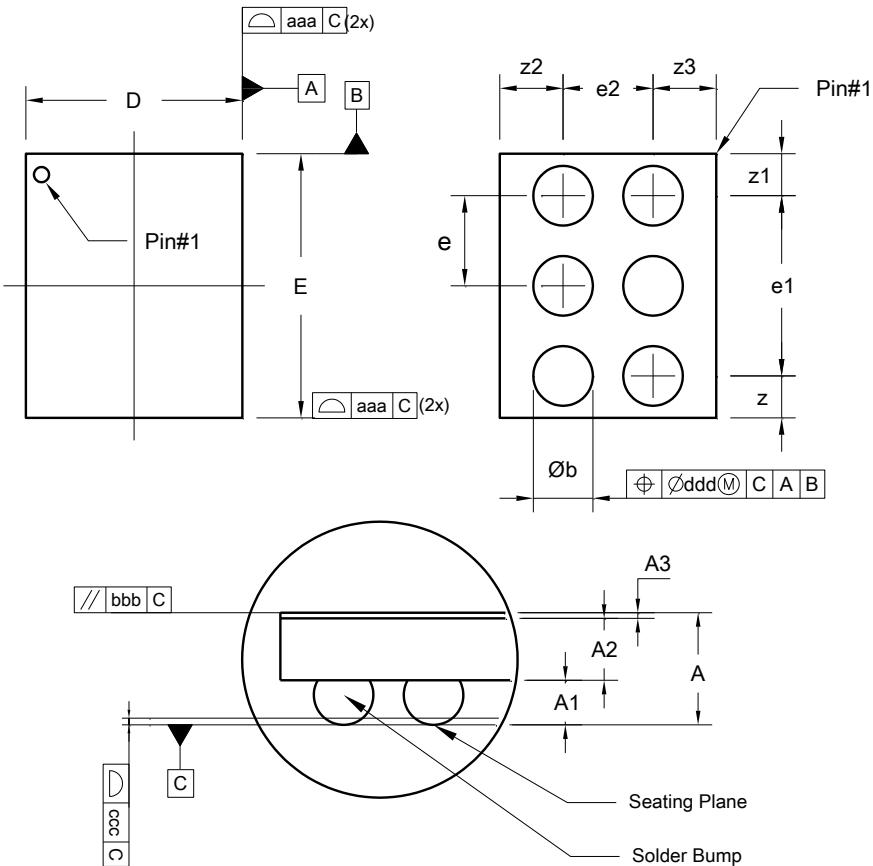
XX : Identification Code
 Y : Year : 0 to 9 (ex: 5 = 2025)
 W : Week : A to Z : week 1 to 26;
 a to z : week 27 to 52; z represents
 week 52 and 53

Orderable Part Number	Package	Identification Code
AP7372-12CBA6-7	U-WLB1012-6 (Type A1)	C2
AP7372-18CBA6-7	U-WLB1012-6 (Type A1)	C3
AP7372-25CBA6-7	U-WLB1012-6 (Type A1)	C4
AP7372-33CBA6-7	U-WLB1012-6 (Type A1)	C5
AP7372-50CBA6-7	U-WLB1012-6 (Type A1)	C6

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-WLB1012-6 (Type A1)



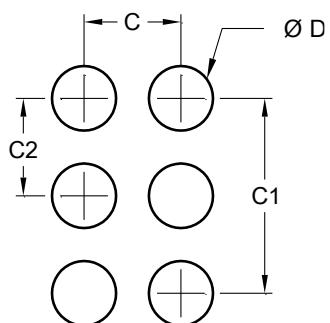
U-WLB1012-6 (Type A1)			
Dim	Min	Max	Typ
A	0.4502	0.5458	0.4980
A1	0.1782	0.2178	0.1980
A2	0.2500	0.3000	0.2750
A3	0.0220	0.0280	0.0250
b	0.2253	0.3048	0.2650
D	0.9350	0.9900	0.9625
E	1.1450	1.200	1.1725
e	--	--	0.4000
e1	--	--	0.8000
e2	--	--	0.4000
z	--	--	0.1863
z1	--	--	0.1863
z2	--	--	0.2813
z3	--	--	0.2813
aaa	--	--	0.0275
bbb	--	--	0.0600
ccc	--	--	0.0300
ddd	--	--	0.1500

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-WLB1012-6 (Type A1)



Dimensions	Value (in mm)
C	0.400
C1	0.800
C2	0.400
D	0.316

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - NiPdAu over Copper Leads, Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0012 grams (Approximate)

IMPORTANT NOTICE

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