A17802

Functional Safety Engineered

Advanced Inductive Position Sensor IC with Sine/Cosine Output

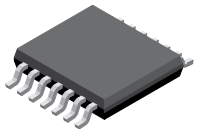
FEATURES AND BENEFITS

- Measures angle with <0.5°elec accuracy at speeds up to 250k eRPM
- Front-end gain automatic optimization at each power-up
- Dynamic autocalibration for continuous error reduction
- Harmonic compensation for enhanced linearization with simpler coil design
- Synchronization compensation perfects commutation timing for efficient motor control
- Programmable zero angle enables arbitrary target alignment
- Programmable via SPI or Manchester protocol
- Qualified to AEC-Q100 grade 0
- ASIL-Compliant: ASIL C(D) safety element out of context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual

ISO 26262 ASIL Compliant

PACKAGE

Not to scale



14-pin TSSOP (Single Die, Suffix LE)

DESCRIPTION

The A17802 IC is an advanced inductive position sensor designed to measure the rotational angle of a metallic target and output the information over a differential sine and cosine analog interface. The IC features digital processing that optimizes the inductive front-end and applies compensations that maximize system-level angle accuracy.

The A17802 operates by applying a megahertz oscillating signal onto a transmit coil connected to an LC tank circuit and demodulating the voltage envelopes present on two receiver coils. Typical systems integrate all three coils on a standard printed circuit board (PCB) and mount the rotating target millimeters above. Electromagnetic induction causes the transmit signal to generate eddy currents in the metallic target, and the currents generate a signal onto the receiver coils that is dependent on rotational angle.

The A17802 provides a high-speed absolute-angle sensor that is suitable for advanced synchronous motor control, including automotive electric motor systems.

The A17802 was developed in accordance with ISO 26262 as a hardware safety element out of context with ASIL C capability for use in automotive safety-related systems up to ASIL D when integrated and used in the manner prescribed in the applicable safety manual and this datasheet. The A17802 is automotive qualified to AEC-Q100 Grade 0 and is packaged in a surface-mount lead (Pb) free 14-pin TSSOP.

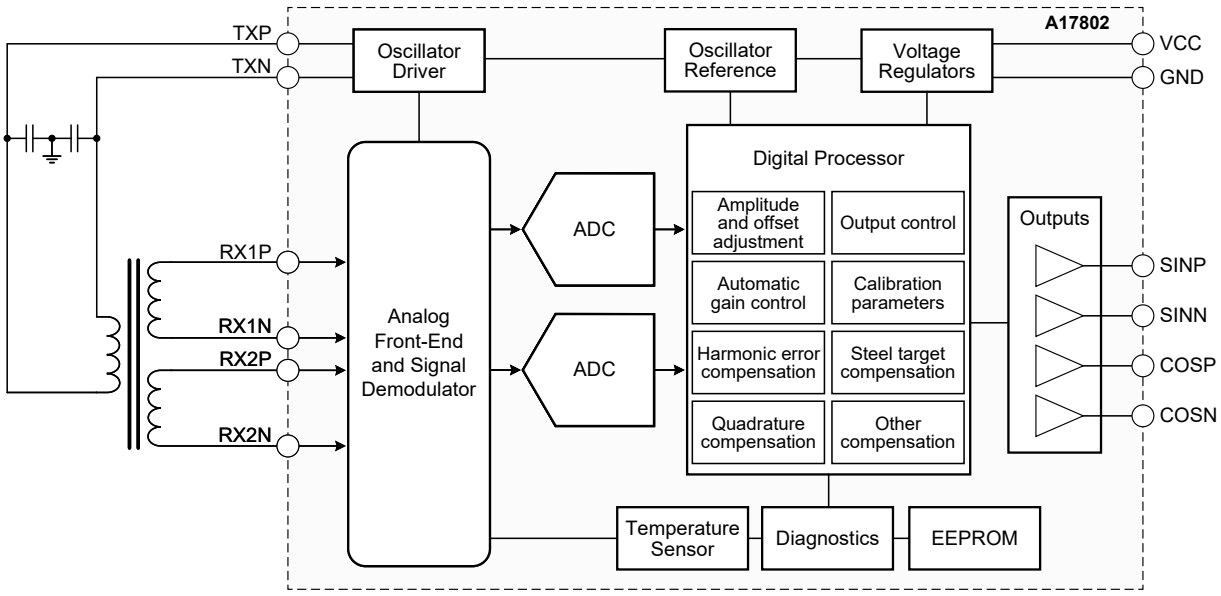


Figure 1: Functional Block Diagram

SELECTION GUIDE

Part Number	Package	Packing
A17802PLEATR	14-pin TSSOP	4000 pieces per 13-in reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Refer to Power Derating section	24	V
Reverse Supply Voltage	V_{RCC}		–18	V
Output Pins Forward Voltage	V_{OUT}	On SINP, SINN, COSP, COSN	14	V
Output Pins Reverse Voltage	V_{ROUT}	On SINP, SINN, COSP, COSN	–14	V
Transmitting Coil Pins Forward Voltage	$V_{IN(TX)}$	On TXP, TXN	4	V
Transmitting Coil Pins Reverse Voltage	$V_{R(TX)}$	On TXP, TXN	–0.5	V
Receiving Coil Pins Forward Voltage	$V_{IN(RX)}$	On RX1N, RX1P, RX2N, RX2P	4	V
Receiving Coil Pins Reverse Voltage	$V_{R(RX)}$	On RX1N, RX1P, RX2N, RX2P	–0.5	V
Operating Ambient Temperature	T_A	P range	–40 to 160	°C
Maximum Junction Temperature	$T_{J(MAX)}$		175	°C
Storage Temperature	T_{STG}		–65 to 170	°C
ESD Rating (VCC, GND, SINP, SINN, COSP, COSN)	V_{ESD}	HBM testing per AEC-Q100	>4	kV
ESD Rating (all other pins)		HBM testing per AEC-Q100	>2	kV

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Operating Characteristics section.

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-14 package on 4-layer PCB based on JEDEC standard JESD51-7	82	°C/W

[1] Additional thermal information available on the Allegro website.

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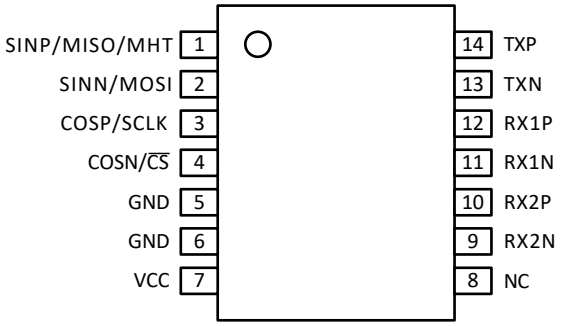
PINOUT DIAGRAM AND TERMINAL LIST



Package LE 14-pin TSSOP Pinout Drawing

Terminal List

Number	Name	Function
1	SINP / MISO / MHT	Sine output differential positive; SPI Master Input, Slave Output; Manchester programming
2	SINN / MOSI	Sine output differential negative; SPI: Master Output, Slave Input;
3	COSP / SCLK	Cosine output differential positive; SPI Clock terminal input
4	COSN / CSN	Cosine output differential negative; SPI: Chip Select terminal, active low input
5	GND	Ground
6	GND	Ground
7	VCC	Power supply
8	NC	Not connected Connect to ground in application
9	RX2N	Receiving coil 2 negative pin
10	RX2P	Receiving coil 2 positive pin
11	RX1N	Receiving coil 1 negative pin
12	RX1P	Receiving coil 1 positive pin
13	TXN	Transmitting coil negative pin
14	TXP	Transmitting coil positive pin

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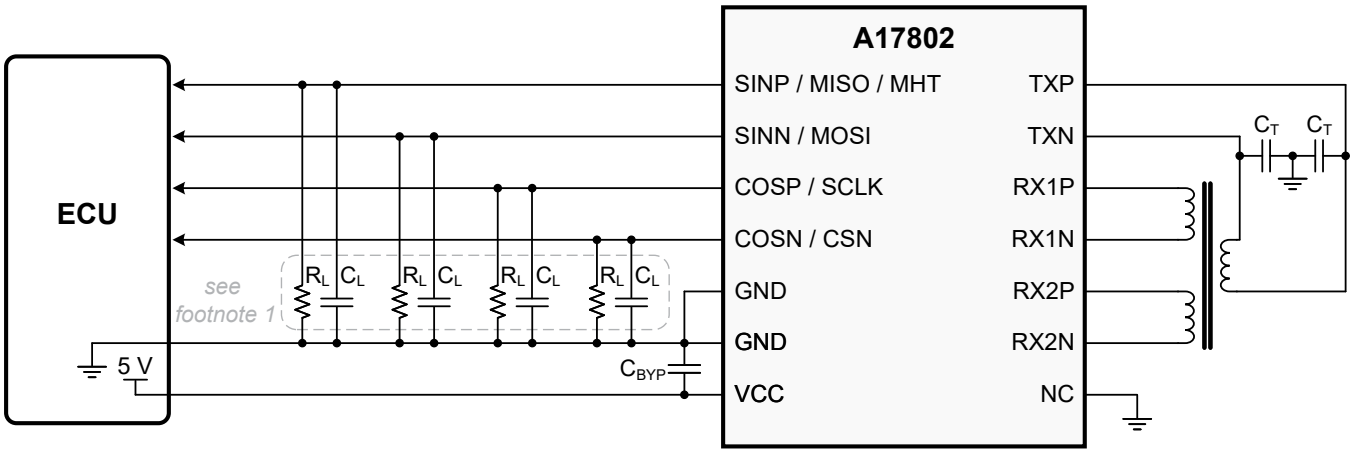
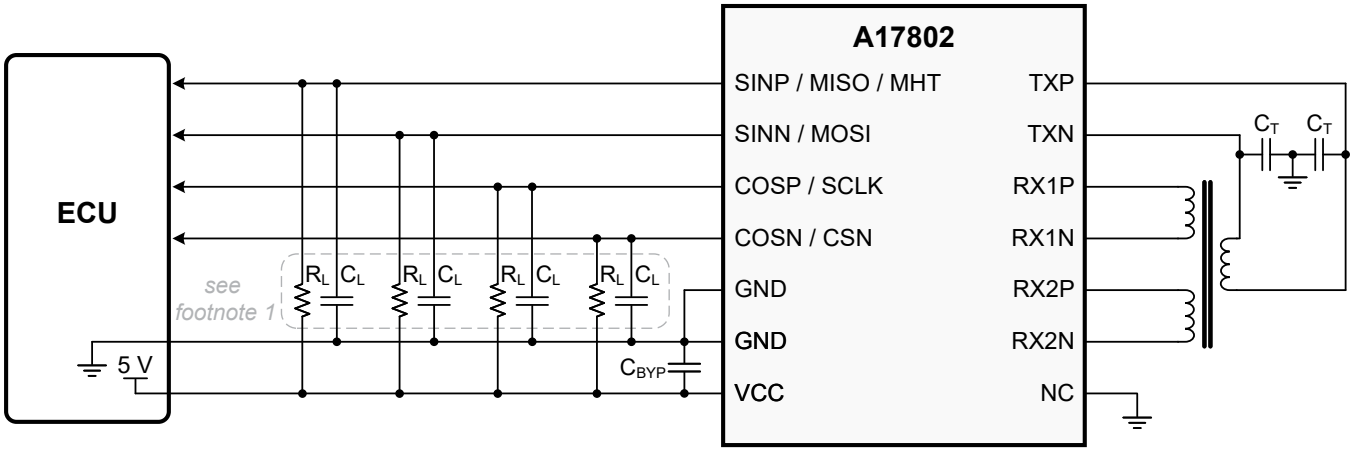
APPLICATION INFORMATION

Applications circuit with pull-down resistive loads



Applications circuit with pull-up resistive loads



[1] Device will be operational without R_L and C_L. For full performance and safety applications, refer to values in Operating Conditions table.

Figure 2: Typical application circuits with differential analog output. C_{BYP} = 200 nF. R_L and C_L values for full safety performance are reported in Operating Characteristics. Coil and target system design and C_T dimensioning is described in Functional Description section.

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CHARACTERISTIC PERFORMANCE

OPERATING CHARACTERISTICS: Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1]	V_{CC}		4.5	5	5.38	V
Supply Current	I_{CC}	Without coils, no load	–	–	23	mA
Transmitting Coil Tail Current [1]	I_{TX}	DC equivalent current; over all temperature range; minimum for TXDRV_TRIM = 0 at –40°C; maximum for TXDRV_TRIM = 127 at 160°C; TX_TC = –2	0.047	–	14.95	mA
Undervoltage Flag Threshold [2]	$V_{UVD(HIGH)}$	V_{CC} rising	4	–	4.4	V
	$V_{UVD(LOW)}$	V_{CC} falling	3.9	–	4.3	V
Undervoltage Detection Hysteresis	$V_{UVD(HYS)}$		75	–	150	mV
Overvoltage Flag Threshold [2]	$V_{OVD(HIGH)}$	V_{CC} rising	5.5	–	5.9	V
	$V_{OVD(LOW)}$	V_{CC} falling	5.38	–	5.8	V
Overvoltage Detection Hysteresis	$V_{OVD(HYS)}$		75	–	150	mV
Power-On Time	t_{PO}	Time from $V_{CC} > V_{CC(min)}$ to valid angle information within specified accuracy	–	–	5	ms
TRANSMITTING COIL DRIVING CHARACTERISTICS [4]						
Transmitting Coil Driving Voltage [3]	$V_{TX,PP}$	Peak-to-peak voltage oscillation between TXP and TXN at f_{TX} frequency	2	5	5.5	V_{PP}
Coil Driving Frequency	f_{TX}	External LC tank resonant frequency	3	–	4	MHz
Transmitting Coil Inductance	L_{TX}	V_{TX} = 5 V_{PP}	1	–	8	µH
LC Tank Quality Factor	Q	V_{TX} = 5 V_{PP}; external LC tank quality factor over all temperature range	10	–	–	–
f × Q × LTX product	f × Q × L_{TX}	V_{TX} = 5 V_{PP}; over all temperature range	30	–	2080	µH
Equivalent Parallel Resistance	R_P	V_{TX} = 5 V_{PP}; over all temperature range	189	–	13069	Ω
INPUT CHARACTERISTICS [4]						
Input Signal Voltage [5]	$V_{RX,PP}$		10	–	200	mV_{PP}
Rotational Electrical Frequency	f_{IN}		–	–	4.16	kHz
Allowed Direct Coupling Amplitude [6]	O_X, O_Y		–10	–	10	mV

[1] Maximum voltage must be adjusted for power dissipation and junction temperature depending on selected transmitting coil current; see Power Derating section.
[2] Full functional performance guaranteed within supply voltage range. Safety limits guaranteed down to $V_{UVD(F)}$ min and up to $V_{OVD(R)}$ max by design.
[3] TX current trim TXDRV_TRIM shall be programmed to have Transmitting Coil Driving Voltage within specified range.
[4] Parameter is not measured at final test. Determined by design.
[5] Full performance starting from 20 mV_{PP}; between 10 and 20 mV_{PP}, resolution and accuracy might be lower.
[6] Direct coupling causes offset on signals after demodulation. Offset can be compensated using fixed offset compensation (OGT) and with IC autocalibration (OGA) to improve sensor accuracy.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Peak-to-Peak Voltage	V_{OUT}	On SINP, SINN, COSP, COSN pins; peak	2.8	3	3.2	V_{PP}
Output Common-Mode	$V_{OUT(CM)}$	On SINP, SINN, COSP, COSN pins	2.2	2.25	2.3	V
Output Common Mode Variation Over Temperature [7]	$\Delta V_{OUT(CM)}$		–40	–	40	mV
Differential Amplitude Mismatch	A_{MIS}		–1	–	1	%
Differential Offset Voltage	$V_{DIFF(OFF,SIN)}$ $V_{DIFF(OFF,COS)}$		–10	–	10	mV
Output Signal Delay [8]	t_{DELAY}	Internal delay compensation enabled	–400	–	400	ns
Allowable Output Load Capacitance	C_L	Analog output mode; load from SINP, SINN, COSP, COSN to GND	4.5	10	25	nF
Allowable Output Load Resistance	R_L	Analog output mode; loads from SINP, SINN, COSP, COSN to GND (pull-down) or loads from SINP, SINN, COSP, COSN to VCC (pull-up)	4.7	–	10	kΩ
FAILURE OUTPUT CHARACTERISTICS						
Internal Failure Output Voltage (Pull-Down)	$V_{FAIL,D}$	Pull-down load; on SINP, SINN, COSP, COSN pins	–	–	0.4	V
Internal Failure Output Voltage (Pull-Up)	$V_{FAIL,U}$	Pull-up load; on SINP, SINN, COSP, COSN pins	0.96 × V_{CC}	–	–	V
Broken Wire Voltage (Pull-Down)	$V_{BRK,U}$	Pull-down load; on SINP, SINN, COSP, COSN pins	–	–	0.4	V
Broken Wire Voltage (Pull-Up)	$V_{BRK,D}$	Pull-up load; on SINP, SINN, COSP, COSN pins	0.96 × V_{CC}	–	–	V
PERFORMANCE CHARACTERISTICS						
Electrical Angle Accuracy [9]	E_{ANG}	Ideal input signals; with external compensation of offset and amplitude mismatch in host on analog differential output signals prior to angle calculation; measured in static condition (no latency effect on error); value is ±3 sigma at 0-hour	–0.36	–	+0.36	degrees
Lifetime Start-Up Error Drift [10]		Based on AEC-Q100 grade 0 qualification	–	–	0.15	degrees
Effective Resolution on SIN, COS	$ER_{SIN,COS}$	Assuming ideal, noise free input; calculated as log2($V_{OUT(SIN/COS)}$ / $Noise_{RMS}$) where $V_{OUT(SIN,COS)}$ is the peak-to-peak value of differential signals output; measurement bandwidth: 20 kHz	–	12	–	bits

[7] Central $V_{OUT(CM)}$ (25°C) value is measured at room temperature as the mean of the single-ended output signal over one period. The difference $V_{OUT(CM)}$ (T) – $V_{OUT(CM)}$ (25°C) at a given operating temperature T should not exceed specified $\Delta V_{OUT(CM)}$.
[8] Output signal delay is not tested or guaranteed at –40°C.
[9] Angle error and drift are inferred through angle characterization and signal path testing–not directly measured at final test. Error value can be decreased by using IC internal compensations with end-of-line calibration and dynamic auto-calibration algorithm (OGA) in continuous rotary applications.
[10] Lifetime error drift can be compensated by dynamic auto-calibration algorithm (OGA) in continuous rotary applications.

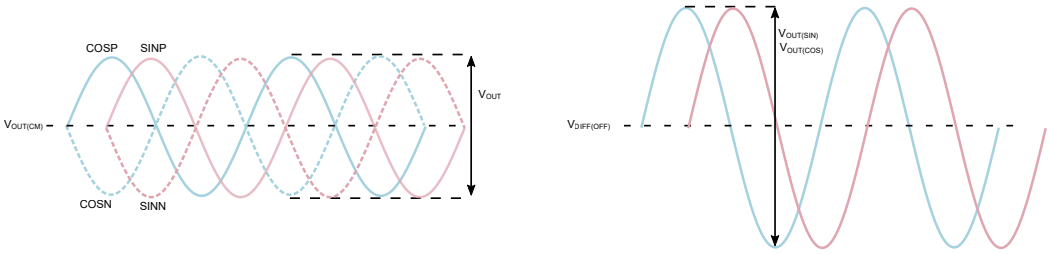

Figure 3: Output signals and differential signals.
$V_{OUT(SIN)} = V_{OUT(SINP)} + V_{OUT(SINN)}$. $V_{OUT(COS)} = V_{OUT(COSP)} + V_{OUT(COSN)}$.

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FUNCTIONAL DESCRIPTION

Overview

The A17802 is an interface IC for position sensors based on electromagnetic induction principle.

The sensing element is constituted by a transmitting coil and two receiving coils, connected to the IC, and a rotating metallic target.

When operating, the IC sustains oscillations in the transmitting coil that is appropriately connected with external capacitors to form an LC tank. The transmitted signal induces Eddy currents in the target, which conversely generate an electromagnetic field that induces an electromotive force in the receiving coils. With an appropriate design of the coils and target system, the received signals amplitude is modulated by the target position and the modulation terms of the two received signals are in quadrature, as depicted in Figure 4.

The received signals can be approximately described by the following equations:

$$v_{RX1} = V_Y(\sin(\theta_e) + H_Y(\theta))\sin(2\pi f_{TX}t + \phi) + O_Y\sin(2\pi f_{TX}t)$$

$$v_{RX2} = V_X(\cos(\theta_e) + H_X(\theta))\sin(2\pi f_{TX}t + \phi) + O_X\sin(2\pi f_{TX}t)$$

where:

V_Y, V_X are the peak amplitude value of target position modulation of input signals,

O_Y, O_X are the direct coupling amplitude,

f_{TX} is the carrier frequency corresponding to the transmitted signal frequency,

t is the time,

ϕ is the phase shift between transmitted signal and target reflected signal,

H_X, H_Y represent all residual distortion terms,

θ is the absolute mechanical position of the target, and

θ_e is the electrical position of the target.

The electrical position and the mechanical position are linked by the number of periods (or teeth) present in the target-receiving coil system:

$$\theta_e = \mathrm{mod}(N\times\theta, 360°)$$

where mod is the modulo function.

The A17802 demodulates the received signals v_{RX1} and v_{RX2} and condition them digitally to accurately extract and output the electrical angle information θ_e.

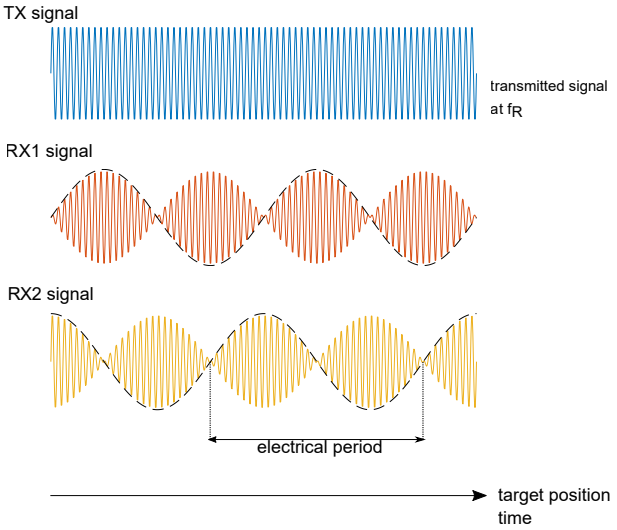

Figure 4: Transmitted and received signals

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Coils and Target Design

The transmitting coil constitutes the inductive part of the external LC tank that must be connected to the IC. The target shape and receiving coil system is chosen depending on the applications to have a single or multiple electrical periods over a single mechanical rotation.

Each receiving coil is composed of at least two loops connected to have the current oriented clockwise (CW) in one loop and counterclockwise (CCW) in the second one in order to cancel the total magnetic flux not reflected by the target. The SIN and COS coils are arranged to have a 90° electrical shift distance between them. The transmitting coil encompasses the set of receiving coils.

For rotary applications, a basic design for the receiving coil loops can be obtained with the following equations in polar coordinate system:

$$R(\theta) = Rin + A\,(1 + \cos(N\theta + \phi))$$

where N is the number of periods, θ is the mechanical angle, ϕ is the mechanical phase shift. The minimum number of four loops can be obtained by choosing ϕ = 0°, 180° for COS and ϕ = 90°, 270° for SIN.

The target is designed to match the receiving coils in terms of number of periods and its teeth should extend over the transmitting coil radius.

The number of windings for the coils and the size of coils must be designed according to the application conditions, such as target material and target-to-coils distance, to match the IC operating conditions for the inputs' voltage levels.

A concept layout for rotary sensor with four electrical periods is shown in Figure 5.

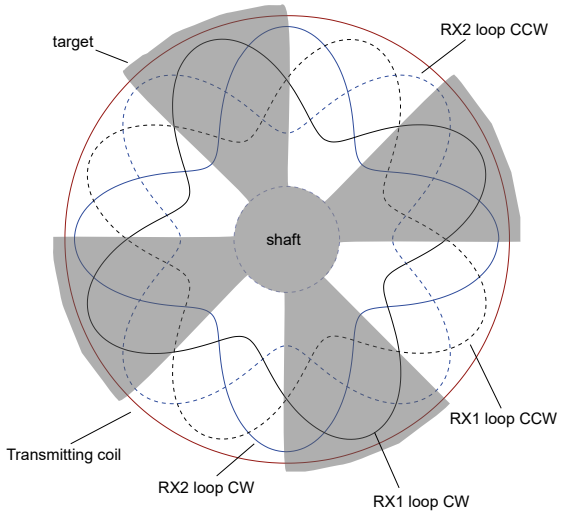

Figure 5: Coil and target design for 4 electrical periods

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LC Oscillator

The A17802 integrates an oscillator driver that sustains transmitted signal oscillation in the external LC tank.

The inductance value L_{TX} is the transmitting coil inductance at the specified frequency range and with the target placed in front of the coils system. The value of the shunt capacitances C_T in application circuit is chosen in combination with L_{TX} to have a resonant frequency f_{TX} within the range specified in operating characteristics table:

$$f_R = \frac{1}{2\pi\sqrt{L_{TX}\frac{C_T}{2}}}$$

$$C_T = \frac{2}{(2\pi f_R)^2 L_{TX}}$$

The LC tank oscillator has non-zero losses due to coil parasitic resistance and electromagnetic interaction with the target. The losses can be represented with an equivalent parallel resistor to the LC tank as in Figure 6.

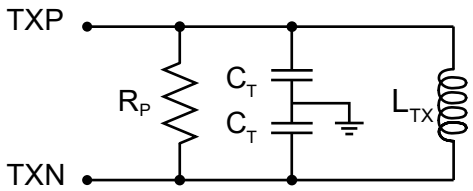

Figure 6: LC tank equivalent circuit; R_P represents losses

The value of the equivalent parallel resistance is related to the quality factor Q of the circuit with the relation:

$$Q = \frac{R_P}{2\pi f_R L_{TX}}$$

The Q-factor shall be evaluated by considering resistive electromagnetic losses in the coil and in the target in application conditions and must be within the specified range.

The LC-oscillator driver works by injecting a controlled current in the external LC circuit determined by the current trim code in EEPROM field TXDRV_TRIM (see EEPROM section). Given a certain transmitting current value, the corresponding transmitting voltage peak amplitude at the resonant frequency is approximately expressed by the equation:

$$V_{TX} = I_{TX}\, R_P\, \sin(2\pi f_{TX} t)$$

where R_P is the equivalent parallel resistor of the LC tank.

TXDRV_TRIM shall be chosen not to exceed $V_{TX(max)}$ as defined in operating characteristics.

The transmitting current is adjusted with the sensed temperature to limit transmitting voltage variation over temperature due to changes in coil resistivity and losses.

The transmitting current amplitude at each temperature T is approximately given by the equation:

$$I_{TX} = I_{TX,25°C}(1 + \mathrm{TC_{TX}} \times (T - 25\,°\mathrm{C}))$$

where $I_{TX,25°C}$ is the nominal current and TC_{TX} is a temperature coefficient determined by EEPROM field D_TX_TC.

For typical operations, D_TX_TC is set to code 14 (default EEPROM value), corresponding to a coefficient nominal value of $2.82 \times 10^{-3}\ °C^{-1}$.

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FRONT-END CONFIGURATION

Automatic Gain Selection

The A17802 integrates a power-on automatic gain selection (AGS) to amplify the received signals before the analog to digital conversion and improve the overall angle calculation accuracy. The optimal gain value is determined after each device repower. Gain does not change during a power cycle.

AGS can be disabled by setting field AGS_EN to 0; in this case, the front-end gain is determined by the value programmed in FE_SENS_TRIM EEPROM field.

Input Phase Delay Compensation (Steel Target Compensation)

The A17802 integrates compensation of the phase delay between TX and RX signals in a demodulation scheme to maximize the demodulated signal amplitude. This feature allows the counter of signal loss in the demodulation scheme due to phase shift caused by extra target losses when using a ferrous material such as steel. The phase compensation value can be adjusted by modifying memory field D_TX_CK_PH_TRIM[3:0].

DIGITAL COMPENSATIONS

The A17802 integrates several digital compensations on input signals Y (RX1) and X (RX2) to improve output angle accuracy.

Offset and Gain Trimming (OGT)

Post-demodulation offset due to CW and CCW loop imbalances in the sensor coil can be digitally removed by programming fields OGT_X_OFFSET_C and OGT_Y_OFFSET_C. The amplitude mismatch between the two channels can be corrected by programming gain fields OGT_X_GAIN_C and OGT_Y_GAIN_C.

Electrical Harmonic Compensation (EHC)

The A17802 integrates the possibility of digitally compensating for the higher electrical harmonic errors due to sensor design.

By programming EEPROM fields X_H(i)_AMP, X_H(i)_PHASE, Y_H(i)_AMP, Y_H(i)_PHASE, where (i) = 2,3,4; the 2nd, 3rd, and 4th electrical harmonics can be digitally removed from input x and y signals. To do so, the A17802 calculates each harmonic component using the programmed fields and calculated angle:

$$Y\_H(i) = Y\_H(i)\_AMP \times \sin(i \times \theta_e + Y\_H(i)\_PHASE)$$

$$X\_H(i) = X\_H(i)\_AMP \times \sin(i \times \theta_e + X\_H(i)\_PHASE),$$

where i = 2, 3, or 4.

The harmonic components are removed from the signals prior to angle calculation.

Offset and Gain Autocalibration (OGA)

During operation, a dynamic offset and gain autocalibration algorithm (OGA) tracks the signals after electrical harmonic compensation and removes residual offset and amplitude mismatch after static trimming.

The OGA algorithm tracks all maxima and minima over a number of electrical periods determined by the EEPROM field N_AVG_CYCLES_OGA and then calculates a correction offset and a correction amplitude to be applied to the x and y signals. For optimal operation, N_AVG_CYCLES_OGA is typically matched to the largest multiple ≤16 of the number of electrical periods over a full mechanical rotation of the target. OGA has an option to filter the applied compensation with a weighted update of offset and gain correction coefficients (25% of new value plus 75% of old value). Filtering can be disabled by setting EEPROM bit OGA_FILT_DIS.

For the algorithm to operate correctly, residual offset after OGT and EHC trim shall be always smaller than half the amplitude of the corresponding X and Y signals after OGT over the mechanical period.

Quadrature Compensation

The A17802 offers the possibility of removing quadrature error up to ±11.25° between the demodulated input signals by programming EEPROM field QUADRATURE_COMP.

Latency Compensation (Synchronization Compensation)

The A17802 integrates a delay compensation mechanism to reduce the effective path latency of the IC. An optional compensation for external delays up to ±256 µs is available for customer by programming field DEL_SYS_ABS.

Angle Reference and Rotation Direction

The A17802 offers the possibility of programming a zero degrees angle reference position (EEPROM field DEL_ZERO_ANGLE). Signals rotation direction for output angle signals with respect to input signals can be inverted by setting EEPROM field DEL_ANGLE_POL.

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DEVICE PROGRAMMING INTERFACES

The A17802 can be programmed in two ways:

- Using the SPI interface.
- Using a Manchester protocol on pin 1.

The programming interface is accessible through output pins, enabling in-system programming with a normal harness.

The A17802 does not require special supply voltages to write to the EEPROM.

All accessible fields of the IC may be read and written using both protocols. If EEPROM locking is used, write access using either protocol may be limited.

Interface Structure

The A17802 consists of two memory blocks: direct memory (primary serial registers), and extended memory (EEPROM, shadow memory, volatile registers). The primary serial interface registers are used for direct writes and reads by the host controller for frequently required information (for example, angle data, warning flags, field strength, and temperature). All forms of communication (including the extended locations) operate through the primary registers, whether it be via SPI or Manchester.

The primary serial registers provide data and address location for accessing extended memory locations. Accessing these extended locations is done in an indirect fashion; the controller writes into the primary interface to give a command to the sensor to access the extended locations. Read/Write is executed, and the result is again presented in the primary interface. This concept is shown in Figure 7.

For writing extended locations, the primary interface registers INDIRECT_WR_ADDRESS (primary: 0x1), INDIRECT_WR_DATA_MSB (primary: 0x2), and INDIRECT_WR_DATA_LSB (primary 0x3) are used for writing extended memory locations. INDIRECT_WR_ADDRESS holds the address of the target extended memory location to be written. INDIRECT_WR_DATA_MSB and INDIRECT_WR_DATA_LSB, contain the two high bytes and the two low bytes for the extended location contents. The INDIRECT_WR_STATUS (primary: 0x4) register is used for commands and status information. For further information and other register fields associated with indirect memory transactions, refer to Read Transaction from EEPROM and Other Extended Locations.

For reading extended locations, the primary interface registers INDIRECT_RD_ADDRESS (primary: 0x5), INDIRECT_RD_DATA_MSB (primary: 0x7), and INDIRECT_RD_DATA_LSB (primary 0x8) are used for reading extended memory locations. INDIRECT_RD_ADDRESS holds the address of the target extended memory location to be read. INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB contain the two high bytes and the two low bytes for the extended location contents. The INDIRECT_RD_STATUS (primary: 0x6) register is used for commands and status information. For further information and other register fields associated with indirect memory transactions, refer to Read Transaction from EEPROM and Other Extended Locations.

For more information on EEPROM and shadow memory read and write access, see EEPROM and Shadow Memory Usage.

The primary serial interface can be accessed using the SPI and using the Manchester interface. These two interfaces are detailed in the following sections.

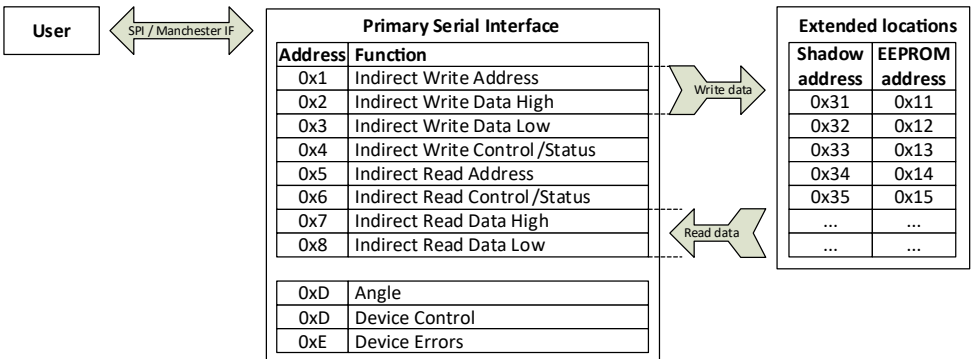

Figure 7: Serial registers allow access to extended memory (EEPROM and shadow)

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SPI

The A17802 provides a full-duplex 4-pin SPI interface, using SPI mode 3 (CPHA = 1, CPOL = 1).

The sensor responds to commands received on the MOSI (controller-out/peripheral in), SCLK (serial clock), and $\overline{CS}$ (chip-select) pins, and outputs data on the MISO (controller in/peripheral out) pin.

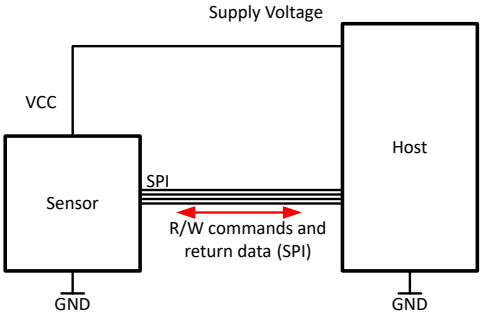

Figure 8: SPI Interface Programming Setup

TIMING

The interface timing parameters from Table 1 are displayed in Figure 9 and Figure 10.

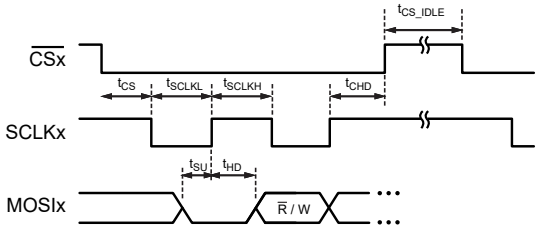

Figure 9: SPI Interface Timings Input

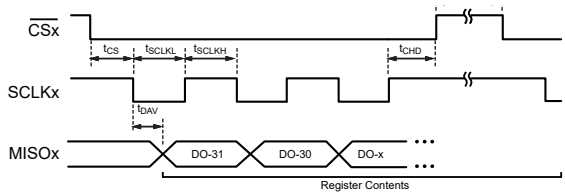

Figure 10: SPI Interface Timings Output

Table 1: SPI Interface Timings Output [1]

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
SPI GENERAL SPECIFICATIONS [1]						
Load Resistance	R_L		100	–	–	kΩ
Load Capacitance	C_L	Loading on digital output (MISO)	–	–	20	pF
SPI INTERFACE VOLTAGE SPECIFICATIONS [1]						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Digital Output High Voltage	V_{OH}	MISO pin, C_L = 20 pF, T_A = 25°C	4	5	5.5	V
Digital Output Low Voltage	V_{OL}	MISO pin, C_L = 20 pF, T_A = 25°C	–	0.3	0.5	V
SPI INTERFACE TIMING SPECIFICATIONS [1]						
SPI Message Length	SPI_{LENGTH}		32	–	32	bits
SPI Clock Frequency	f_{SCLK}	MISO pins, $C_L \leq 20$ pF	0.1	–	5	MHz
SPI Clock Duty Cycle	D_{fSCLK}	SPI_{CLKDC}	40	–	60	%
SPI Frame Rate	f_{SPI}	SPI message is 32 bits	3	–	140	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge, C_L = 20 pF	–	30	–	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to $\overline{CS}$ Hold Time	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns

[1] Parameter is not measured at final test. Limits are based on design simulations.

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MESSAGE FRAME

The SPI interface uses a 32-bit packet and is designed to provide a high level of confidence in data integrity. Three SPI transactions are possible: write cycle, read request (from the controller), and read response (from the peripheral).

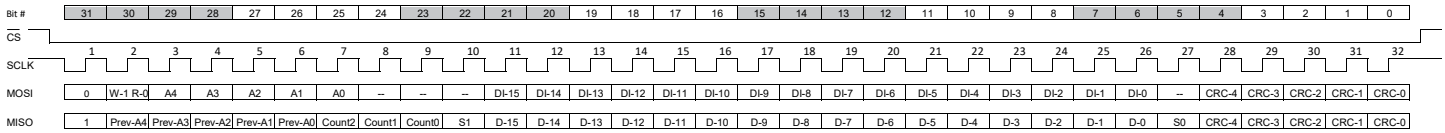

Figure 11: 32-Bit SPI Frame

Write Cycle or Read Request Cycle

The frame structures of the write cycle and read request are shown in Figure 12 and Figure 13, respectively. The frames consist of:

- Start Bit [31]: Static bit with logic = 0. This bit is not used in the CRC calculation.
- R/W [30]: Read/Write bit set to logic = 1 indicates a write cycle; logic = 0 indicates a read request.
- Address [29:25]: Address bits for accessing primary registers.
- Data [21:6]: Data bit for writing primary registers. Considered immaterial for a read request.
- CRC [4:0]: CRC bits calculated on the frame bits [30:5].
- Immaterial bits [24:22, 5]: Can be set to logic = 1 or logic = 0.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	Address [4:0]					—			Data [15:0]																—	CRC [4:0]				

Figure 12: Write Cycle SPI Frame

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	Address [4:0]					—			Data [15:0] (Immaterial for a read request)																—	CRC [4:0]				

Figure 13: Read Request Cycle Frame

Read Response Cycle

The read response cycle frame is sent from the IC, as shown in Figure 14. The frame consists of the following:

- Start bit [31]: This bit is set to logic = 1. This bit is not used in the CRC calculation.
- Previous address [30:26]: Register address corresponding to the read request data.
- Frame count [25:23]. Frame counter increments with each SPI frame.
- S1 [22]: Status/Error Flag
  - □ Logical OR of all unmasked error flags.
  - □ Will clear once presented following a read (assuming condition has cleared).
- S0 [5]: Status/Error Flag
  - □ Logical OR of all unmasked error flags.
  - □ Will clear once presented following a read (assuming condition has cleared).
- Data [21:6]: Data contents from primary register.
- CRC [4:0]: CRC bits calculated over the frame [30:5].

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	Previous Address [4:0]					Frame Count [2:0]			S1	Data [15:0]																S0	CRC [4:0]				

Figure 14: Read Response Cycle Frame

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SPI CRC

Each SPI frame includes a 5-bit CRC, calculated using the polynomial: $x^5 + x^2 + 1$ with a seed value of 11111_2.

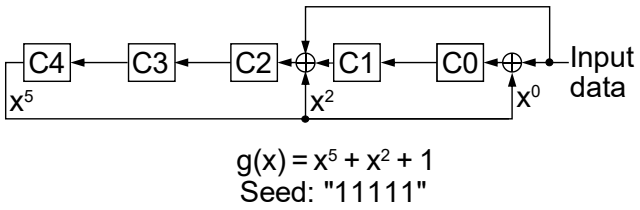

Figure 15: CRC Calculation with Left Shift Register

The outgoing CRC is calculated by the A17802 and transmitted on the MISO pin. The incoming CRC must be calculated by the controller and included on the MOSI pin. The A17802 checks the CRC on every incoming frame, and any invalid frame is ignored. The CRC achieves a Hamming distance of 3 for secure data transmission.

The CRC may be calculated with the following Python code:

```
def spi_crc(data_frame):
 """
 SPI CRC: Takes 27 bit input and generates 5 bit CRC.
 Polynomial = x^5 + x^2 + 1
 Initial CRC value set to all 1s

 Input:
 data_frame: a string representing 27 bit binary data
 """
 crc = list('11111') #CRC seed = 11111
 # MSB of SPI frame is not used during CRC calculation.
 for j in range(1, 27):
 old_crc = crc
 aux_crc_1 = crc[1]
 aux_crc_4 = crc[4]
 crc[4] = int(old_crc[3])
 crc[3] = int(old_crc[2])
 crc[2] = int(aux_crc_1) ^ int(aux_crc_4) ^ int(data_frame[j])
 crc[1] = int(old_crc[0])
 crc[0] = int(aux_crc_4) ^ int(data_frame[j])
 #flips calculated CRC around to obtain value in proper order
 crc = crc[::-1]
 return crc
```

A MATLAB implementation of the CRC is:

```
function [output_binary_word,CRC]=Allegro_CRC_x5_x2(input_
binary_word)
%% Initialization
CRC=ones(5,1);
%% CRC calculation
for i=1:length(input_binary_word)
 old_CRC=CRC;
 aux_CRC2=CRC(2);
 aux_CRC5=CRC(5);
 CRC(5)=old_CRC(4);
 CRC(4)=old_CRC(3);
 aux=xor(aux_CRC2,aux_CRC5);
 CRC(3)=xor(aux,str2num(input_binary_word(i)));
 CRC(2)=old_CRC(1);
 CRC(1)=xor(aux_CRC5,str2num(input_binary_word(i)));
end
%% Outputs
CRC=[num2str(CRC(5)) num2str(CRC(4)) num2str(CRC(3))
num2str(CRC(2)) num2str(CRC(1))];
output_binary_word=[input_binary_word CRC];
```


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Manchester Interface

The A17802 incorporates a serial interface shared with the SINP pin (Note: The A17802 may be programmed via SPI, with additional wiring connections). This interface allows an external controller to read and write registers in the A17802 EEPROM and volatile memory. The point-to-point communication protocol is based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first.

The setup for communication using the Manchester interface is given in Figure 17.

The Manchester interface allows programming and readout with a minimal number of pins involved. A valid auxiliary request command recognized by the sensor places the device into communications mode. In this mode, serial data is transmitted or received on the MHT pin. In the absence of a clock signal, Manchester encoding is used, allowing the sensor to determine the bit rate requested by the Controller. The high and low logic level for the Manchester serial data is determined by the Manchester High and Low Voltage parameters.

The MHT output consists of an open drain type circuit. A sufficient pull-up resistor and external supply voltage are required.

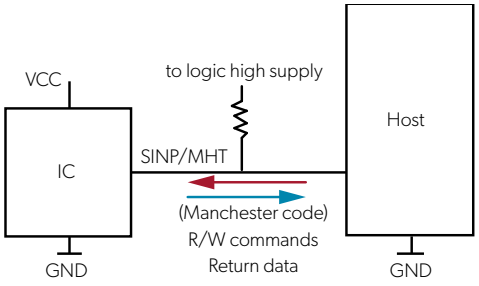

Figure 16: Manchester Programming Interface Setup

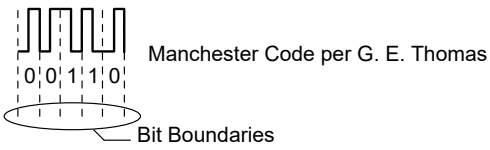

Figure 17: Manchester Code

MANCHESTER MESSAGE STRUCTURE

The general format of the Manchester message frame is shown in Figure 19. Serial binary data is encoded using a Manchester encoding scheme, where logic = 1 is indicated by a falling edge within the bit boundary, and logic = 0 is indicated by a rising edge within the bit boundary. The time period for the bit boundary is determined by the baud rate initiated by the external controller. The A17802 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 2.

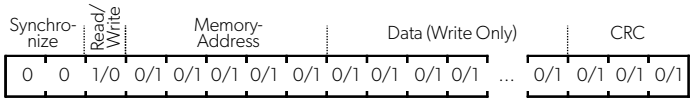

Figure 18: Manchester Message Structure

Table 2: Manchester Message Structure

Quantity of Bits	Name	Values	Description
2	Synchro-nization	0	Used to identify the beginning of a serial interface command and communication bit time
1	Read / Write	0	[As required] Write operation
		1	[As required] Read operation
5	Address	0x-0x1F	[Read/Write] Register address (of primary serial interface)
16	Data	0/1	Write only
3	CRC	0/1	Bits to check the validity of frame

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READ COMMAND

The Read command is 11 bits in length, composed of 2 synchronization bits, 1 R/W bit, 5 memory address bits, and 3 CRC bits.

READ ACKNOWLEDGE

The Read Acknowledge frame is 21 bits in length, composed of 2 synchronization bits, 16 data bits, and 3 CRC bits.

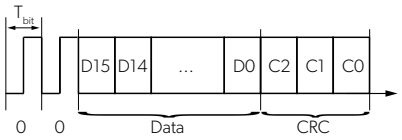

Figure 19: Manchester Read Acknowledge Command

WRITE COMMAND

The Write command is 27 bits in length, composed of 2 synchronization bits, 1 R/W bit, 4 die ID bits, 5 memory address bits, 16 data bits, and 3 CRC bits.

The 5-bit memory address corresponds to the serial register address to which the 16 bits is written.

TIMING DURING A MANCHESTER READ RESPONSE

The A17802 never initiates communication. The A17802 recognizes four transactions: write access, write to EEPROM, write to volatile, and read. Only the read transaction prompts the A17802 to respond with data. When responding to a read command, the A17802 does not check for line contention; it is the responsibility of the controller to release the line in time and to be ready to read the data sent by the A17802.

After a read command is received, there is a delay between when the last bit of the command is sent to the device and when the device begins to respond on the line. This delay has two parts:

- The first part of the delay (t_d) occurs between the time the last bit of the read command is received and the time the device begins to pull the line low in preparation to send data.
- The second part of the delay (t_b) occurs between the time the device pulls the line low to the time the device begins outputting data. The output is fully readable as long as the controller releases control before $t_d + t_b$; however, it is recommended that the line be released before t_d.

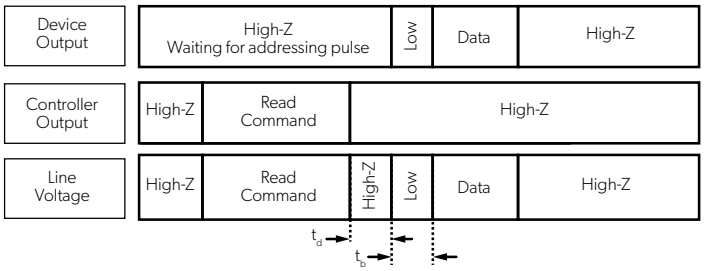

Figure 20: Manchester Read Response Timing

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MANCHESTER CRC

The Manchester serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored by the check). The CRC algorithm is based on the following polynomial and the CRC calculation is represented graphically in Figure 21. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 0b111.

$$g(x) = x^3 + x + 1$$

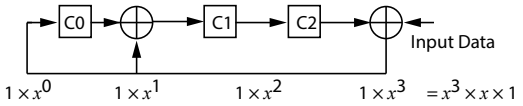

Figure 21: Manchester CRC Calculation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the Manchester command, right justified, does
not include the space for the CRC
// numberOfBits: number of bits in the command not includ-
ing the 2 zero sync bits at the start of the command and the
three CRC bits
// Returns: The three bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD

uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
 bool C0 = false;
 bool C1 = false;
 bool C2 = false;
 bool C0p = true;
 bool C1p = true;
 bool C2p = true;
 uint64_t bitMask = 1;

 bitMask <<= numberOfBits - 1;

 // Calculate the state machine
 for (; bitMask != 0; bitMask >>= 1)
 {
 C2 = C1p;
 C0 = C2p ^ ((data & bitMask) != 0);
 C1 = C0 ^ C0p;

 C0p = C0;
 C1p = C1;
 C2p = C2;
 }

 return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U : 0U);
}
```


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EEPROM AND SHADOW MEMORY USAGE

The A17802 device features include integrated EEPROM to permanently store configuration parameters for operation. EEPROM is customer programmable and retains data, or parameter values, to configure the device for the application requirements. After a reset or EEPROM write operation, parameter data is copied from EEPROM to shadow (volatile) memory. Parameter data in shadow memory can be overwritten by performing an extended write to the shadow addresses. Access of device parameters through shadow memory is faster than access through EEPROM. In situations where it is desired to test many parameters quickly before permanently programming, use of shadow memory is recommended. The shadow memory registers have the same format as EEPROM and are accessed at extended addresses 0x20 higher than the equivalent EEPROM address. Some bits do not impact device operation and are not copied into shadow memory. Shadow registers do not contain the ECC bits and may have read or write protection restrictions similar to EEPROM.

Enabling EEPROM Access

Writes to indirect memory, EEPROM, and shadow memory are restricted and require an unlock code (reading is allowed without unlocking the device). The unlock code must be written to the primary serial register access (primary: 0x1E [15:0]) within 20 ms from power-on. This involves two write commands, which should be executed one after the other.

The last bit of unlock code sets or clears field COMM_EN (extended 0xA5 [15]), determining if output is disabled or not. When COMM_EN is set, it allows continuous R/W commands with the output being disabled without needing to overdriving the output pin.

Sequence to enable memory access while keeping output enabled (COMM_EN=0):

Write 0xC418 to register primary 0x1E [15:0].
Write 0x0E80 to register primary 0x1E [15:0].

Sequence to enable memory access and disable output (COMM_EN=1):

Write 0xC418 to register primary 0x1E [15:0].
Write 0x0E81 to register primary 0x1E [15:0].

When the COMM_EN is written with logic = 0, or when a reset event occurs, the outputs are enabled again.

The access status is indicated by the direct serial register access. A read of primary 0x1E [1] set to logic = 1 indicates the customer unlock code is set.

When using SPI interface customer unlock code is not required for write and read operations to all direct serial registers.

Following an EEPROM write, EEPROM margin checking should be performed. The device must be unlocked when performing margin checks.

EEPROM and Shadow Access Protections

The A17802 contains features to protect against unwanted EEPROM access.

- Setting the EEPROM parameter MEM_LOCK (extended: 0x1F [23:20]) to a value of 0xC (1100 binary) restricts write access to prevent changes to the EEPROM registers. Temporary changes to device configuration settings are still possible by writing to the indirect volatile and shadow memory. Note, any changes to the indirect volatile memory are reset after a device reset event. Read access of the EEPROM is still possible.
- Setting the EEPROM parameter MEM_LOCK (extended: 0x1F [23:20]) to a value of 0x3 (0011 binary) restricts write access to prevent changes to EEPROM, indirect volatile, and shadow memory. Once set, the parameter settings in indirect memory are read only. Read access is still possible.
- Writes to MEM_LOCK with the above values are one-time access only and are not erasable through subsequent write commands.

Write Transactions to Extended Memory: EEPROM, Shadow, and Volatile

Invoking an extended write access is a three-step process:

1. Write the target extended address to the primary register INDIRECT_WR_ADDRESS (primary: 0x1 [7:0]).
2. Write the desired data, for the target extended register, to the primary registers INDIRECT_WR_DATA_MSB (primary: 0x2 [15:0]) and INDIRECT_WR_DATA_LSB (primary: 0x3 [15:0]). The register INDIRECT_WR_DATA_LSB corresponds to the data bits [15:0] of the target extended memory address. The register INDIRECT_WR_DATA_MSB corresponds to the data bits [31:16] of the target extended memory address.
3. Execute the extended memory write by setting the extended memory execute write bit (EXW; primary: 0x4 [15]), to logic = 1.

   A. EEPROM writes require ≈ 6.5 ms to complete.

When EXW is set, the 32 bits of data contained in INDIRECT_WR_DATA_LSB and INDIRECT_WR_DATA_LSB are written to the indirect memory address specified by INDIRECT_WR_ADDRESS. The status of the write operation may be interrogated

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by polling the primary register INDIRECT_WR_STATUS (primary: 0x4). The write-in-progress bit (WIP; primary: 0x4 [8]), when set, indicates the write transaction in progress. The write operation done bit (WDN; primary: 0x4 [0]), when set, indicates the write transaction is done or complete. The extended execute error status bit (XEE; primary: 0x0F [14]), when set, indicates an error occurred when executing the write. For example, if a write is attempted without the proper access enabled, XEE indicates an error.

READ TRANSACTION FROM EEPROM AND OTHER EXTENDED LOCATIONS

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM and EEPROM shadow registers. All extended registers are up to 32 bits wide. Invoking an extended read access is a three-step process:

1. Write the extended address to be read into the INDIRECT_RD_ADDRESS (primary: 0x5) register (using SPI or Manchester direct access). The 8-bit extended address that determines which extended memory address to access is INDIRECT_RD_ADDRESS.
2. Invoke the extended access by writing the extended read bit (EXR; primary: 0x6 [15]) with a value of 1. The address specified in INDIRECT_RD_ADDRESS is then read, and the data is loaded into the registers INDIRECT_RD_DATA_MSB (primary: 0x7) and INDIRECT_RD_DATA_LSB (primary: 0x8).
3. Read the registers INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB (using SPI or Manchester direct access) to get the full data contents of the extended read address. The register INDIRECT_RD_DATA_LSB corresponds to the data bits [15:0] of the target extended memory address. The register INDIRECT_RD_DATA_MSB corresponds to the data bits [31:16] of the target extended memory address.

EEPROM read accesses may take up to 2 µs to complete. The read operation done bit (RDN; primary: 0x6 [0]) can be polled to determine if the read access is complete before reading the data. Shadow register reads complete in one system clock cycle after synchronization. Do not attempt to read the registers INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB if the read access is in process (RIP; primary: 0x6 [8] = 1), as it could change during the serial access, which would result in inconsistent data. It is also possible that an SPI CRC error would be detected if the data were to change during the serial read via the SPI interface.

Shadow Memory Read and Write Transactions

Shadow memory read and write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM extended address, the shadow extended addresses must be addressed. Shadow extended addresses are located at an offset of 0x20 above the EEPROM. For all addresses, refer to the EEPROM section, Table 3 and Table 4.

EEPROM Margin Check

The A17802 contains a test mode, EEPROM margining, to check the logic levels of the EEPROM bits. EEPROM margining is customer accessible. EEPROM margining is selectable to check all logic = 1 values, logic = 0 values, or both. The results of the test are reported back in extended memory registers 0x42, 0x43, and 0x44. Note that a fail of the margin test does not force the outputs to a diagnostic state or trigger a diagnostic error flag. The following is a step-by-step procedure to verify EEPROM programming:

1. Enable EEPROM access by sending the unlock code to primary address 0x1E
2. Write a 1 to the MARGIN_START field (volatile 0x44 [0])
   A. Once started the device automatically checks high/low thresholds for all EEPROM addresses.
3. Read MARGIN_STATUS (volatile 0x44[4:3])
   0 = No result from margin testing (margin testing not run)
   1 = Pass. Margin checking completed with no errors.
   2 = Failure detected during margin testing
   3 = Running. Margin testing is still running.
4. If a margin failure is detected additional information can be retrieved.
   MARGIN_MIN_MAX_FAIL [volatile 0x44 [5]
   0 = Margin low threshold failure
   1 = Margin high threshold failure
   EE_ADDR [volatile 0x42 [11:7] contains the failing address.

5. EEPROM should not be considered valid unless margin testing passes. If the margin failure occurs on a previously modified address space, EEPROM can be rewritten and margin checking repeated in an attempt to clear the issue.

For more information about EEPROM margining, refer to the Volatile Memory Map section (addresses 0x42, 0x43, and 0x44). Time required to verify margin levels across all EEPROM is ≈100 µs

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PRIMARY SERIAL INTERFACE REGISTER REFERENCE

Table 3: Direct Serial Interface Registers Bits Map

ADDRESS (0X00)	REGISTER SYMBOL	ACCESS	PRIMARY ADDRESSED BYTE (MSB)								PRIMARY ADDRESSED BYTE (LSB)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	NULL_REG	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x01	INDIRECT_WR_ADDRESS	RW	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							
0x02	INDIRECT_WR_DATA_MSB	RW	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							
0x03	INDIRECT_WR_DATA_LSB	RW	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							
0x04	INDIRECT_WR_STATUS	WO/RO	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
0x05	INDIRECT_RD_ADDRESS	RW	0	0	0	0	0	0	0	0	INDIRECT_READ_ADDR							
0x06	INDIRECT_RD_STATUS	RO	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
0x07	INDIRECT_RD_DATA_MSB	RO	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							
0x08	INDIRECT_RD_DATA_LSB	RO	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							
0x09	ANGLE_ROW	RO	ANGLE															
0x0A	SPEED_ROW	RO	SPEED															
0x0D	CTRL	RO	0	0	0	0	0	0	0	0	0	0	0	0	COMM_EN	-	-	SOFT_RST
0x0E	ERROR	ROC	IER	XEE	BSY	EUE	ESE	SME	TSE	VCF	TDE	POR	VCC	OFE	ICA	SPD	SAT	SPE
0x0F	TEMPERATURE_ROW	RO	TEMPERATURE															
0x10	X_EHC_ROW	RO	X_EHC															
0x11	Y_EHC_ROW	RO	Y_EHC															
0x12	ANGLE_HYST_ROW	RO	ANGLE_HYST															
0x1E	ACCESS	RO/WO	ACCESS_KEY		FREE_ REG_ LOCK_RD	FREE_ REG_ LOCK_WR	FACT	FACT	CUST_ REG_ LOCK_RD	CUST_ REG_ LOCK_WR	FACT	FACT	CUST_ EE_ LOCK_RD	CUST_ EE_ LOCK_WR	FACT	FACT	CUST_ ACCESS	FACT
0x1F	LOOPBACK_REG	RW	LOOPBACK															

Address 0x00 (NOP) – Null Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

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Address 0x01 (INDIRECT_WR_ADDRESS) Extended Write Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_ADDR [7:0]

Target address to be used for an extended memory write. Address ranges:

Extended 0x00 - 0x1F: EEPROM (requires ≈ 6 ms following execution of a write)

Extended 0x24 - 0x3F: Shadow (Volatile)

Extended 0x40 - 0x71: Miscellaneous (Volatile)

Address 0x02 (INDIRECT_WR_DATA_MSB) Extended Write Data Bytes High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_DATA_3 [15:8]

Upper fourth byte of data for an extended write operation, corresponds to bit [31:24] of the extended write address.

INDIRECT_WR_DATA_2 [7:0]

Third byte of data for an extended write operation, corresponds to bit [23:16] of the extended write address.

Address 0x03 (INDIRECT_WR_DATA_LSB) Extended Write Data Bytes Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_DATA_1 [15:8]

Second byte of data for an extended write operation, corresponds to bit [15:8] of the extended write address.

INDIRECT_WR_DATA_0 [7:0]

Lower first byte of data for an extended write operation, corresponds to bit [7:0] of the extended write address.

Address 0x04 (INDIRECT_WR_STATUS) Extended Write Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
Access	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EXW [15]

Initiates extended write by writing 1. Sets WIP, clears WDN. Write-only, always reads back 0.

WIP [8]

Indicates write in progress when set to 1.

WDN [0]

Write operation complete when to a value of 1, clears when EXW is set to 1.

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Address 0x05 (INDIRECT_RD_ADDRESS) Extended Read Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	INDIRECT_RD_ADDR							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_RD_ADDR [7:0]
Address to be used for an extended read. Address ranges:

Extended 0x00 - 0x1F: EEPROM (requires ≈ 2 µs)

Extended 0x24 - 0x3F: Shadow (Volatile)

Extended 0x40 - 0x71: Miscellaneous (Volatile)

Address 0x06 (INDIRECT_RD_STATUS) Extended Read Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
Access	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EXR [15]
Initiates extended read by writing 1. Sets RIP, clears RDN. Write-only, always reads back 0.

RIP [8]
Indicates read in progress when set to 1.

RDN [0]
Read operation complete when to a value of 1, clears when EXR is set to 1.

Address 0x07 (INDIRECT_RD_DATA_MSB) Extended Read Data Bytes High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

INDIRECT_RD_DATA_3 [15:8]
Upper fourth byte of data for an extended read operation, corresponds to bit [31:24] of the extended read address after execution of a read operation.

INDIRECT_RD_DATA_2 [7:0]
Third byte of data for an extended read operation, corresponds to bit [23:16] of the extended read address after execution of a read operation.

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Address 0x08 (INDIRECT_RD_DATA_LSB) Extended Read Data Bytes Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

INDIRECT_RD_DATA_1 [15:8]
Second byte of data for an extended read operation, corresponds to bit [15:8] of the extended read address after execution of a read operation.

INDIRECT_RD_DATA_0 [7:0]
Lower first byte of data for an extended read operation, corresponds to bit [7:0] of the extended read address after execution of a read operation.

Address 0x09 (ANGLE_ROW) Angle Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ANGLE[15:0]:
Register indicates the calculated angle from the RX1 (sin or Y channel) and the RX2 (cos or X channel) inputs. The parameter is a 16-bit unsigned integer with value of angle x 360/2^16 in degrees.

Address 0x0A (SPEED_ROW) Speed Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPEED															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

SPEED[15:0]:
Register indicates the calculated angular velocity. The parameter is a 16-bit signed integer.

Velocity in revolutions per minute can be calculated as:

Velocity[RPM] = uncomplement(speed[15:0]) × 14.3051

Accuracy of the velocity measurement is not quantified at final test and is not guaranteed by Allegro.

Address 0x0D (CTRL) Control register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	COMM_EN	-	-	SOFT_RST
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW

COMM_EN [3]:
Allows continuous R/W commands with the output being disabled without needing to overdriving the output pin.

SOFT_RST[0]:
Soft Reset. Writing at value of one to this bit triggers a full reset of the device logic, reset of all the status and error registers, reset of the signal processing, and reset of the outputs and communication protocols.

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Address 0x0E (ERROR) Device Error Flags

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IER	XEE	BSY	EUE	ESE	SME	TSE	VCF	TDE	POR	VCC	OFE	ICA	SPD	SAT	SPE
Access	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC

All errors in the register are latched, meaning they remain in a high logic state after they occurred until they are cleared. Errors clear after a read of the register and the error conditions no longer persist. An example is after a power on event the POR error flag is asserted a read of this register resets the POR error flag.

IER[15]: Interface Error Condition

XEE[14]: Extended Execute Error Condition

BSY[13]: Extended Access Busy Condition

EUE[12]: Shadow Memory Error. (Multiple Input Shift Register signature error)

ESE[11]: Multi-Bit EEPROM Error (uncorrectable)

SME[10]: Single Bit EEPROM Error (correctable)

TSE[9]: Temperature Error

VCF [8]: Voltage Check Failure Error

TDE [7]: Transmitting Signal/Driver Error

POR [6]: Power On Reset Event

VCC [5]: Overvoltage/Undervoltage Error

OFE [4]: Oscillator Frequency Error

ICA [3]: Input Signal Out of Range Error

SPD [2]: Maximum Speed Error

SAT [1]: Saturation Error

SPE [0]: Angle error

Address 0x0F (TEMPERATURE_ROW) Temperature

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEMPERATURE															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

TEMPERATURE[15:0]:
Current ambient temperature from the internal temperature sensor.
Temperature is coded as a 12-bit signed integer on the first 12 MSB (TEMPERATURE[15:3]).
To obtain the temperature reading in degrees Celsius the following equation is used:
Temperature (°C) ≈ uncomplemented(TEMPERATURE[15:3]) / 13.3226 + 25

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Address 0x10 (X_EHC_ROW) X_EHC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	X_EHC															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

X_EHC [15:0]:
Digital x channel register, corresponding to RX2 input (cosine input), after OGT, OGA, and electrical harmonic compensation. Value is used by the IC to calculate angle.

Address 0x11 (Y_EHC_ROW) Y_EHC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Y_EHC															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Y_EHC [15:0]:
Digital y channel register, corresponding to RX1 input (sine input), after OGT, OGA, and electrical harmonic compensation. Value is used by the IC to calculate angle.

Address 0x12 (ANGLE_HYST _ROW) Hysteresis Angle Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_HYST															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

ANGLE_HYST[15:0]:
Register indicates the angle with hysteresis applied. The parameter is a 16-bit unsigned integer with value of angle × 360 / 2^{16} in degrees.

Address 0x1E (ACCESS) Access Register

Writing to register 0x1E is a special command to enable access to the extended memory space, EEPROM and Volatile. See section Enabling EEPROM Access for more information.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														CUSTOMER_ ACCESS	RESERVED
Access	WO	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

CUSTOMER_ACCESS [1]
Bit indicates access to customer registers within the extended memory space. A logic value of 1 indicates access to the customer registers within the extended memory space is enabled.

Address 0x1F (LOOPBACK_REG) Loopback Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOOPBACK															
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

LOOPBACK [15:0]
Customer loopback register. The registers allow the external controller to perform a loopback test of the SPI communication between the controller and the peripheral A17802.

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EXTENDED MEMORY TABLE

EEPROM (NONVOLATILE), SHADOW (VOLATILE), AND MISCELLANEOUS (VOLATILE)

The EEPROM/Shadow register bitmap is shown below. All EEPROM and shadow contents can be read by the user, without unlocking. Writing requires a device unlock. The shadow memory is a copy of the EEPROM in the address range 0x24 to 0x3F.

Table 4: EEPROM/Shadow Memory Map

EEPROM Address	Shadow Address	Bits																											
		31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	N/A	ECC	factory reserved				FACTORY_DIE_ID																factory reserved					
0x01	N/A	ECC	factory reserved				FACTORY_LOT																FACTORY_WAFER					
0x02	N/A	ECC	CAS_ID																factory reserved									
0x03	N/A	ECC	CUSTOMER_ID																									
0x04 to 0x0F	0x24 to 0x29	factory reserved																										
0x10	0x30	ECC	D_TX_TC				N/A																					
0x11	0x31	ECC	OGA_FILT_DIS	OGT_X_GAIN_C												OGT_X_OFFSET_C												
0x12	0x32	ECC	OGA_ALL_DIS	OGT_Y_GAIN_C												OGT_Y_OFFSET_C												
0x13	0x33	ECC	N/A	N_AVG_CYCLES_OGA			EHC_X_H2_PHASE												EHC_X_H2_AMP									
0x14	0x34	ECC	N/A	N/A		ASC_BW	EHC_X_H3_PHASE												EHC_X_H3_AMP									
0x15	0x35	ECC	FE_SENS_TRIM				AGS_EN	EHC_X_H4_PHASE											EHC_X_H4_AMP									
0x16	0x36	ECC	SET_TO_ZERO	AGS_MAX_ROOM		AGS_RANGE_ROOM	EHC_Y_H2_PHASE												EHC_Y_H2_AMP									
0x17	0x37	ECC	N/A				EHC_Y_H3_PHASE												EHC_Y_H3_AMP									
0x18	0x38	ECC	D_TX_CK_PH_TRIM				EHC_HARM_WEIGHT_EN	EHC_Y_H4_PHASE											EHC_Y_H4_AMP									

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EEPROM Address	Shadow Address	Bits																										
		31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x19	0x39	ECC	FACTORY RESERVED																									
0x1A	0x3A	ECC	FACTORY RESERVED																									
0x1B	0x3B	ECC	N/A	ASC_QUAD_COMP										N/A					DEL_SYS_ABS									
0x1C	0x3C	ECC	TXDRV_TRIM							N/A		DEL_ZERO_ANGLE																DEL_ANGLE_POL
0x1D to 0x1E	0x3C to 0x3E	ECC	N/A																									
0x1F	0x3F	ECC	UNLOCK_CODE	BLOCK_VOLATILE_OUTPUT	MEM_LOCK				ASIL_EN	N/A		MANUFACTURER_CODE																N/A

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EEPROM

Address 0x0

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	factory reserved				FACTORY_DIE_ID																factory reserved					
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

FACTORY_ID [21:6]:
Identification number. When used in combination with FACTORY_LOT and FACTORY_WAFER, it creates a unique identification for device traceability. The register access is customer read only.

Address 0x1

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	factory reserved				FACTORY_LOT																FACTORY_WAFER					
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

FACTORY_LOT [21:6]:
Identification number. When used in combination with FACTORY_ID and FACTORY_WAFER, it creates a unique identification for device traceability. The register access is customer read only.

FACTORY_WAFER [5:0]:
Identification number. When used in combination with FACTORY_ID and FACTORY_LOT, it creates a unique identification for device traceability. The register access is customer read only.

Address 0x2

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAS_ID																factory reserved									
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

CAS_ID [25:10]:
Type identification number. May contain an identification number to distinguish a specific device configuration. The register access is customer read only.

Address 0x3

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CUSTOMER_ID																									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

CUSTOMER_ID [25:0]:
Customer identification number. The register space is open for customer write access. The contents of the register have no effect on the device operating modes. A common use for the register is to store a unique identification number written by the customer. The register access is customer read and write.

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Address 0x10

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D_TX_TC				N/A																					
Default	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

D_TX_TC[25:22]:
Determines temperature coefficient for transmitting current adjustment.

D_TX_TC (CODE)	TX_{TC} ($°C^{-1}$)
8	5.70×10^{-5}
9	5.46×10^{-4}
10	1.02×10^{-3}
11	1.49×10^{-3}
12	1.94×10^{-3}
13	2.39×10^{-3}
14	2.82×10^{-3}
15	3.24×10^{-3}
0	3.66×10^{-3}
1	4.06×10^{-3}
2	4.46×10^{-3}
3	4.85×10^{-3}
4	5.23×10^{-3}
5	5.60×10^{-3}
6	5.96×10^{-3}
7	6.32×10^{-3}

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Address 0x11

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OGA_FILT_DIS	OGT_X_GAIN_C												OGT_X_OFFSET_C												
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

OGA_FILT_DIS[25]:
Disables filtering in OGA correction update.

OGT_X_GAIN_C[24:13]:
Gain correction coefficient for x digital channel (RX2), represented in 12-bit signed fixed-point number with 13-bit fractional length. It can compensate ±25% gain mismatch with steps of 0.0122%.

OGT_X_OFFSET_C[12:0]:
Offset correction for x digital channel (RX2), represented in 13-bit signed fixed-point number with 16-bit fractional length. It can compensate ±6.25% ADC range at minimum AGS gain with steps of 0.001526%.

Address 0x12

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OGA_ALL_DIS	OGT_Y_GAIN_C												OGT_Y_OFFSET_C												
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

OGA_ALL_DIS [25]:
Disable Offset and Gain Autocalibration (OGA) algorithm.

OGT_Y_GAIN_C [24:13]:
Gain correction coefficient for y digital channel (RX1), represented in 12-bit signed fixed-point number with 13-bit fractional length. It can compensate ±25% gain mismatch with step of 0.0122%.

OGT_Y_OFFSET_C [12:0]:
Offset correction for y digital channel (RX1), represented in 13-bit signed fixed-point number with 16-bit fractional length. It can compensate ±6.25% ADC range at minimum AGS gain with steps of 0.001526%.

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Address 0x13

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A	N_AVG_CYCLES_OGA				EHC_X_H2_PHASE											EHC_X_H2_AMP									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

N_AVG_CYCLES_OGA [24:21]:

Number of electrical cycles for OGA algorithm. Code 0 corresponds to value of 16. Value shall be set to be largest multiple of number of target teeth and sensor periods ≤ 16, according to table below.

Number of target teeth/ sensor electrical periods	N_AVG_CYCLES_OGA (code)
1	0
2	0
3	15
4	0
5	15
6	12
7	14
8	0
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	0

EHC_X_H2_PHASE [20:10]:

Phase value of 2nd electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_X_H2_AMP [9:0]:

Amplitude value of 2nd electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

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Address 0x14

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	N/A	N/A		ASC_ BW		EHC_X_H3_PHASE											EHC_X_H3_AMP									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ASC_BW [22:21]:
Sets bandwidth for angle and speed calculation control loop. It shall be set to 0 for all ASIL applications.

ASC_BW	–3 dB BW (kHz)
0	1.19
1	1.95
2	4.97
3	8.54

EHC_X_H3_PHASE [20:10]:
Phase value of 3rd electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_X_H3_AMP [9:0]:
Amplitude value of 3rd electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

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Address 0x15

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FE_SENS_TRIM				AGS_EN	EHC_X_H4_PHASE											EHC_X_H4_AMP									
Default	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

FE_SENS_TRIM[25:22]:
It sets the gain of front-end amplifier if automatic gain adjustment is disabled (AGS_EN = 0).

Value	FE amplifier Gain (V/V)
0	8
1	16
2	24
3	32
4	40
5	48
6	56
7	64
8	72
9	80
10	88
11	96
12	104
13	112
14	120
15	128

AGS_EN [21]:
Enables automatic gain selection (AGS) algorithm to determine optimal front-end gain at start-up. When clear, front-end gain is determined by FE_SENS_TRIM value.

EHC_X_H4_PHASE[20:10]:
Phase value of 4th electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_X_H4_AMP[9:0]:
Amplitude value of 4th electrical harmonic for x signal channel (RX2). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

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Address 0x16

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SET_TO_ZERO	AGS_MAX_ROOM		AGS_RANGE_ROOM		EHC_Y_H2_PHASE											EHC_Y_H2_AMP									
Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

SET_TO_ZERO[25]:

Shall always be set to 0 for correct TX drive operations.

AGS_MAX_ROOM [24:23]:

Reduces the used input range for the front-end ADC to give room for offset or mechanical input modulation. Value is used in AGS algorithm to determine optimal FE gain.

Value	ADC input room
0	0 mV
1	5 mV
2	15 mV
3	20 mV

AGS_RANGE_ROOM[22:21]:

Reduces the used input range of the front-end ADC. Value is used in AGS algorithm to determine optimal FE gain.

Value	ADC input range reduction
0	0%
1	10%
2	15%
3	20%

EHC_Y_H2_PHASE[20:10]:

Phase value of 2nd electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_Y_H2_AMP[9:0]:

Amplitude value of 2nd electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

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Address 0x17

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED					EHC_Y_H3_PHASE											EHC_Y_H3_AMP									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

EHC_Y_H3_PHASE [20:10]:
Phase value of 3rd electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_Y_H3_AMP [9:0]:
Amplitude value of 3rd electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

Address 0x18

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D_TX_CK_PH_TRIM				EHC_HARM_WEIGHT_EN	EHC_Y_H4_PHASE											EHC_Y_H4_AMP									
Default	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

D_TX_CK_PH_TRIM [25:22]:
Modifies demodulation clock phase. It shall be kept to default values for standard operation. It can be calibrated for special targets such as steel. Value is represented as signed integer on 4 bits, coded in 2's complement. Code 8 corresponds to min value (–8), code 7 corresponds to max value (+7). Each step correspond to approximately 5°.

EHC_HARM_WEIGHT_EN [21]:
Enables electrical harmonic compensations term scaling with input amplitude. Shall be kept to 1 for normal operation.

EHC_Y_H4_PHASE [20:10]:
Phase value of 4th electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 11-bit unsigned fixed-point number with 11-bit fractional length. Value range is normalized to 1 and corresponds to 0 to 360 degrees with 0.176 degrees step.

EHC_Y_H4_AMP [9:0]:
Amplitude value of 4th electrical harmonic for y signal channel (RX1). Used in electrical harmonic compensation algorithm. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate 6.25% second harmonic amplitude referred to first electrical harmonic amplitude with steps of 0.0061%.

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Address 0x1B

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED	ASC_QUAD_COMP										N/A					DEL_SYS_ABS									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ASC_QUAD_COMP [24:15]:

Compensates deviation from quadrature between y (RX1) and x (RX2) digital channels before angle calculation. Value is represented in 10-bit unsigned fixed-point number with 14-bit fractional length. It can compensate ±11.25 degrees with steps of 0.022 degrees.

DEL_SYS_ABS [9:0]:

Additional system delay to be used for delay compensation when calculating angle. Value is represented in 10-bit signed number. It can compensate ±256 µs with steps of 0.5 µs.

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Address 0x1C

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXDRV_TRIM							N/A		DEL_ZERO_ANGLE																DEL_ANGLE_POL
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

TXDRV_TRIM[25:19]:

Sets tail current for transmitting oscillator according to table below. Resulting oscillation amplitude depends on external LC tank circuit characteristics: amplitude increasing from value 0 (minimum amplitude) to 127 (maximum amplitude).

TXDRV_TRIM	I_{TX} (mA)	TXDRV_TRIM	I_{TX} (mA)	TXDRV_TRIM	I_{TX} (mA)	TXDRV_TRIM	I_{TX} (mA)	TXDRV_TRIM	I_{TX} (mA)	TXDRV_TRIM	I_{TX} (mA)	TXDRV_TRIM	I_{TX} (mA)
0	0.125	20	0.280	40	0.552	60	1.010	80	2.203	100	4.078	120	8.116
1	0.131	21	0.287	41	0.571	61	1.029	81	2.257	101	4.240	121	8.276
2	0.137	22	0.293	42	0.589	62	1.047	82	2.312	102	4.402	122	8.438
3	0.144	23	0.299	43	0.607	63	1.065	83	2.366	103	4.564	123	8.598
4	0.156	24	0.311	44	0.644	64	1.104	84	2.476	104	4.888	124	8.919
5	0.162	25	0.318	45	0.662	65	1.159	85	2.531	105	5.050	125	9.079
6	0.169	26	0.324	46	0.681	66	1.214	86	2.586	106	5.212	126	9.240
7	0.175	27	0.330	47	0.699	67	1.269	87	2.641	107	5.374	127	9.400
8	0.187	28	0.343	48	0.736	68	1.379	88	2.750	108	5.697		
9	0.193	29	0.349	49	0.754	69	1.434	89	2.805	109	5.859		
10	0.200	30	0.355	50	0.772	70	1.488	90	2.859	110	6.021		
11	0.206	31	0.361	51	0.791	71	1.543	91	2.914	111	6.182		
12	0.218	32	0.369	52	0.827	72	1.653	92	3.023	112	6.505		
13	0.225	33	0.387	53	0.846	73	1.708	93	3.078	113	6.666		
14	0.231	34	0.405	54	0.864	74	1.763	94	3.133	114	6.827		
15	0.237	35	0.424	55	0.882	75	1.818	95	3.188	115	6.989		
16	0.249	36	0.461	56	0.919	76	1.928	96	3.266	116	7.311		
17	0.256	37	0.479	57	0.937	77	1.983	97	3.428	117	7.472		
18	0.262	38	0.497	58	0.955	78	2.038	98	3.591	118	7.634		
19	0.268	39	0.516	59	0.974	79	2.093	99	3.753	119	7.794		

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DEL_ZERO_ANGLE [16:1]:
Offsets the output angle of a value between 0 and 360 degrees in 65536 steps. Angle output is equal to calculated angle plus DEL_ ZERO_ANGLE × 360 / 65536.

DEL_ANGLE_POL [0]:
Defines the angle polarity. 0: Forward, increasing angle when x (RX2 envelop) leads y (RX1 envelop). 1. Reversed polarity, angle decreasing when x (RX2 envelop) leads y (RX1 envelop).

Address 0x1F

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNLOCK_CODE	BLOCK_VOLATILE_OUTPUT	MEM_LOCK				ASIL_EN	N/A		MANUFACTURER_CODE												N/A				
Default	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

UNLOCK_CODE[25]:
Determines if an extra unlock code is needed before writing access code as described in section EEPROM and Shadow Memory Usage. When UNLOCK_CODE = 0 the extra unlock code is not needed. When UNLOCK_CODE = 1 an unlock code in addition of the access code needs to be sent to access memory.

BLOCK_VOLATILE_OUTPUT [24]:
Controls write access to volatile memory. When set, write operations to volatile memory are disabled.

It shall be set for ASIL applications.

MEM_LOCK [23:20]:
Defines protection for memory access as described in section EEPROM and Shadow Memory Usage.

ASIL_EN [19]:
Enables error reporting. It shall be set for ASIL applications.

MANUFACTURER_CODE [16:5]:
Bits available for customer purposes.

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VOLATILE MEMORY MAP

Address 0x42

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							EE_DBE_FLAG	EE_SBE_FLAG	EE_ECC						EE_ADDR					EE_ERR_STATUS					CP_ERR	EE_ERR
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RC	RC

EE_DBE_FLAG [19]:

Error flag indicates detection of an EEPROM dual-bit error. The EEPROM ECC logic detects an address with a dual-bit error. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM dual bit error detected
1	EEPROM dual bit error detected

EE_SBE_FLAG [18]:

Error flag indicates detection of an EEPROM single-bit error. The EEPROM ECC logic detects an address with a single-bit error. The ECC logic automatically corrects the faulty bit in the volatile region of memory. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM single-bit error detected
1	EEPROM single-bit error detected

EE_ECC [17:12]:

EEPROM ECC data. After the internal margin test is complete, this parameter contains the ECC data bits of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x44 [4:3]) for margin results information.

EE_ADDR [11:7]:

EEPROM address data. After the internal margin test is complete, this parameter contains the address of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x44 [4:3]) for margin results information.

EE_ERR_STATUS [6:2]:

Indicates the error status of the last EEPROM write. If logic > 0, an error was detected during the last EEPROM write.

CP_ERR [1]:

Indicates the error status of the EEPROM write charge pump during the last EEPROM write. If logic = 1, an error is detected, and the error is set in EE_ERR_STATUS (extended: 0x42 [6:2]).

EE_ERR [0]:

Indicates detection of an EEPROM write error. If logic = 1, an EEPROM write error is detected. The bit clears after read.

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Address 0x43

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EE_DATA																									
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EE_DATA [25:0]:
EEPROM field data. After the internal margin test is complete, this parameter contains information from the data fields of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x44 [4:3]) for margin results information.

Address 0x44

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	EE_LOOP	EE_TEST_ADDR					EE_USE_TEST_ADDR	MARGIN_MIN_MAX_FAIL	MARGIN_STATUS		MARGIN_NO_MIN	MARGIN_NO_MAX	MARGIN_START
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RO	RO	RO	RW	RW	RW

EE_LOOP [12]:
Continuously loops the margin test. When bit logic = 1, the margin test loops continuously. If an error is detected or if MARGIN_START (extended: 0x44 [0]) is cleared, the margin test stops.

Value	Description
0	Margin test runs once
1	Margin test loops continuously until an error is detected

EE_TEST_ADDR [11:7]:
Optional start address for margin test. Defines the starting address for the margin test when EE_USE_TEST_ADDR (extended: 0x44[6]) is set to logic = 1.

EE_USE_TEST_ADDR [6]:
When set to logic = 1, the margin test starts at the address defined by EE_TEST_ADDR (extended: 0x44 [12:7]).

Value	Description
0	Margin test starts at address 0x0
1	Margin test starts at address defined by EE_TEST_ADDR

MARGIN_MIN_MAX_FAIL [5]:
If a margin failure is detected, this bit indicates if the failure was detected at the minimum or maximum reference level.

Value	Description
0	Margin test failure detected at minimum threshold
1	Margin test failure detected at maximum threshold

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MARGIN_STATUS [4:3]:
Indicates the status of the margin test. The bits clear after a read or reset event.

Value	Description
0	Reset condition: No result from margin test
1	Pass: No errors detected during margin test
2	Fail: Error detected during margin test
3	In progress: Margin test still running

MARGIN_NO_MIN [2]:
Disables the minimum reference level during margin test. When set to logic = 1, the margin test does not check for errors at the low reference level.

Value	Description
0	Margin test includes check at the low reference level
1	Margin test does not include check at the low reference level

MARGIN_NO_MAX [1]:
Disables the maximum reference level during margin test. When set to logic = 1, the margin test does not check for errors at the high reference level.

Value	Description
0	Margin test includes check at the high reference level
1	Margin test does not include check at the high reference level

MARGIN_START [0]:
Triggers start of margin test. When set to LOGIC = 1, the margin test begins. The bit clears when the margin test completes and EE_LOOP (extended: 0x44 [13]) = 0; if EE_LOOP = 1, the margin test runs until MARGIN_START = 0. If the margin test detects an error, the MARGIN_START bit clears.

Address 0x47

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																								LBIST_PASS1_FAIL0	BIST_DONE	BIST_START
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RC	RO	RW

LBIST_PASS1_FAIL0 [2]:
Indicates pass or fail result of LBIST (logic built-in self test).

Value	Description
0	Indicates a fail result from the LBIST
1	Indicates a pass result from the LBIST

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BIST_DONE [1]:
Indicates BIST (built-in self test) is complete.

Value	Description
0	Indicates BIST is in progress, BIST did not execute, or BIST was aborted.
1	Indicates BIST is complete.

BIST_START [1]:
Initiates start of BIST. Bit is set to a logic value of one to initiate the start of LBIST. The bit self clears when LBIST is started. LBIST requires ≈105 ms to run. Angle is not available during LBIST.

Value	Description
0	Indicates LBIST is in progress or result not available.
1	Indicates BIST is complete.

Address 0x51

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																D_TX_AMP_TRIM							D_FE_SENS			
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

D_TX_AMP_TRIM [10:4]:
In use current trim code for oscillator driver.

D_FE_SENS [3:0]:
In use front-end gain code.

Address 0x5B

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										OGA_Y_GAIN_COEFF																
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_Y_GAIN_COEFF [16:0]:
Gain coefficient applied on y channel by OGA algorithm. Value is unsigned on 17 bit, with 13-bit fractional length.

Address 0x5C

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OGA_Y_OFFSET_COEFF																	
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_Y_OFFSET_COEFF [17:0]:
Offset correction applied on y channel by OGA algorithm. Value is signed on 18 bit, with 17-bit fractional length.

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Address 0x5D

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										OGA_X_GAIN_COEFF																
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_X_GAIN_COEFF [16:0]:
Gain coefficient applied on x channel by OGA algorithm. Value is unsigned on 17 bit, with 13-bit fractional length.

Address 0x5E

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OGA_X_OFFSET_COEFF																	
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_X_OFFSET_COEFF[17:0]:
Offset correction applied on x channel by OGA algorithm. Value is signed on 18 bit, with 17-bit fractional length.

Address 0x5F

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										OGA_X_REF_AMPLITUDE																
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_X_REF_AMPLITUDE[16:0]:
Calculated reference amplitude for x channel for OGA algorithm. Value is an unsigned integer on 17 bits.

Address 0x60

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OGA_X_REF_OFFSET																	
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_X_REF_OFFSET[17:0]:
Calculated reference offset for x channel for OGA algorithm. Value is a signed integer on 18 bits, with 17-bit fractional length.

Address 0x61

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										OGA_Y_REF_AMPLITUDE																
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_Y_REF_AMPLITUDE[16:0]:
Calculated reference amplitude for y channel for OGA algorithm. Value is an unsigned integer on 17 bits, with 17-bit fractional length.

Address 0x62

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									OGA_Y_REF_OFFSET																	
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

OGA_Y_REF_OFFSET[17:0]:
Calculated reference offset for y channel for OGA algorithm. Value is a signed integer on 18 bits.

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POWER DERATING

The A17802 must operate below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the A17802 to dissipate heat from the junction (die) through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D) can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: $T_A = 25°C$, $V_{CC} = 5$ V, $I_{CC} = 25$ mA, and $R_{\theta JA} = 82°C/W$, then:

$$P_D = V_{CC} \times I_{CC} = 125 \text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 125 \text{ mW} \times 82°C/W = 10.25°C$$

$$T_J = T_A + \Delta T = 25°C + 10.25°C = 35.25°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)} \times I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at $T_A = 160°C$, package LE.

Observe the case with a total current $I_{CC(tot)} = I_{CC(max)} + I_{CC(TX)} = 23$ mA + 9 mA = 32 mA and the worst-case ratings for the device, specifically: $R_{\theta JA} = 82°C/W$, $T_{J(max)} = 175°C$, $V_{CC(max)} = 5.5$ V.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 175°C - 160°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 82°C/W = 183 \text{ mW}$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)}$$
$$= 183 \text{ mW} \div 32 \text{ mA}$$
$$= 5.72 \text{ V}$$

The result indicates that, at T_A, the application and A17802 with a TX equivalent DC current of 9 mA can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$. TX currents larger than 9 mA might require power derating.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then a reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these condition.

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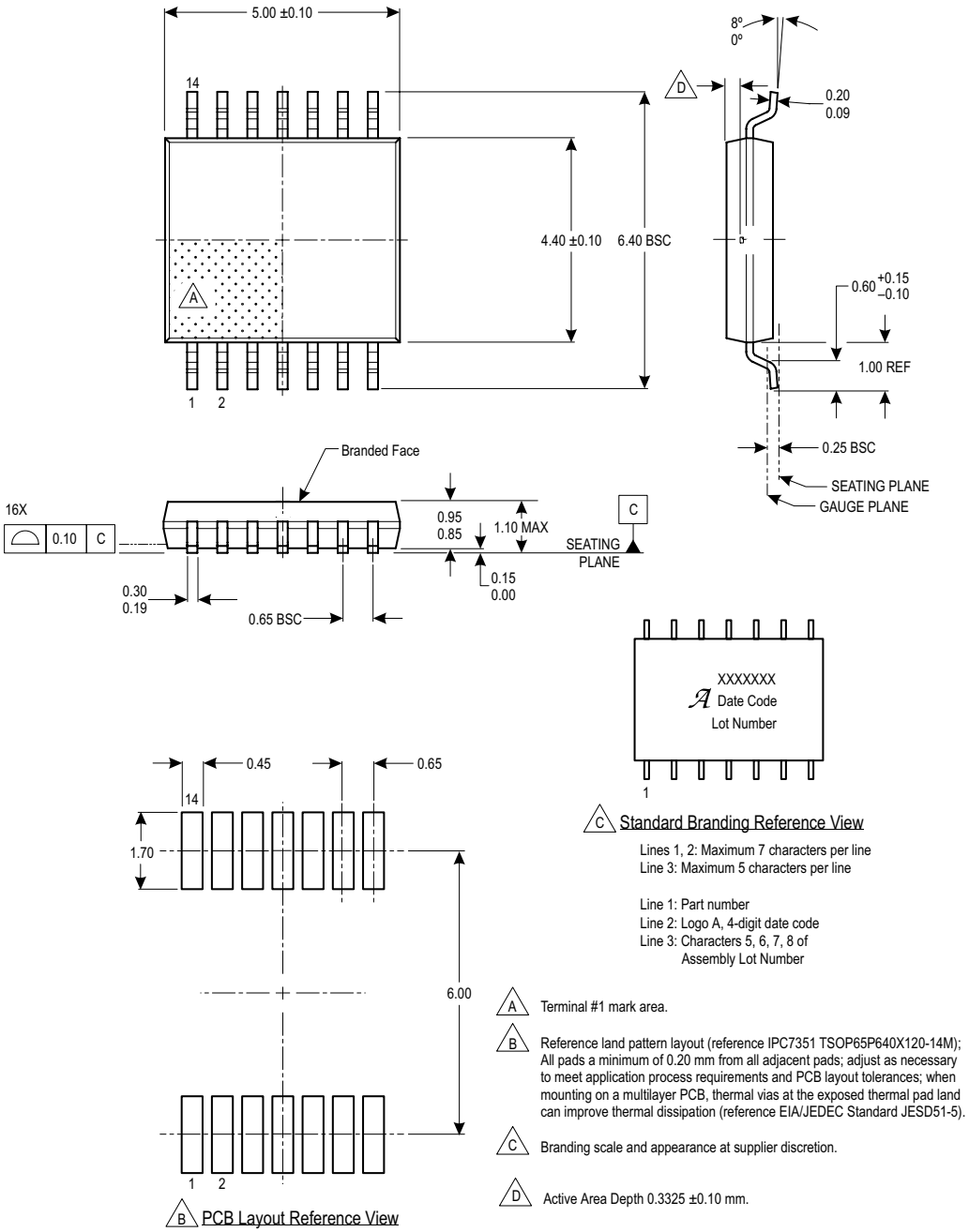
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 AB-1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area.

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-14M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

C Branding scale and appearance at supplier discretion.

D Active Area Depth 0.3325 ±0.10 mm.

Figure 22: 14-Pin TSSOP Package

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REVISION HISTORY

Number	Date	Description
–	March 13, 2025	Initial release
1	March 21, 2025	Added ASIL logos; added footnote to Output Signal Delay (page 6)

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