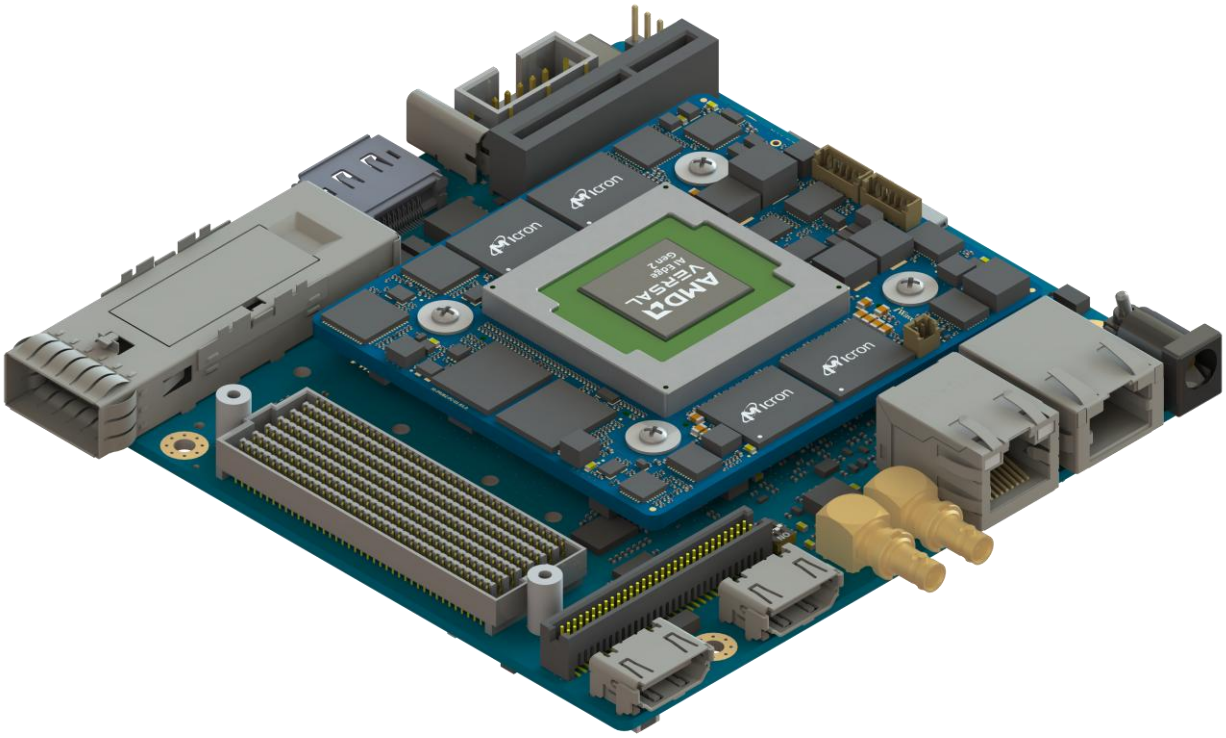
iG-RainboW-G77D

Versal AI Edge Gen2 SOM Development Platform

Hardware Datasheet



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1. INTRODUCTION

1.1 Purpose

The Versal AI Edge Gen2 SOM Development platform incorporates Versal AI Edge Gen2 based SOM and REN development board for complete validation of Versal AI Edge Gen2 functionality. This document is the Hardware User Guide for the Versal AI Edge Gen2 development Board and provides detailed information on the overall design & usage of the development Board from a Hardware Systems perspective. The details about the Versal AI Edge Gen2 SOM hardware are explained in another document “iG-RainboW-G77M- Versal AI Edge Gen2-SOM-Datasheet”.

1.2 Overview

iWave's Versal AI Edge Gen2 Development platform comes with Versal AI Edge Gen2 SOM and the REN development Board. The development board can be used for quick prototyping of various applications targeted by the Versal AI Edge Gen2. With the 120mm x 120mm size, development board is packed with all the necessary on-board connectors to validate the features of Versal AI Edge Gen2 SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
B2B	Board To Board
CPU	Central Processing Unit
CAN	Controller Area Network
eMMC	Embedded Multimedia Card
FPGA	Field Programmable Gate Array
FMC+	FPGA Mezzanine Card Plus
GEM	Gigabit Ethernet Controller
GB	Giga Byte
Gbps	Gigabits per sec
GHz	Giga Hertz
GPIO	General Purpose Input Output
HDMI	High-Definition Multimedia interface
HS	High Speed
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LPDDR5	Low Power Double Data Rate fifth-generation
LVDS	Low Voltage Differential Signaling
MAC	Media Access Controller
Mbps	Megabits per sec
MHz	Mega Hertz

Acronyms	Abbreviations
SoC	System On Chip
SOM	System On Module
SD	Secure Digital
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PMIC	Power Management Integrated Circuit
PMOD	Peripheral Module Interface
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SDI	Serial Digital Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

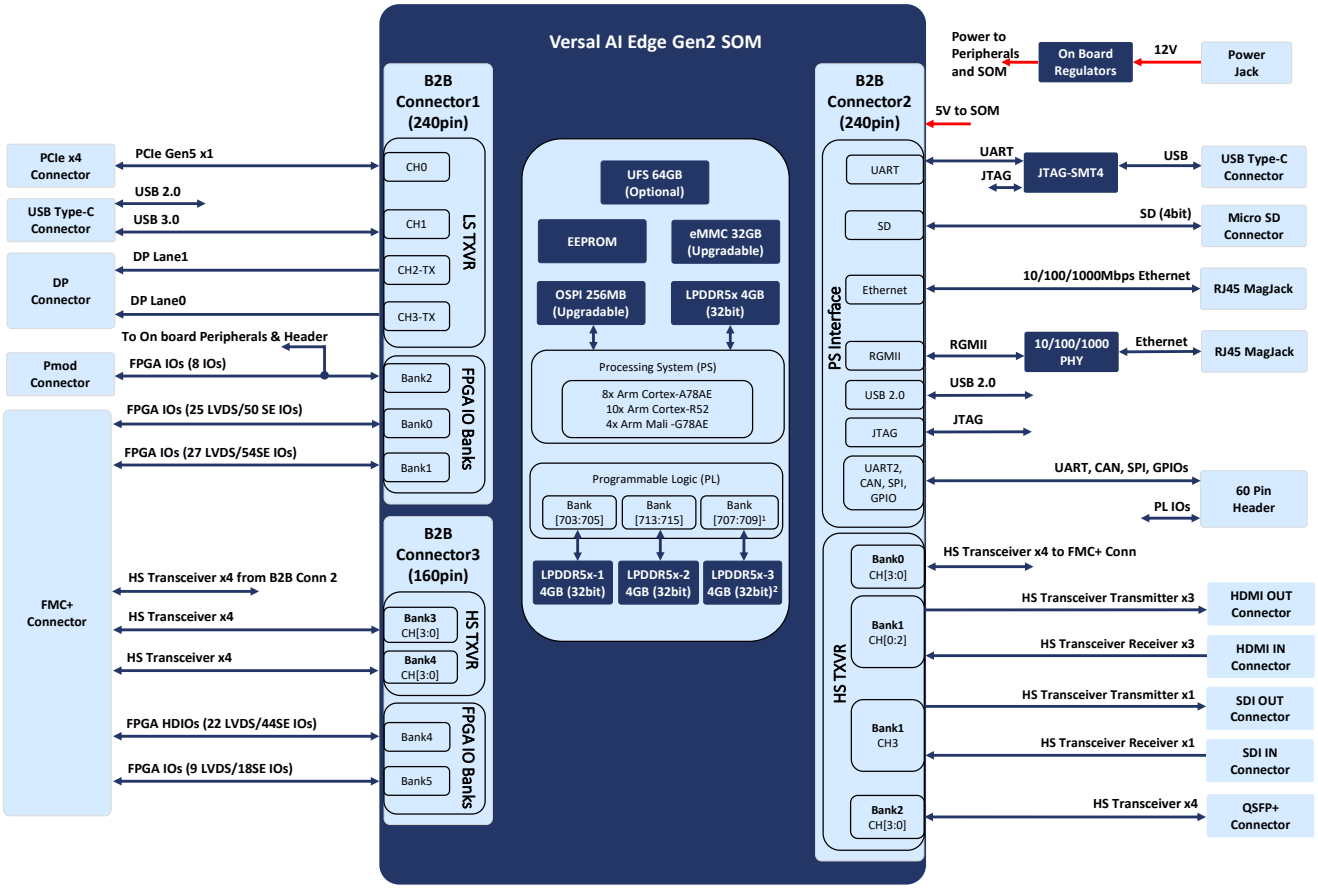
1.5 References

- Versal AI Edge Gen2 Datasheet & Reference Manual
- Versal AI Edge Gen2 SOM Hardware Datasheet

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Versal AI Edge Gen2 SOM Development board features with high level block diagram and detailed information about each block.

2.1 Versal AI Edge Gen2 SOM Development Board Block Diagram



Note:
[1] X5IO Bank 707 only supported in 2VE3858 & 2VE3804 devices
[2] LPDDR5x-3 only supported in 2VE3858 & 2VE3804 devices

Figure 1: Versal AI Edge Gen2 SOM development Board Block Diagram

2.2 Versal AI Edge Gen2 SOM Development Board Features

Versal AI Edge Gen2 SOM based development board supports the following features to validate the Versal AI Edge Gen2 SOM supported interfaces.

Versal AI Edge Gen2 SOM features

SoC

- Versal AI Edge Gen2 SoC with SSVA2112 package
- Compatible with 2VE3858, 2VE3804, 2VE3558, 2VE3504 devices
  - **Processing System**
    - Arm Cortex-A78AE Application processor (up to 1.875GHz)
    - Arm Cortex-R52 Real Time Processor (up to 875MHz)
    - Arm Mali -G78AE with 4-core Graphics Processing Unit
    - Supports High Speed Interfaces like PCI Express Gen5 x4, USB 3.2, DisplayPort 1.4, 10G Ethernet
  - **Programmable System**
    - System Logic cells up to 1,188K Logic cells
    - LUTs up to 543K and DSP Engines up to 2,064
    - Supports AI Engine-ML v2 up to 144 Tiles
    - Supports 100G Multirate Ethernet MAC and PLPCIE5 Gen5 for high-speed connectivity
    - GTYP High speed Transceivers up to 32Gbps

Memory Interfaces

- 32bit 4GB LPDDR5x for PS (Expandable)
- Three 32bit 4GB LPDDR5x for PL (Expandable)[1]
- 32GB eMMC Flash (Expandable)
- 256MB OSPI Flash
- 4Kbit EEPROM
- 64GB UFS Flash (Optional)[2]

Power

- Renesas/Dialog's DA9062 PMIC and other discrete regulators

Features Supported Through Board-to-Board Connectors

PL Interface Features

- QSFP+ Connector
- HDMI IN/ OUT Connector
- SDI IN/OUT Connector
- PMOD Connector
- FMC+ Connector
  - 12 GTYP High Speed Transceivers Channels
  - 3 GTYP Reference Clock
  - 61LVDS /122 Single ended (SE) IOs from X5IO Bank
  - 22LVDS /44 Single ended (SE) IOs from HDIO Bank

PS Interface Features

- PS-GTYP PCIe Gen5 x1 interface through PCIe x4 Connector
- USB 3.0 & USB2.0 OTG through Type-C Connector
- Display Port Connector x2 lanes
- USB Type-C for Debug UART and JTAG
- 1GbE RJ45 MagJack Connector
- On-board Gigabit Ethernet PHY with RJ45 MagJack Connector
- Micro SD Connector

Additional Features

- Clock Synthesizers/Generators x2
- 16-Bit IO Expanders x2
- I2C Bus Switch x1
- DIP Switch
- User LEDs
- Configuration Done & Power LEDs
- Power ON/OFF Switch x1
- RTC Coin Cell Holder x1
- Reset Button
- GPIO Header (CAN, SPI, I2C, PL-IOs)

General Specification

- Power Supply : DC 12V, 5A Power Input
- Form Factor : 120mm X 120mm

Important Note:

1. *Throughout this document, the PL IO Bank name and pin name are provided as per the 2VE3858 device. Please refer to the Versal AI Edge Gen2 SOM Datasheet's* ***Bank Migration in Board-to-Board Connectors*** *section for further details regarding bank migration among supported FPGA devices.*
2. *In Versal AI Edge Gen2 SOM, all the transceivers' channels and all PL IOs pair's P & N (Intra pair) are length matched considering internal 2VE3858 device pin package delay.*

2.3 Versal Adaptive SoC

AMD Versal™ adaptive SoCs combine Scalar Engines, Adaptable Engines, and Intelligent Engines with leading-edge memory and interfacing technologies to deliver powerful heterogeneous acceleration for any application The Versal portfolio is the first to combine software programmability and domain-specific hardware acceleration with the adaptability necessary to meet today's rapid pace of innovation. The portfolio includes six series of devices uniquely architected to deliver scalability and AI inference capabilities for a host of applications across different markets—from cloud—to networking—to wireless communications—to edge computing and endpoints. The Versal architecture combines different engine types with a wealth of connectivity and communication capability and a programmable network on chip (NoC) to enable seamless memory-mapped access to the full height and width of the device.

The Versal AI Edge Gen2 series provides breakthrough heterogeneous integration, very high-performance compute, connectivity, and security in an adaptable platform with a minimized power and area footprint. The series is designed to exceed the demands of high-bandwidth, compute-intensive applications in wired communications, data centre, test & measurement, and other applications. The Versal AI Edge Gen2 series include PCI Express® Gen5, 100G Multirate Ethernet MAC, AI Engine-ML v2 and high-speed cryptography.

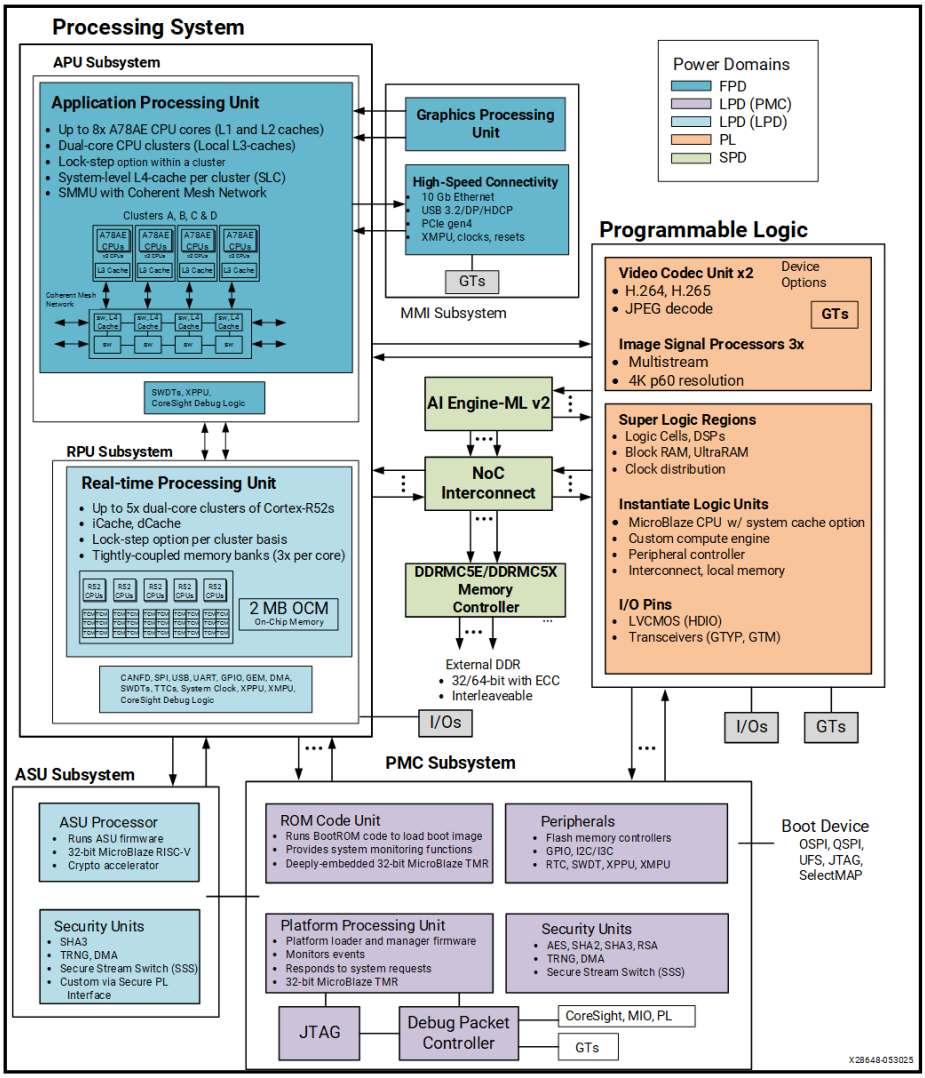


Figure 2: Versal AI Edge Gen2 Simplified Block Diagram

The Versal AI Edge Gen2 SOM is compatible to 2VE3858, 2VE3804, 2VE3558, 2VE3504 SoC of SSVA2112 package devices and feature comparison between these devices are shown below.

	2VE3858	2VE3804	2VE3558	2VE3504
AI Engine-ML v2 Tiles	144	144	96	96
AIE-ML v2 Data Memory (Mb)	72	72	48	48
AIE-ML v2 Shared Memory (Mb)	288	288	96	96
APU	Arm® Cortex®-A78AE, 64 KB I w/parity & D w/ECC L1 Cache, 512 KB L2 Cache, 1 MB L3 Cache (per 2-core cluster), CMN600 w/4 MB Last-Level Cache			
RPU	Arm Cortex-R52, 32 KB L1 Cache w/ECC, 128 KB TCM w/ECC			
High-Speed Connectivity	PCI Express® Gen5 x4(1), USB 3.2, DisplayPort 1.4, 10G Ethernet, 1G Ethernet, UFS 3.1			
System Logic Cells	11,88,040	11,88,040	4,92,188	4,92,188
LUTs	5,43,104	5,43,104	2,25,000	2,25,000
DSP Engines	2,064	2,064	700	700
NoC Master / Slave Ports	24	24	7	7
Distributed RAM (Mb)	16.6	16.6	6.9	6.9
Total Block RAM (Mb)	47.2	47.2	13.6	13.6
UltraRAM (Mb)	33.2	33.2	3.4	3.4
Total PL Memory (Mb)	97	97	23.9	23.9
GPU (4-core Arm Mali -G78AE)	1	1	1	1
Video Codec Unit (VCU)	1	-	1	-
Image Signal Processor	3	-	3	-
PCI Express (PLPCIE5)	4 x Gen5 x4	4 x Gen5 x4	3 x Gen5 x4	3 x Gen5 x4
100G Multirate Ethernet MAC	3	3	1	1
X5IO	172	172	122	122
HDIO	44	44	44	44
PS-GTYP Transceivers (32Gb/s)	4	4	4	4
PL-GTYP Transceivers (32Gb/s)	20	20	12	12

Figure 3: Versal AI Edge Gen2 SoC Devices Comparison

The Versal AI Edge Gen2, Processing System (PS) supports a total 78 dedicated I/O pins referred as MIO (Multiplexed I/O) for peripheral interfaces. These 78 MIO pins are divided as Platform Management Controller (PMC) and Low Power Domain (LPD). The PMC supports total 52 MIO with BANK 500 & 501 and each bank include 26 device pins. The LPD supports a 26 MIO with Bank 502 and this bank also includes a 26 MIO pins. 78 MIO pins are not enough to support simultaneous use of all the peripherals supported by PS, there is option in Versal to route IO peripheral interfaces to PL Bank I/O pins referred as EMIO (Extended MIO). Versal AI Edge Gen2 PS peripheral pin mapping options between MIO & EMIO is shown below. The Versal AI Edge Gen2 supports Video and Imaging IP's, with 4-core Arm Mali -G78AE graphics processing unit, up to 1 Video Codec Unit and up to 3 Image Signal Processor.

The AMD Versal adaptive SoCs combine scalar engines, adaptable engines, and intelligent engines with leading-edge memory and interfacing technologies to deliver powerful heterogeneous acceleration for any application. This Versal AI Edge Gen2 consist of AIE-ML v2 up to 144 Tiles containing 512 KB of high-density, high-bandwidth memory.

Table 3:MIO and EMIO Pin Mapping Table

Peripheral Interface	Controller Location	PMC MIO	LPD MIO	EMIO	Notes
CAN_FD 0,1	LPD	Yes	Yes	Yes	-
GEM 0,1	LPD	Yes	Yes	-	RGMII
		-	-	Yes	GMII/MII, TSU, and external FIFO
		Yes	Yes	Yes	MDIO
LPD DMA	LPD	-	-	YES	Flow control
PMC_GPIO	PMC	Yes	-	-	Bank 0,1 (no Bank 2)
		-	-	Yes	BANK 3,4
LPD_GPIO	LPD	-	Yes	-	LPD GPIO BANK 0 (no Bank 1,2)
		-	-	Yes	LPD GPIO Bank 3
LPD_I3C 0,1	LPD	Yes	Yes	Yes	-
SYSMON_I2C	PMC	Yes	-	Yes	-
Octal SPI	PMC	Yes		-	-
SelectMAP	PMC	Yes	-	-	-
SPI 0, 1	LPD	Yes	Yes	Yes	-
Quad SPI	PMC	Yes	-	-	-
CoreSight™ Trace Out	FPD	16-bit	16-bit	32-bit	-
TTC 0,1,2,3	LPD	Yes	Yes	Yes	Clock in and wave out
TTC 4,5,6,7	LPD				
UART 0,1	LPD	Yes	Yes	Yes	MIO only includes RX, TX, CTS, and RTS
USF	PMC	Yes	-	-	Includes GTs for I/O
USB_2.0	LPD	Yes	-	-	ULPI PHY interface
RPU_A_SWDT	LPD	Yes	-	Yes	Interrupt signal only (INT)

The Versal AI Edge Gen2 PL Banks are classified as Xtreme Performance (X5) banks or high-density (HD) banks. The X5 Bank IO's are optimized for highest performance operation organized in a bank of 710, 711, 712, 713, 706 & 707. Each X5IO bank contains a 16 LVDS / 32 SE pins. The HD Bank I/O's are reduced-feature I/O's organized in a bank of 400 and 402 with 44 SE pins.

In Versal AI Edge Gen2, each X5IO bank supports one Global Clock (GC) input pin pairs. GC pins have direct access to the global clock buffers, MMCMs and DPLLs of the same Bank. The HD bank supports a two High Density Global Clock (HDGC) input pin pair and have direct access only to the DPLL.

Versal AI Edge Gen2 supports 4 high-speed GTYP transceiver from Processing System (PS) and 20 high-speed GTYP transceiver from Programmable Logic (PL), these banks support up to 32Gbps speed.

2.3.1 Power

The Versal AI Edge Gen2 SOM uses discrete power regulators and the DA9062 PMIC from Dialog Semiconductor (Renesas) to manage SOM power. In the SOM, the PS low-power domain, PS full-power domain, and PL power domain supply voltage (VCC_LPD, VCC_FPD, VCC_MMD and VCCINT) are up to 0.88V. AMD Versal AI Edge Gen2 devices are available in -2 (highest performance), -1 speed grades, depending on the speed grade of the device. Additionally, all PS Bank I/O voltages (VCCO_PSIO) are fixed at 1.8V.

The I/O voltage of FPGA IOs are generated from PMIC. PL X5IO Bank 710, 711, 712, 713, 706 and 707 supplies are all combined and generated from PMIC LDO 3&4. PL HD Bank 400 and 402 supply voltages are combined and generated from PMIC LDO2. By default, X5IO Banks voltages are set to 1.2V, and HD Banks voltages are set to 1.8V, but they can be configured through software during boot-up. This SOM also supports VCC_BATT from external regulator with fixed output of 1.5V to the battery-backed RAM and battery-backed real-time clock.

2.3.2 Reset

The Versal AI Edge Gen2 SOM uses Output of the reset IC TPS3808G01DBVR (nRESET) for PS Power On Reset and connected to POR_B_503 pin of SoC. The reset is de asserted after the last of power of SOM is stable.

The SOM also supports hard reset from board-to-board connector2 pin B11.

2.3.3 Versal System Monitor

The System Monitor (SYSMON) resides in the PMC and monitors operating conditions on the device. The SYSMON can access internal sensors for monitoring internal power supplies and temperature. The results captured by the SYSMON are stored in a register map that is accessible through platform management controller resources. These pins are muxed with the pins of SPI interface. MIO pin for this SysMon I2C are PMC_MIO 35, 36 and 37 with SCL, SDA and SMB pins respectively.

2.3.4 Versal Configuration Power & Status LEDs

The Platform management controller (PMC) is responsible for booting the Versal from the primary boot source in a multi-stage boot process that supports both a non-secure and a secure boot. Upon reset, device executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip RAM.

The Versal AI Edge Gen2 SOM supports two LEDs, Power LED indication and error Out indication. LED D2 is for Power Status LEDs. which is connected to last power rail of the SOM in power sequence to make sure all the powers are stable. LED D3 is for Error Out indication. It is asserted for accidental loss of power, a hardware error and not booting etc. Please refer the Image below for this LED identification on SOM.

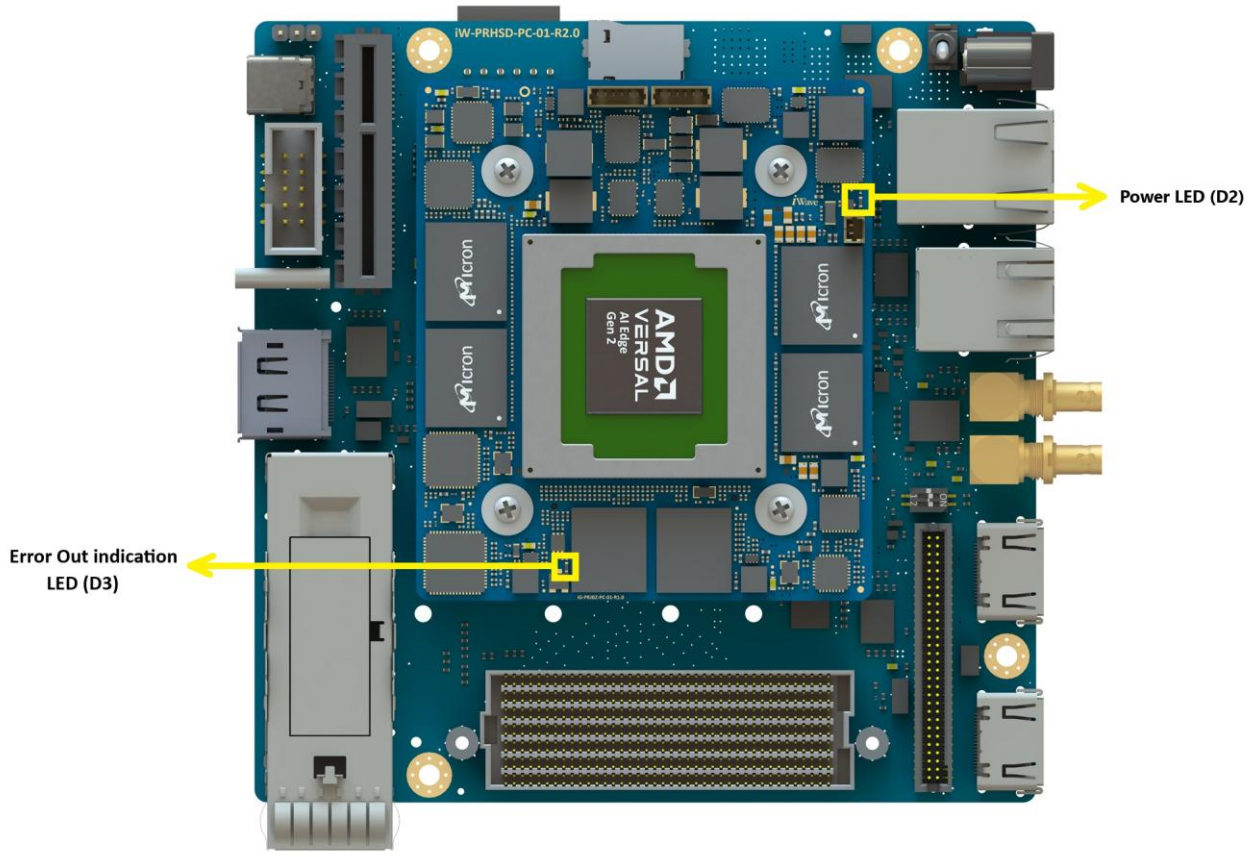


Figure 4: SOM Power and Error Out indication LEDs

The Versal AI Edge Gen2 SOM supports one dedicated input and output configuration pins. PUDC_B pin is an input and is used to select the behaviour of the X5IO or HDIO during configuration and this pin is connected pullup of VCC_1V8 through 4.7K by default. If the pins are high PL IOs are in tri-state and if this pin is low PL IOs internal pullups are enabled.

DONE_503 is output and it's in open drain pin with weak internal pullup. This pin will become high when the boot sequence is complete. By default, this pin is connected to VCC_1V8 through 4.7K.

2.3.5 Reference Clock

The Versal AI Edge Gen2 SOM supports an on-board clock synthesizer for PS reference clock and reference clock to different blocks of Versal AI Edge Gen2 SOC. These reference clock details are mentioned in the below table.

The Versal AI Edge Gen2 SOM supports on board clock synthesizer for PS reference clock and reference clock to different blocks of Versal AI Edge Gen2 SOC. The reference clock from Clock Synthesizer to SoC is mentioned in the below table. The SOM supports two clock synthesizer IC to provide clock to on SOM interfaces and transceiver reference clock1. Versal AI Edge Gen2 SOM clock synthesizer1, "SI5341B-D-GM" is pre-programmed to support on board interfaces during power ON. The address of Clock syntehsizer1 is 74h.

Versal AI Edge Gen2 SOM support one clock synthesizer, “SI5332A-D-GM1” to support FPGA transceiver secondary reference clocks. The output of this clock synthesizer is configured using I2C-1. The 7-bit address of Clock synthesizer2 is 6Ah. Refer the below table for clock output frequency details.

Table 4: SOM Clock Synthesizer 1 reference Clocks

Sl. No	On-SOM Synthesizer	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
1	300MHz	IO_L3P_GC_H0O0P6_M0P70_702	702	AP3	LVDS	LVDS reference clock for PS LPDDR5x. This is connected to X5IO_BANK 702 Global clock pins from OUT2 of Clock Synthesizer 1.
		IO_L3N_GC_H0O0P7_M0P71_702		AP2		
2	24MHz	PAD_USB3_PHY_REF_PAD_CLK_P_504	504	U7	LVDS	LVDS reference clock for PS PMC DIO. This is connected to BANK 504 Reference clock pins from OUT3 of Clock Synthesizer 1.
		PAD_USB3_PHY_REF_PAD_CLK_M_504		U6		
3	300MHz	IO_L19P_GC_H1O0P6_M1P102_703	703	AW10	LVDS	LVDS reference clock for PL LPDDR5x-1. This is connected to X5IO_BANK 703 Global clock pins from OUT4 of Clock Synthesizer 1.
		O_L19N_GC_H1O0P7_M1P103_703		AW9		
4	26MHz	REF_PAD_CLK_P_507	507	AA7	LVDS	LVDS reference clock for PS PMC DIO. This is connected to BANK 507 Reference clock pins from OUT5 of Clock Synthesizer 1.
		REF_PAD_CLK_M_507		AA6		
5	300MHz	IO_L19P_GC_H1O0P6_M3P102_713	713	AP38	LVDS	LVDS reference clock for PL LPDDR5x-2. This is connected to X5IO_BANK 713 Global clock pins from OUT6 of Clock Synthesizer 1.
		IO_L19N_GC_H1O0P7_M3P103_713		AP39		
6	100MHz	IO_L19P_GC_H1O0P6_M2P38_711	711	BA38	LVDS	LVDS reference clock. This is connected to X5IO BANK 711 Global clock pins from OUT7 of Clock Synthesizer 1.
		IO_L19N_GC_H1O0P7_M2P39_711		AY38		
7	300MHz	IO_L19P_GC_H1O0P6_707	707	BA22	LVDS	LVDS reference clock for PL LPDDR5x-3. This is connected to X5IO_BANK 707 Global clock pins from OUT8 of Clock Synthesizer 1.
		IO_L19N_GC_H1O0P7_707		BA23		

Table 5: SOM Clock Synthesizer 2 reference Clocks

Sl. No	On-SOM Synthesizer	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
1	156.25MHz	GTYP_MMI_REFCLKP1_105	105	K5	LVDS	LVDS reference clock This is connected to GTYP_BANK 105 Global clock pins from OUT0 of Clock Synthesizer 2.
		GTYP_MMI_REFCLKN1_105		K4		
2	156.25MHz	GTYP_REFCLKP1_106	106	L7	LVDS	LVDS reference clock This is connected to GTYP_BANK 106 Global clock pins from OUT1 of Clock Synthesizer 2.
		GTYP_REFCLKN1_106		K7		
3	156.25MHz	GTYP_REFCLKP1_107	107	J10	LVDS	LVDS reference clock This is connected to GTYP_BANK 107 Global clock pins from OUT2 of Clock Synthesizer 2
		GTYP_REFCLKN1_107		H10		
4	156.25MHz	GTYP_REFCLKP1_205	205	M38	LVDS	LVDS reference clock This is connected to GTYP_BANK 205 Global clock pins from OUT3 of Clock Synthesizer 2
		GTYP_REFCLKN1_205		M39		
5	156.25MHz	GTYP_REFCLKP1_206	206	K38	LVDS	LVDS reference clock This is connected to GTYP_BANK 206 Global clock pins from OUT4 of Clock Synthesizer 2
		GTYP_REFCLKN1_206		K39		
6	156.25MHz	GTYP_REFCLKP1_207	207	G40	LVDS	LVDS reference clock This is connected to GTYP_BANK 207 Global clock pins from OUT5 of Clock Synthesizer 2
		GTYP_REFCLKN1_207		G41		

2.4 Memory

2.4.1 LPDDR5x SDRAM for PS

The Versal AI Edge Gen2 SOM supports 32bit, 4GB LPDDR5x RAM memory for PS. These LPDDR5x devices operates up to 8533MT/s data rate. Versal AI Edge Gen2 SOM, PL X5IO bank of 700, 701 and 702 are used for LPDDR5x interface. Also, the integrated DDR memory controller (DDRMC) is attached to the NoC interconnect.

The Versal AI Edge Gen2 supports 300MHz clock from Clock synthesizer to PL X5IO bank of 702 for LPDDR5x bank reference clock and it is connected to AP3 & AP2 clock input pins through AC Coupling capacitors.

2.4.2 LPDDR5x SDRAM1 for PL

The Versal AI Edge Gen2 SOM supports 32bit, 4GB LPDDR5x RAM memory for PL. These LPDDR5x devices operates up to 8533MT/s data rate. Versal AI Edge Gen2 SOM, PL X5IO bank of 703, 704 and 705 are used for LPDDR5x interface.

The Versal AI Edge Gen2 SOM supports 300MHz clock from Clock synthesizer to PL X5IO bank of 703 for LPDDR5x bank reference clock and it is connected to AW10 & AW9 clock input pins through AC Coupling capacitors.

2.4.3 LPDDR5x SDRAM2 for PL

The Versal AI Edge Gen2 SOM supports 32bit, 4GB LPDDR5x RAM memory for PL. These LPDDR5x devices operates up to 8533MT/s data rate. Versal AI Edge Gen2 SOM, PL X5IO bank of 713, 714 and 715 are used for LPDDR5x interface.

The Versal AI Edge Gen2 SOM supports 300MHz clock from Clock synthesizer to PL X5IO bank of 713 for LPDDR5x bank reference clock and it is connected to AP38 & AP39 clock input pins through AC Coupling capacitors.

2.4.4 LPDDR5x SDRAM3 for PL

The Versal AI Edge Gen2 SOM supports 32bit, 4GB LPDDR5x RAM memory for PL. These LPDDR5x devices operates up to 8533MT/s data rate. Versal AI Edge Gen2 SOM, PL X5IO bank of 707, 708 and 709 are used for LPDDR5x interface.

The Versal AI Edge Gen2 SOM supports 300MHz clock from Clock synthesizer to PL X5IO bank of 707 for LPDDR5x bank reference clock and it is connected to BA22 & BA23 clock input pins through AC Coupling capacitors.

2.4.5 OSPI Flash

The Versal AI Edge Gen2 SOM supports 256MB of Octal SPI through Octal interface. The OSPI controller use an interface through MIO pins of Versal SOM with 1.8V voltage level. The Flash can be used as boot device or storage device. By default, mode bit is configured for OSPI Flash as configuration device. PMC MIO pins from 0 to 12 are connected to OSPI flash for booting.

2.4.6 eMMC Flash

The Versal AI Edge Gen2 SOM supports 32GB eMMC Flash memory and Storage of Versal Adaptive SoC PS. This eMMC Flash memory is directly connected to the SD0 controller of the SOC's PS through MIO pins and operates at 1.8V Voltage level. This SDIO eMMC controller supports eMMC 5.1 standard with up to 8bit HS400 mode. The eMMC Flash size can be expandable up to 128GB for storage. PMC MIO pins from 40 to 51 are connected to eMMC flash for booting and storage.

2.4.7 EEPROM

The Versal AI Edge Gen2 SOM supports 2Kb EEPROM for storing SOM configuration. The I2C1 module of Versal Adaptive SoC PS is used for EEPROM interface through MIO pins with I2C address 0x52h, 0x5Ah and 0x32h. This device operates at 1.8 voltage level.

2.4.8 UFS Flash

The Versal AI Edge Gen2 SOM supports optional 64GB UFS Flash memory for booting and Storage of Versal Adaptive SoC PS. This UFS Flash memory is directly connected to the UFS controller of the SOC's PS through DIO pins and operates at 1.2V Voltage level. This UFS controller supports UFS 3.1 standard with maximum bandwidth of 23.32 Gb/s.

Note: By default, this UFS Flash is not mounted on SOM. To support this feature please contact iWave.

2.5 Versal SoC Boot Mode Switch

In Versal AI Edge Gen2 SOM, Boot modes are categorized into master and slave mode. The master boot modes automatically load the programmable device image from a memory source and the slave boot modes require an external processor or controller to load the programmable device image with a command set (JTAG or SelectMAP). Versal SOM can support Octal SPI, SD1, eMMC, JTAG & UFS(Optional) as boot device and configurable through boot mode pins. These boot mode pins can be controlled from the D12, D13, B13 & D14 pin of board-to-board connector2. Upon reset, the mode pins are read to determine the primary boot device. By default, PS Mode 0,1,2,3 signals are directly connected to VCC_1V8 through 4.7K Ohm resistor. By default, OSPI is supported as boot device.

Please refer the below table for boot media selection and supported configuration details.

Table 6: Boot Mode Truth Table

Boot Mode Selection				
Boot Media	**MODE3**	**MODE2**	**MODE1**	**MODE0**
PS JTAG	0	0	0	0
SD1	0	0	1	1
OSPI	1	0	0	0
eMMC	0	1	1	0
UFS	1	0	1	1

This Boot Mode switch is physically located at the top of the board as shown below.

Table 7: Boot Mode Switch Truth Table

Versal AI Edge Gen2 Boot Device	**SW4 (4 Position Switch)**				
	PS Mode 0 (Boot SEL0) SW4.1	**PS Mode 1 (Boot SEL1) SW4.2**	**PS Mode 3 (Boot SEL3) SW4.3**	**PS Mode 2 (PWRBTN#) SW4.4**	**Switch Position Image**
PS JTAG	ON	ON	ON	ON	
SD1	OFF	OFF	ON	ON	
eMMC	ON	OFF	ON	OFF	
OSPI (Default)	ON	ON	OFF	ON	

Versal AI Edge Gen2 Boot Device	SW4 (4 Position Switch)				
	PS Mode 0 (Boot SEL0) SW4.1	PS Mode 1 (Boot SEL1) SW4.2	PS Mode 3 (Boot SEL3) SW4.3	PS Mode 2 (PWRBTN#) SW4.4	Switch Position Image
UFS (Optional)	OFF	OFF	OFF	ON	

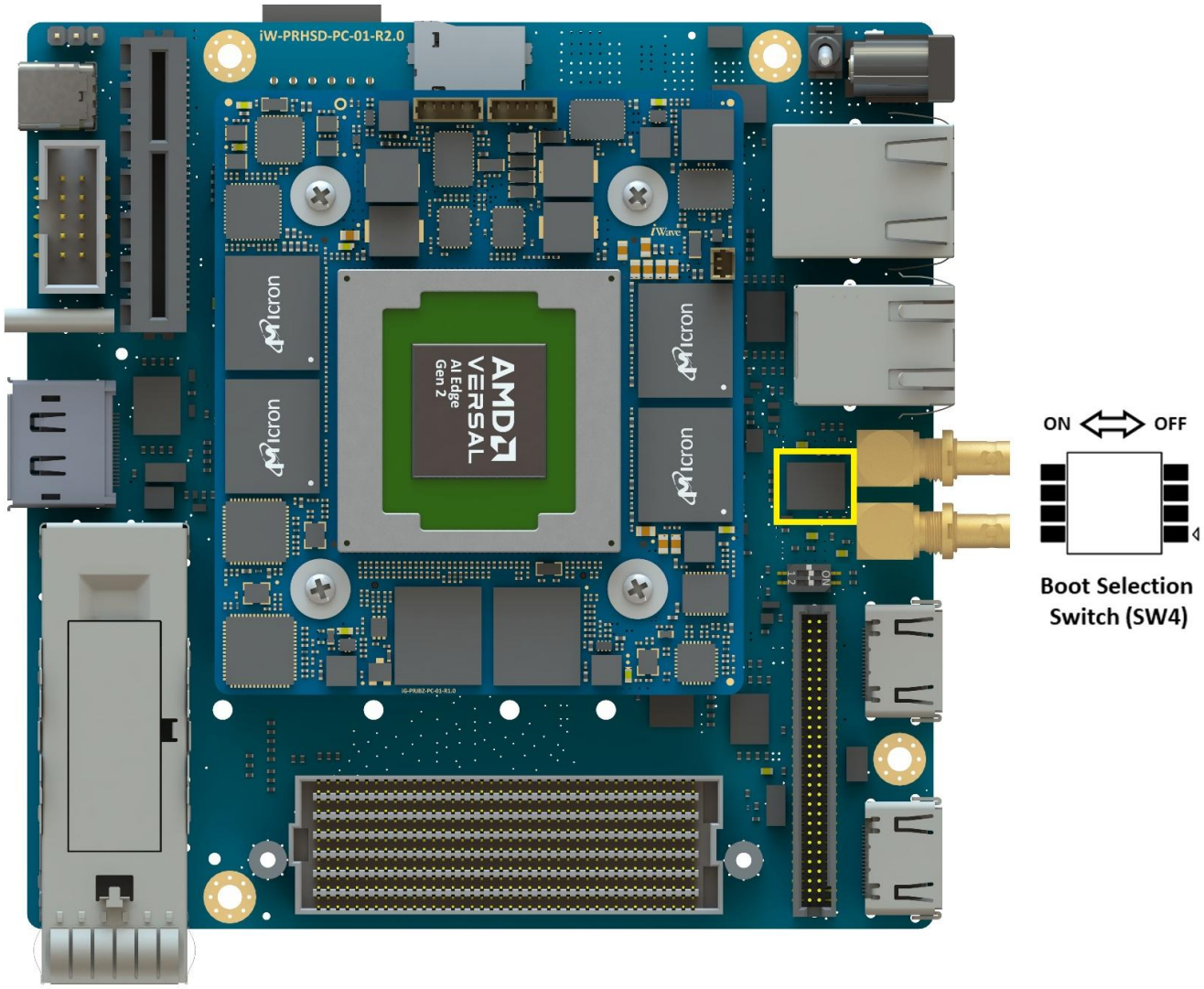


Figure 5: Boot Mode Switch

2.6 Board to Board Connectors

The Versal AI Edge Gen2 SOM development board supports three Board to Board mating connectors for Versal AI Edge Gen2 SOM SOM attachment. This Board-to-Board connector are capable of handling high-speed serialized signals and can be used for size constrained embedded applications.

2.6.1 Board to Board Connector1

Board to Board Connector1 (J10) is physically located at the top of the board as shown below.

Number of Pins - 240

Connector Part Number - ADF6-60-03.5-L-4-2-A-TR from Samtec

Mating connector Part Number - ADM6-60-01.5-L-4-2-A-TR from Samtec

Note: For the Board-to-Board Connector1 pinout, refer the Versal AI Edge Gen2 SOM Hardware Datasheet.

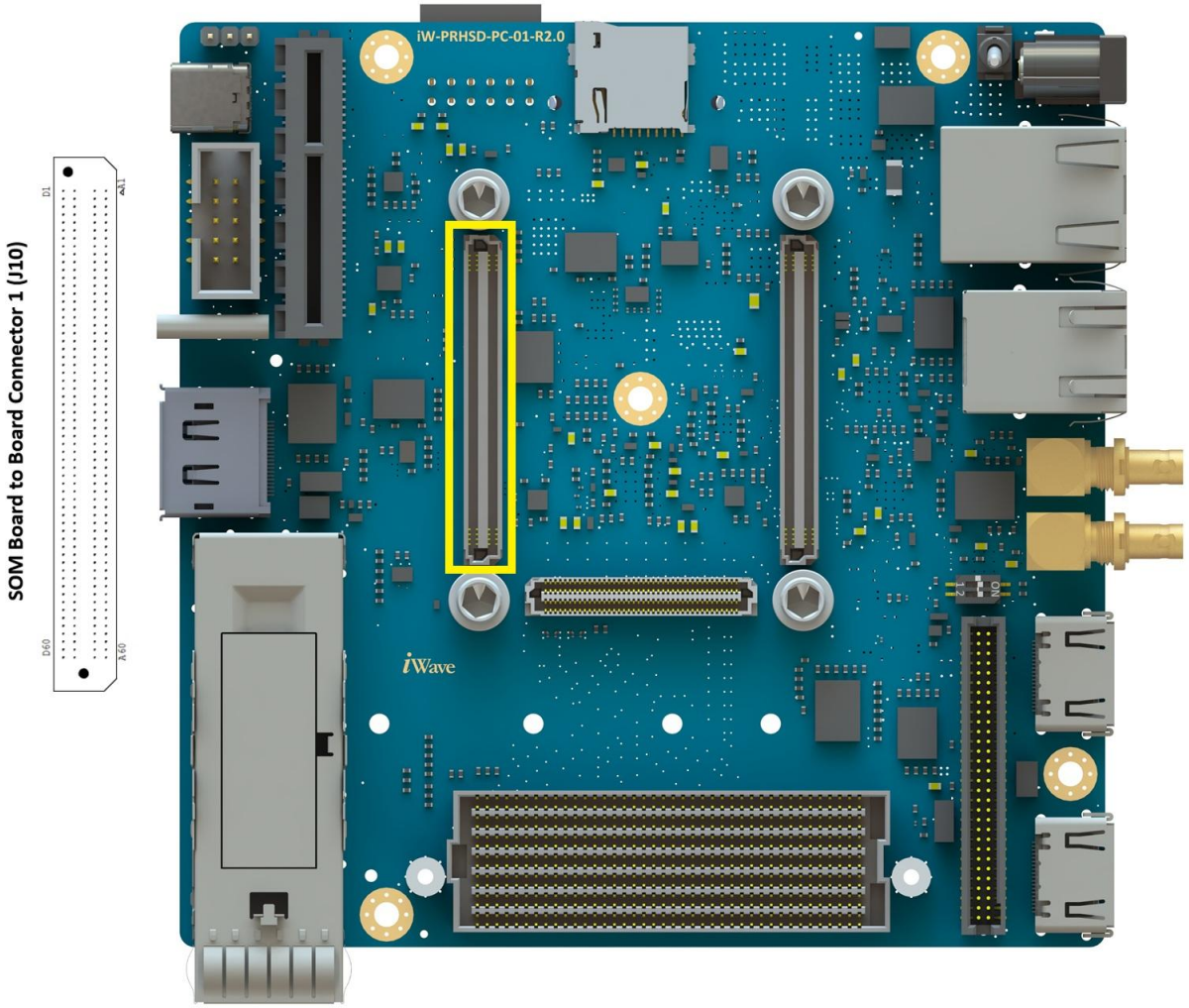


Figure 6: Board to Board Connector1

2.6.2 Board to Board Connector2

Board to Board Connector2 (J11) is physically located at the top of the board as shown below.

Number of Pins - 240

Connector Part Number - ADF6-60-03.5-L-4-2-A-TR from Samtec

Mating connector Part Number - ADM6-60-01.5-L-4-2-A-TR from Samtec

Note: For the Board-to-Board Connector2 pinout, refer the Versal AI Edge Gen2 SOM Hardware Datasheet.

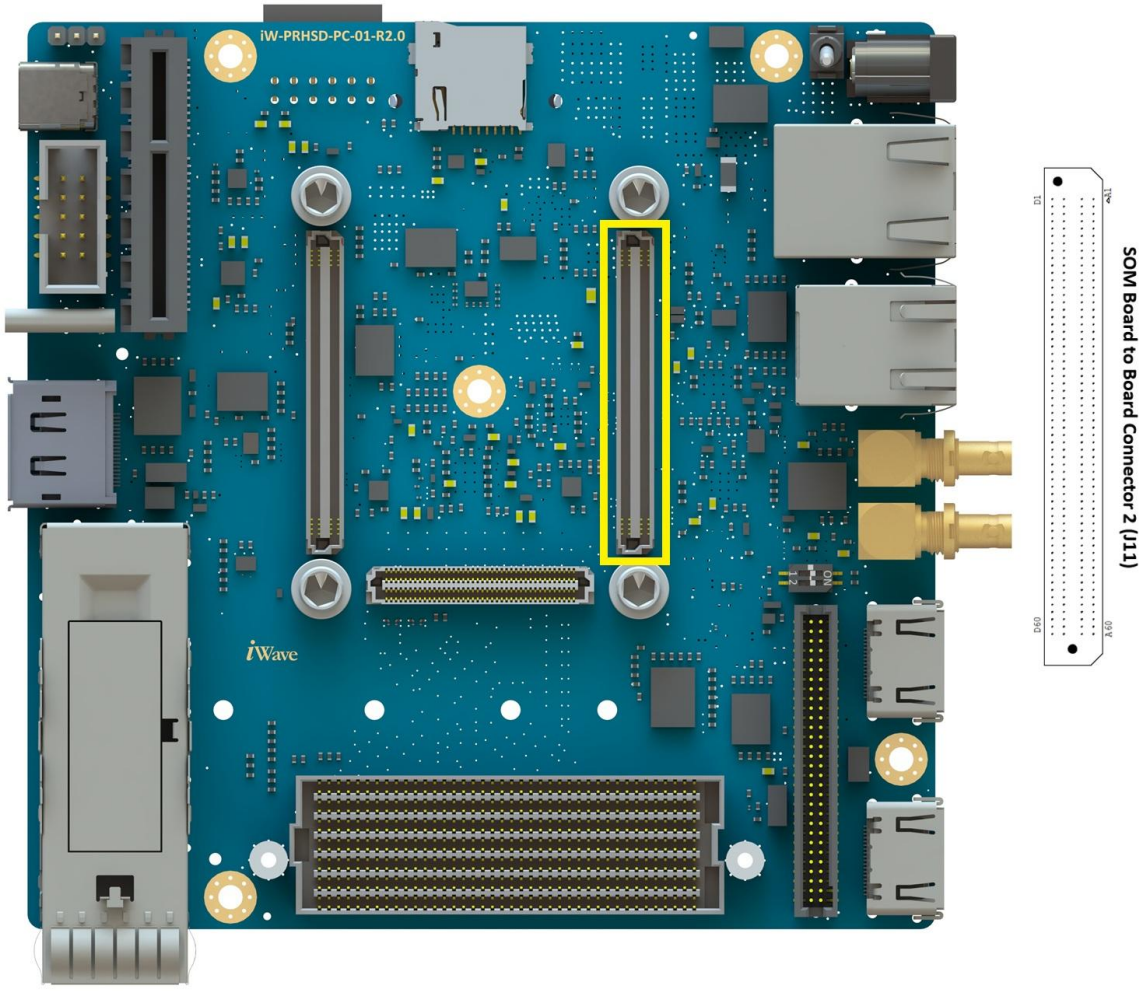


Figure 7: Board to Board Connector 2

2.6.3 Board to Board Connector3

Board to Board Connector3 (J15) is physically located at the top of the board as shown below.

Number of Pins - 160

Connector Part Number - ADF6-40-03.5-L-4-2-A-TR from Samtec

Mating connector Part Number - ADM6-40-01.5-L-4-2-A-TR from Samtec

Note: For the Board-to-Board Connector3 pinout, refer the Versal AI Edge Gen2 SOM Hardware Datasheet.

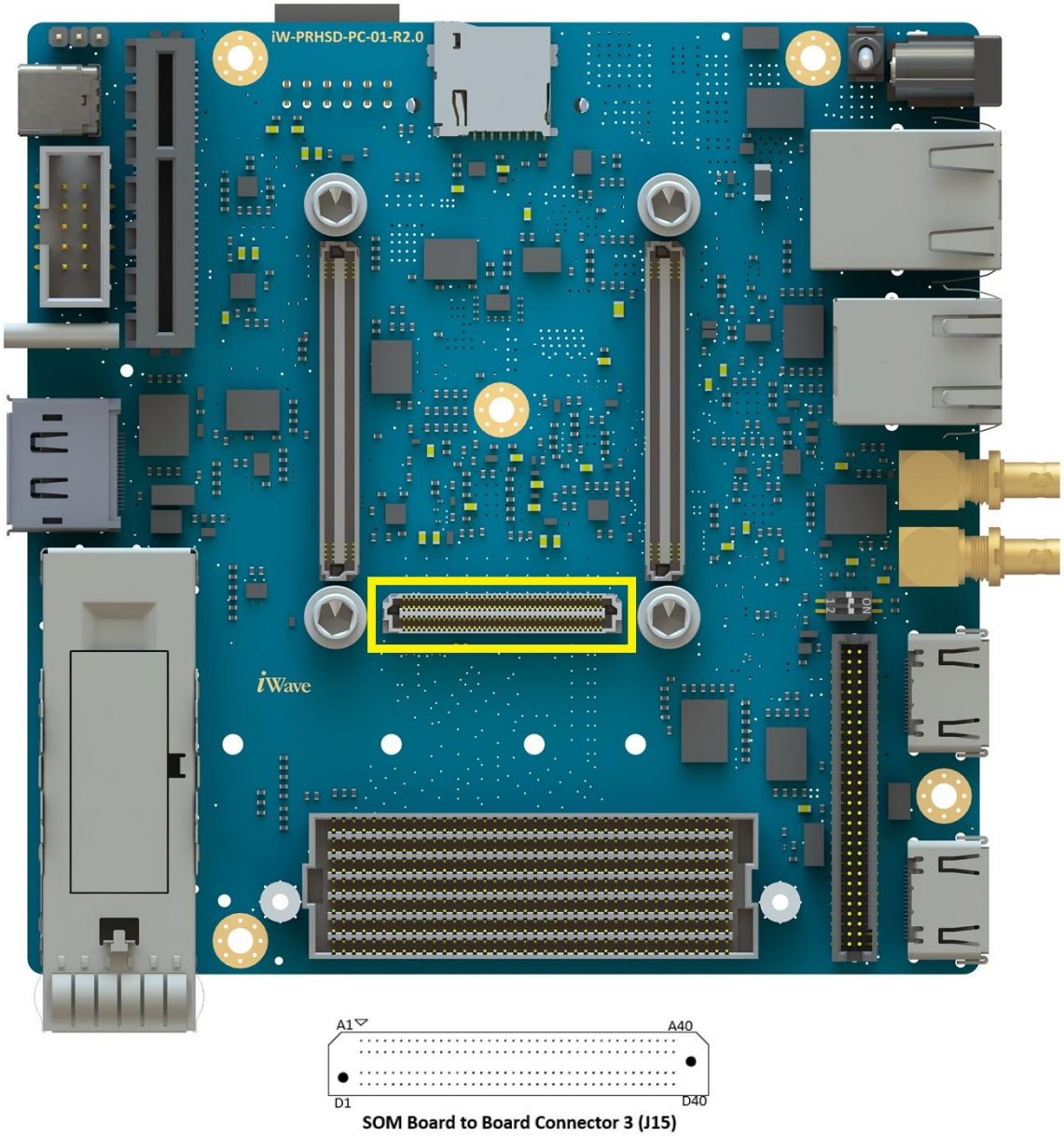


Figure 8: Board to Board Connector 3

2.7 PL Interface Features

The features which are supported from Versal AI Edge Gen2 PL is explained in the following section.

2.7.1 QSFP+ Connector

The Versal AI Edge Gen2 development board supports one QSFP+ Connector through GTYP transceiver Versal AI Edge Gen2 SOM. The GTYP transceiver of FPGA Bank 107, Channels 0 to 3, is connected to QSFP+ Connector via Board-to-Board Connector 2. Also, I2C0 through port 3 of I2C bus switch is connected to QSFP+ connector for control and configuration. All other control signals of QSFP+ connector is connected from IO Expanders.

The QSFP+ Connector (J16) with QSFP+ cage (J18) is physically located at the top of the board as shown below.

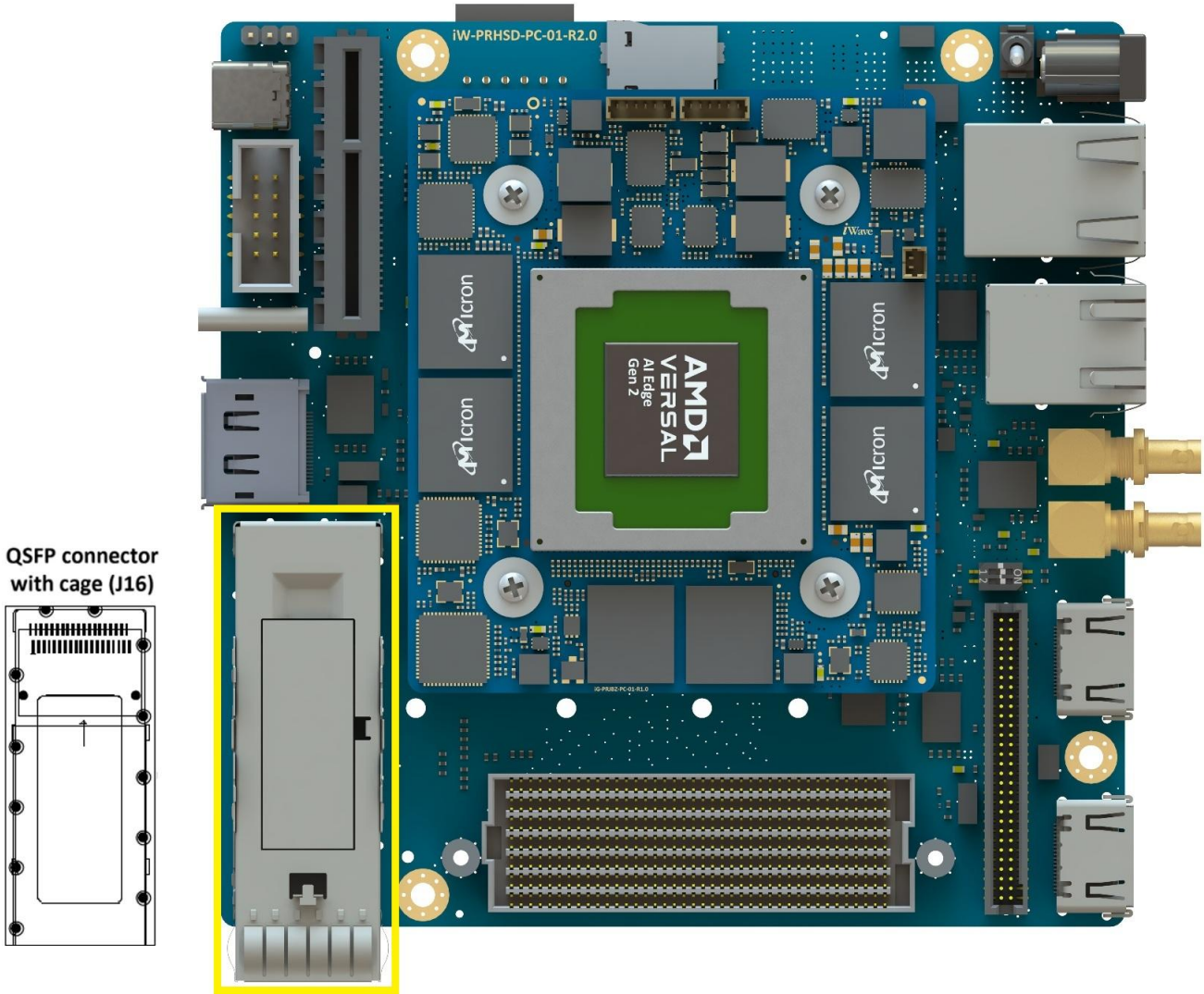


Figure 9:QSFP+ Connector

Table 8: QSFP+ Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground
2	TX2N	GTYP_TXN1_107	O, DIFF	QSFP Transmit2 Data Negative
3	TX2P	GTYP_TXP1_107	O, DIFF	QSFP Transmit2 Data Positive
4	GND	GND	Power	Ground
5	TX4N	GTYP_TXN3_107	O, DIFF	QSFP Transmit4 Data Negative
6	TX4P	GTYP_TXP3_107	O, DIFF	QSFP Transmit4 Data Positive
7	GND	GND	Power	Ground
8	MODSELL	IOEXP2_Q_ModeSEL	O, 3.3V CMOS/ 4.7K PD	Mode Select, connected to IO Expander 2 Port 10. **Low - Responds to serial communication** **High - Will not respond to serial communication**
9	RESETL	IOEXP2_Q_ResetL	O, 3.3V CMOS/ 4.7K PU	Module Reset, connected to IO Expander 2 Port 11. **Low - Module in reset state** **High (3.3V) - Module in out of reset state**
10	VCCRX	VCCRX_3V3	O, 3.3V Power	3.3V Receiver Supply Voltage
11	SCL	I2C0_SW3_SCL	O, 3.3V CMOS/ 4.7K PU	I2C Clock Connected from port SC3 of I2C Bus Switch
12	SDA	I2C0_SW3_SDA	IO. 3.3V CMOS /4.7K PU	I2C Data Connected from port SD3 of I2C Bus Switch
13	GND	GND	Power	Ground
14	RX3P	GTYP_RXP2_107	I, DIFF	QSFP Receiver2 Data Positive
15	RX3N	GTYP_RXN2_107	I, DIFF	QSFP Receiver2 Data Negative
16	GND	GND	Power	Ground
17	RX1P	GTYP_RXP0_107	I, DIFF	QSFP Receiver0 Data Positive
18	RX1N	GTYP_RXN0_107	I, DIFF	QSFP Receiver0 Data Negative
19	GND	GND	Power	Ground
20	GND	GND	Power	Ground
21	RX2N	GTYP_RXN1_107	I, DIFF	QSFP Receiver1 Data Negative
22	RX2P	GTYP_RXP1_107	I, DIFF	QSFP Receiver1 Data Positive
23	GND	GND	Power	Ground
24	RX4N	GTYP_RXN3_107	I, DIFF	QSFP Receiver3 Data Negative
25	RX4P	GTYP_RXP3_107	I, DIFF	QSFP Receiver3 Data Positive
26	GND	GND	Power	Ground

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
27	MODPRSL	IOEXP2_Q_ModPrsl	I, 3.3V CMOS/ 4.7K PU	Module Present, connected to IO Expander 2 Port 14 **Low - When module is inserted** **High - When module is absent**
28	INTL/RXLOS	IOEXP2_Q_INTL	I, 3.3V CMOS/ 4.7K PU	Module Interrupt, Connected to IO Expander 2 Port 13. **Low - Operational fault** **High - Normal operation**
29	VCCTX	VCCTX_3V3	O, 3.3V Power	3.3V Transmit Supply Voltage
30	VCC1	VCC1_3V3	O, 3.3V Power	3.3V Supply Voltage
31	LPMODE/TXDIS	IOEXP2_Q_LPMode	O, 3.3V CMOS/ 4.7K PD	Module Low power mode, connected to IO Expander 2 Port 12 **High for LpMode** **Low for TXDIS mode**
32	GND	GND	Power	Ground
33	TX3P	GTYP_TXP2_107	O, DIFF	QSFP Transmit2 Data Positive
34	TX3N	GTYP_TXN2_107	O, DIFF	QSFP Transmit2 Data Negative
35	GND	GND	Power	Ground
36	TX1P	GTYP_TXP0_107	O, DIFF	QSFP Transmit0 Data Positive
37	TX1N	GTYP_TXN0_107	O, DIFF	QSFP Transmit0 Data Negative
38	GND	GND	Power	Ground

2.7.2 SDI Video IN

The Versal AI Edge Gen2 development board supports one 3G/12G SDI Video IN interface through HD BNC connector (J14). The Video input signals from HD BNC Connector is directly connected to Adaptive Cable Equalizer chip and then connected to Bank106 Channel3 GTYP receiver of Versal AI Edge Gen2 through Board-to-Board connector2.

The Versal AI Edge Gen2 development board supports Video Input Lock status LED (D14) for presence and absence of the Video Input signal on HD BNC connector (J14). This LED will glow when the Video Input signal is detected on HD BNC connector (J14). Also, Channel 1 of I2C Bus switch is connected to Adaptive Cable Equalizer chip for control and configuration with I2C address 0x20. SDI Video IN HD BNC connector (J14) is physically located at the top of the board as shown below.

Note: By default, 12G Adaptive Cable Equalizer chip "LMH1297" is supported on the board. To support 3G Adaptive Cable Equalizer chip "LMH0397", contact iWave.

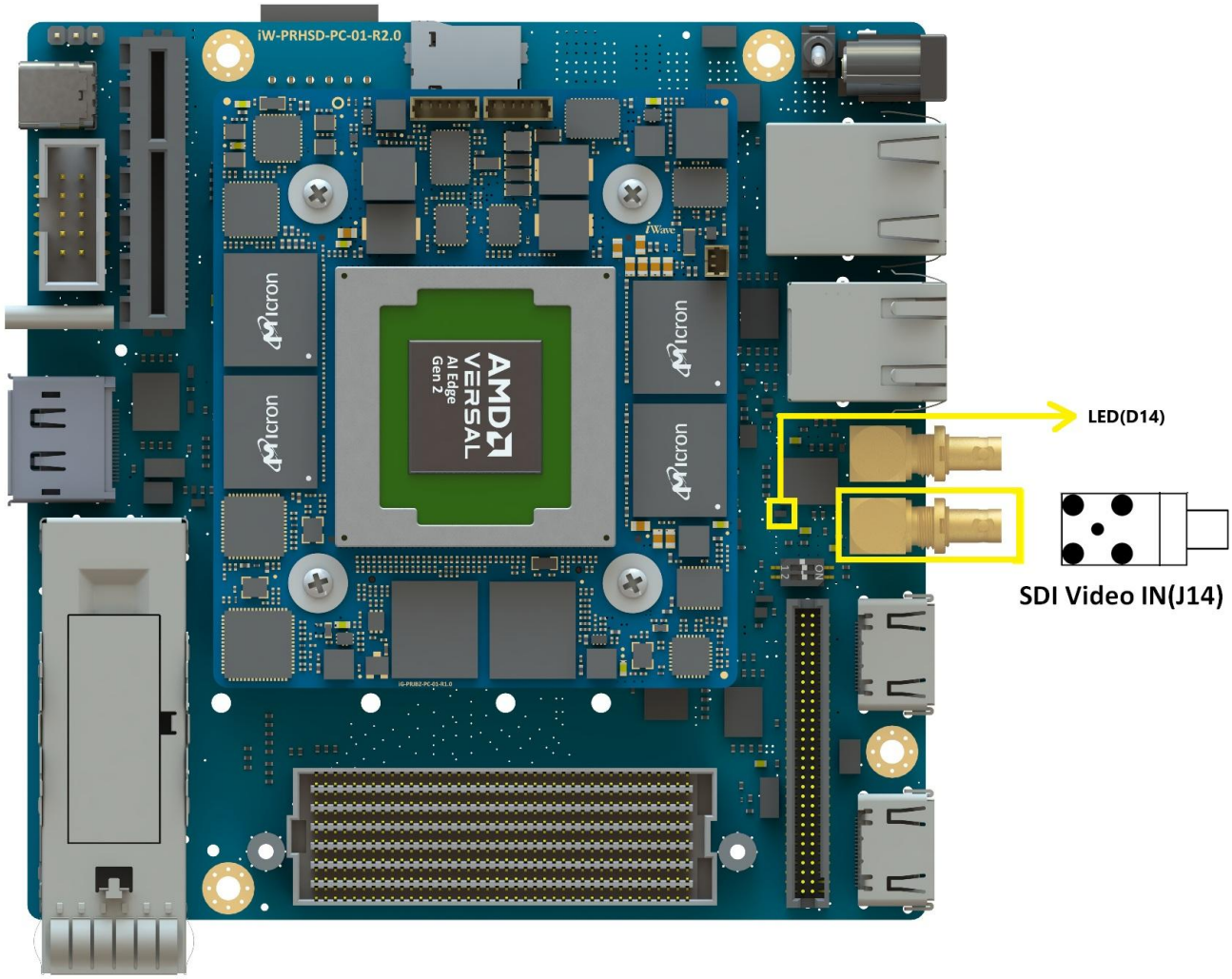


Figure 10:SDI Video IN

2.7.3 SDI Video Out

The Versal AI Edge Gen2 development board supports one 3G/12G SDI Video OUT interface through HD BNC connector (J13). Versal AI Edge Gen2's Bank106 Channel3 GTYP transmitter from Board-to-Board connector2 is directly connected to Cable Driver chip and then connected to HD BNC Connector (J13) for Video out.

The Versal AI Edge Gen2 development board supports Video Output Lock status LED (D9). This LED will glow when the video signal from Versal GTYP transmitter is detected on Cable Driver chip. Also, Channel 1 of I2C Bus switch is connected to Cable Driver chip for control and configuration with I2C address 0x30. SDI Video OUT HD BNC connector (J13) is physically located at the top of the board as shown below.

Note: By default, 12G Adaptive Cable Equalizer chip "LMH1297" is supported on the board. To support 3G Adaptive Cable Equalizer chip "LMH0397", contact iWave.

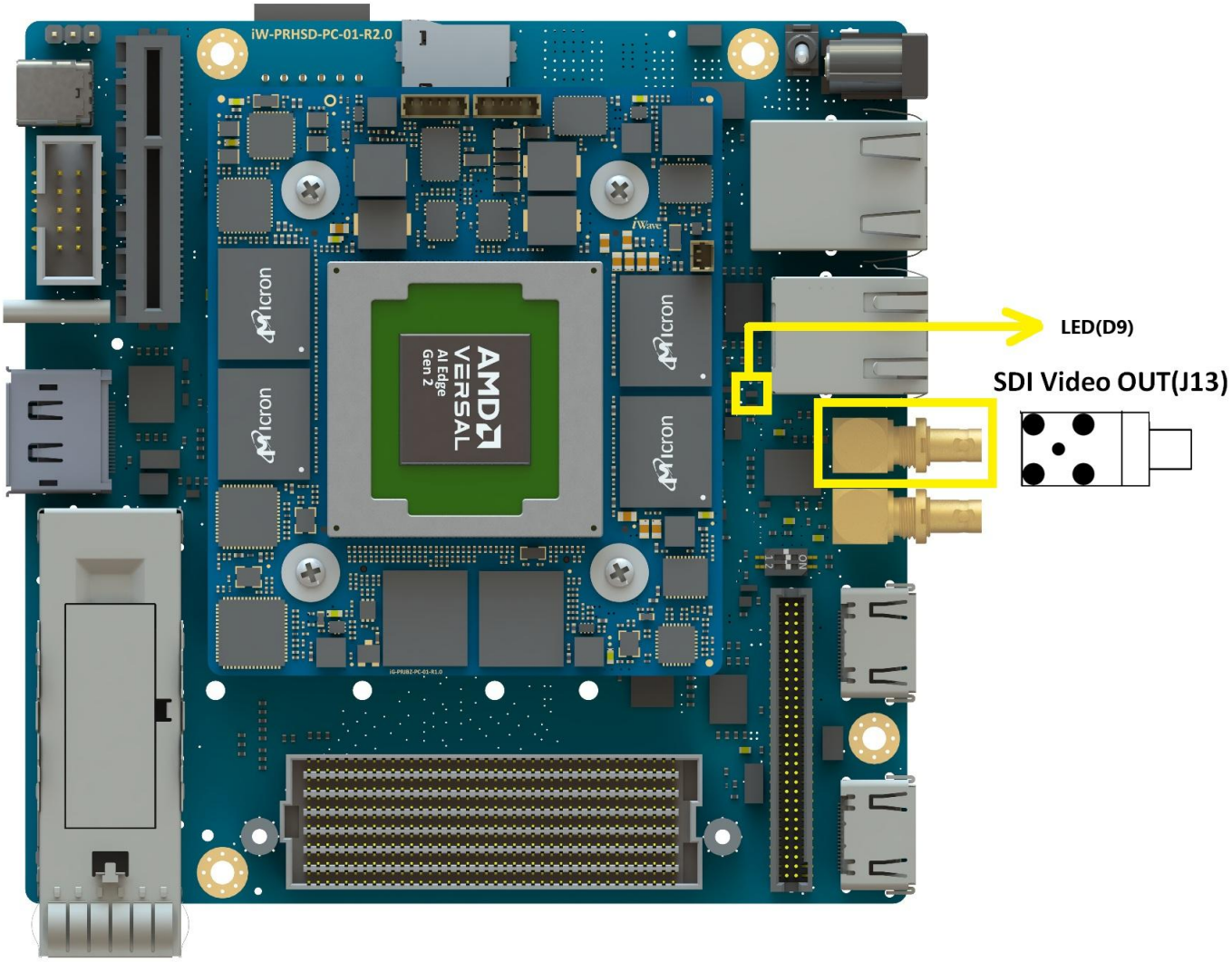


Figure 11:SDI Video OUT

2.7.4 HDMI IN

The Versal AI Edge Gen2 development board supports one HDMI IN interface through HDMI connector (J21). Versal AI Edge Gen2's Bank106 Channel0 to Channel2 GTYP receiver from Board-to-Board connector2 is directly connected from HDMI IN Connector (J21) through AC caps for HDMI IN support. HDMI-IN cable detect feature is supported through PL IO through level translator. HDMI IN connector (J21) is physically located at the top of the board as shown below.

Note: Make sure that SW8.2 switch position set as OFF in bottom view.

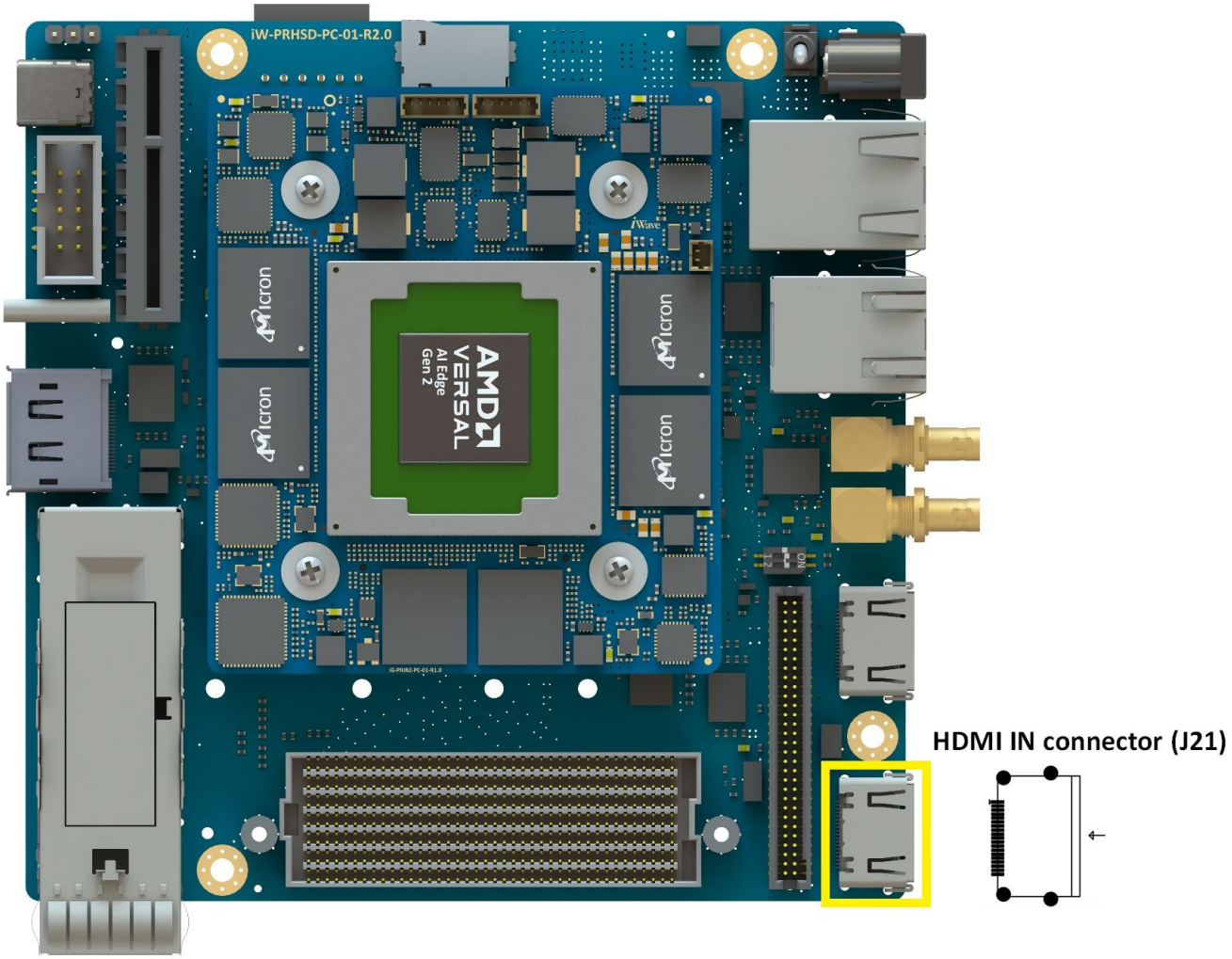


Figure 12:HDMI IN Connector

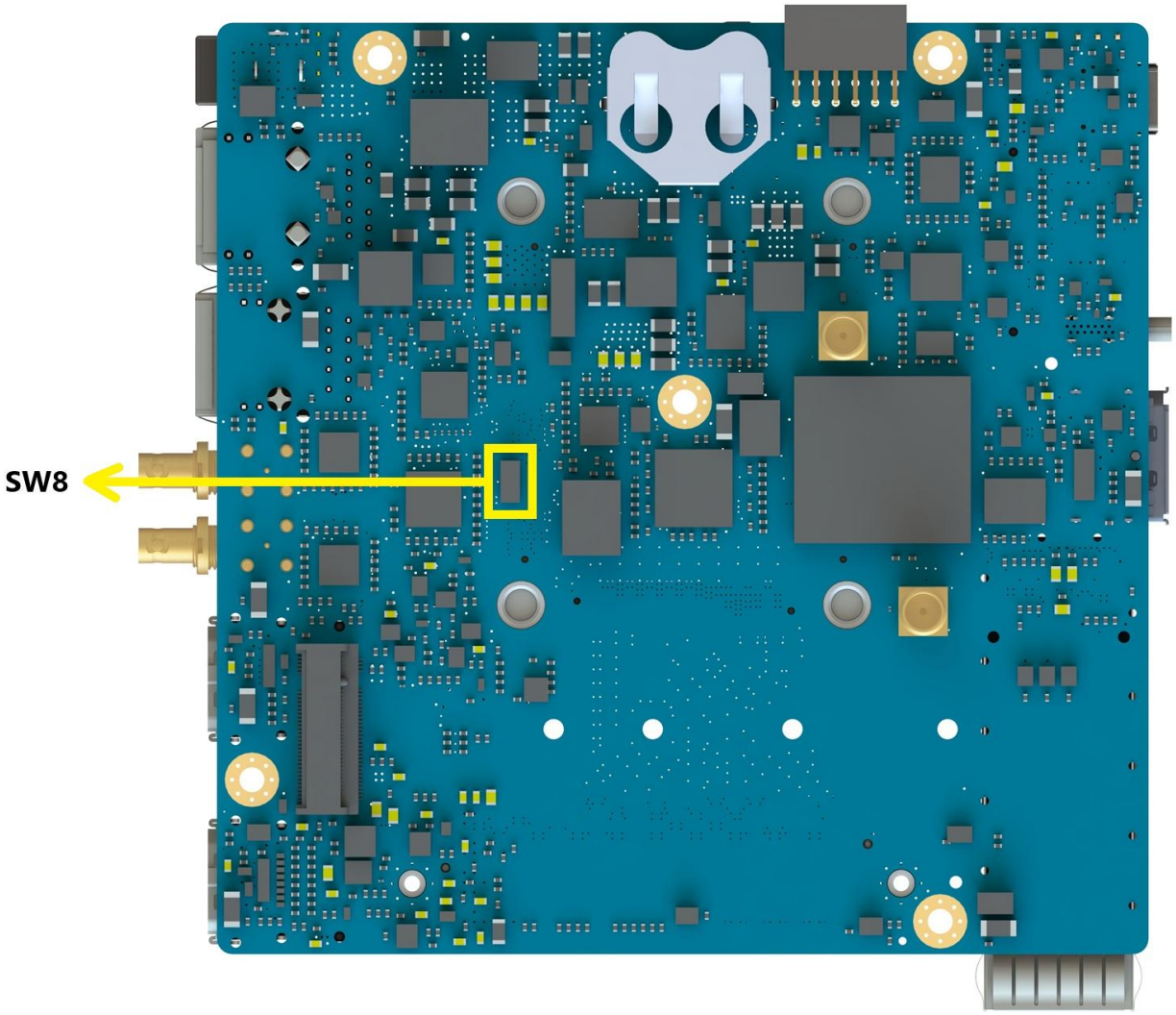


Figure 13: HDMI select switch

2.7.5 HDMI OUT

The Versal AI Edge Gen2 development board supports one HDMI OUT interface through HDMI connector (J17). Versal AI Edge Gen2's Bank106 Channel0 to Channel2 GTYP transceiver from Board-to-Board connector2 is directly connected to HDMI Retimer chip (SN65DP159RGZR) through AC caps and then connected to HDMI OUT Connector (J17) for HDMI Video out. I2C0 from Port 0 of I2C Bus switch is connected to this HDMI Retimer IC for configurations.

Note: Make sure that SW8 switch position set as OFF in bottom view.

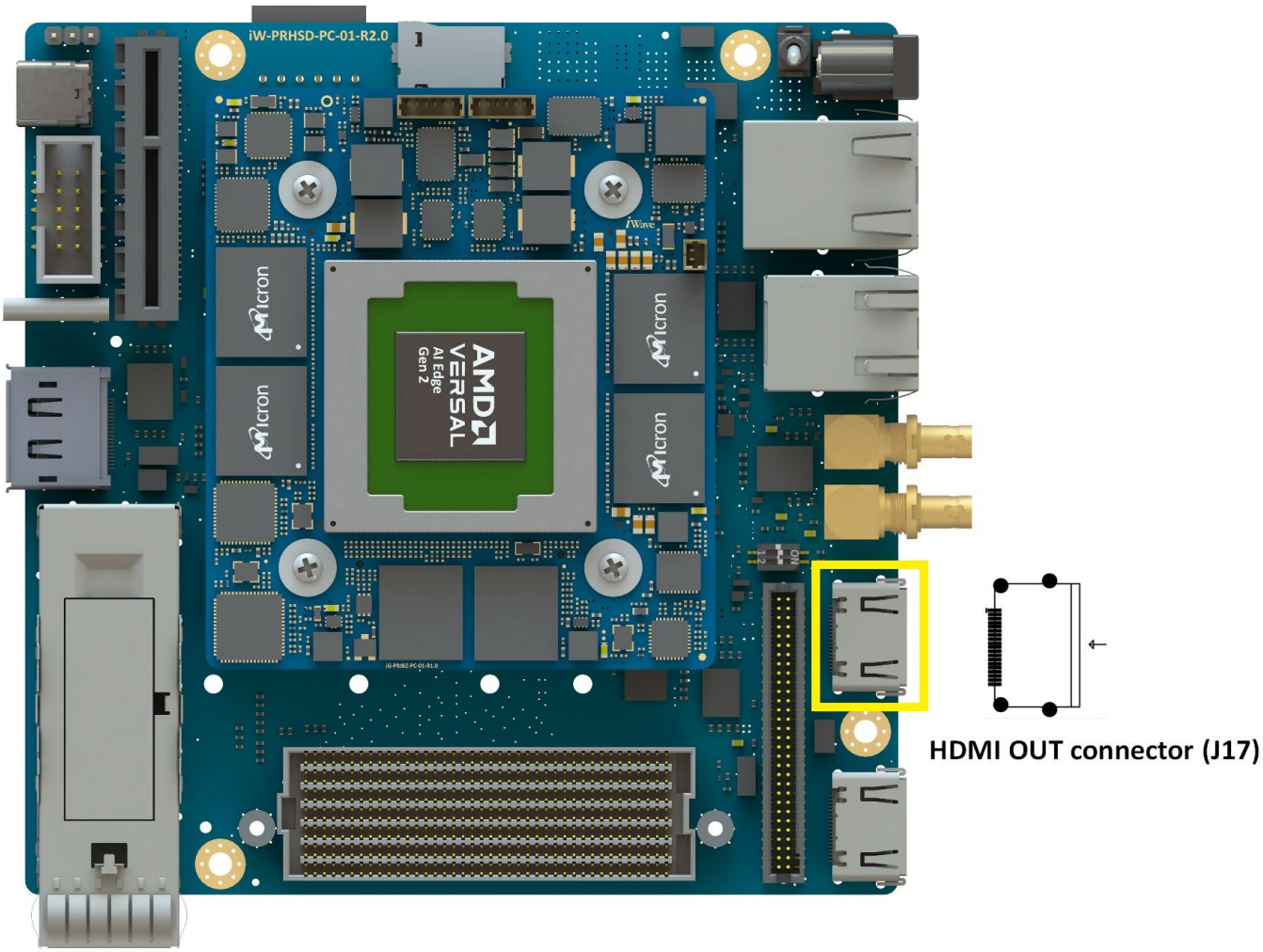


Figure 14:HDMI OUT Connector

2.7.6 FMC+ Connector

The Versal AI Edge Gen2 development board supports one 560Pin FMC+ HSPC connector to support standard ANSI/VITA 57.4 FMC modules.

The FMC+ HSPC Connector 1 (J20) supports the below mentioned interface from Versal AI Edge Gen2 SOM module.

- 12 GTYP High Speed Transceivers Channels
- 3 GTY Reference Clock
- 61LVDS /122 Single ended (SE) IOs from X5IO Bank
- 22LVDS /44 Single ended (SE) IOs from HDIO Bank

This 560Pin FMC+ HSPC connector (J20) is physically located at the top of the board as shown below.

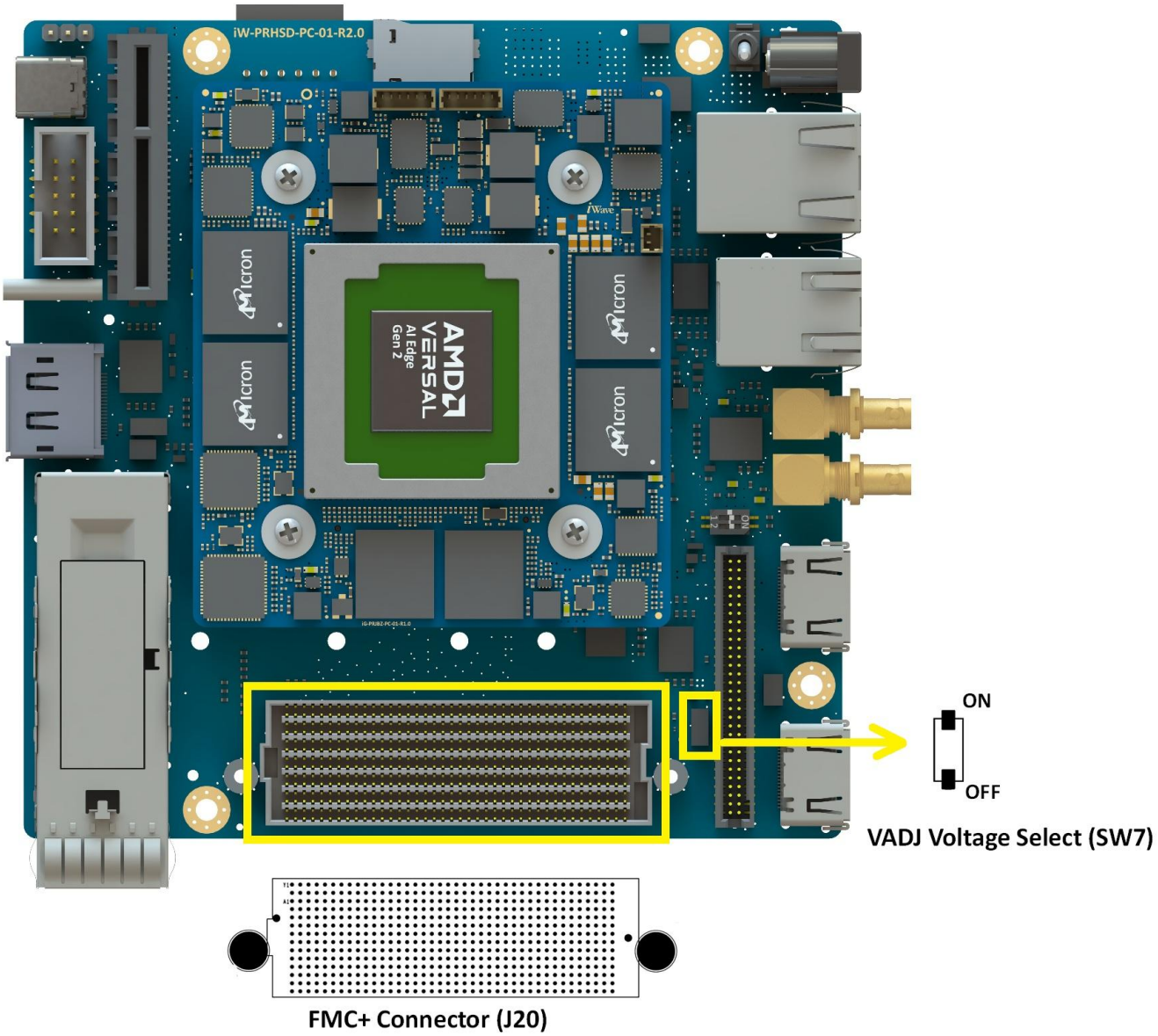


Figure 15: FMC+ Connector

	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	NC	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	NC	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	NC
3	NC	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	NC
4	GND	NC	NC	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	NC	GND
5	GND	NC	NC	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	NC	GND
6	NC	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	NC
7	NC	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	NC
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	NC	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	NC	GND
10	NC	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	NC	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	NC	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	NC	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	NC	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	NC	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	NC	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	NC
19	NC	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	NC
20	GND	NC	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	NC	GND
21	GND	NC	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	NC	GND
22	NC	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	NC
23	NC	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	NC
24	GND	NC	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	NC	HB00_P_CC	HB01_N	NC	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	NC	GND	HB00_N_CC	GND	NC	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	NC	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	NC	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	NC	GND
29	GND	NC	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	NC	GND
30	NC	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	NC
31	NC	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	NC
32	GND	NC	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	NC	GND
33	GND	NC	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	NC	GND
34	NC	GND	HB14_P	HB15_N	LA30_P	LA31_N	NC	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	NC
35	NC	GND	HB14_N	GND	LA30_N	GND	NC	GND	GA1	12P0V	GND	DP4_C2M_N	GND	NC
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	NC	3P3V	GND	DP6_C2M_P	GND	NC	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	NC	GND	12P0V	DP6_C2M_N	GND	NC	GND
38	NC	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	NC
39	NC	GND	GND	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	NC
40	GND	12P0V	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	NC	GND	3P3V	GND

Figure 16:FMC+ Connector Pin Out

Number of Pins - 560

Connector Part Number - ASP-184329-01 from Samtec

Mating Connector - ASP-184330-01 from Samtec

Staking Height - 10mm

Note:

**The FMC+ Adj Voltage is controlled through switch SW7, with a default voltage of 1.2V. When SW7.1 is in the "ON" position and SW7.2 is in the "OFF" position, the voltage is set to 1.8V.*

** By default, FMC+ connector power is disabled as per Vita Specification. While booting the FMC or FMC+ Modules EEPROM is read and enabling the FMC+ connector power.*

** If FMC & FMC+ modules EEPROM is not programmed, then FMC+ connector power is not enabled*

Table 9: FMC+ Connector Pin Assignment

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
1	**A1**	GND1	NA	NA	GND	NA	NA	Power	Ground.
2	**A2**	DP1_M2C_P	B2B Connector 2	B33	GTYP_RXP1_205	205	L45	I, DIFF	GTYP Bank205 channel1 High speed differential receiver positive.
3	**A3**	DP1_M2C_N	B2B Connector 2	B34	GTYP_RXN1_205	205	L46	I, DIFF	GTYP Bank205 channel1 High speed differential receiver negative.
4	**A4**	GND2	NA	NA	GND	NA	NA	Power	Ground.
5	**A5**	GND3	NA	NA	GND	NA	NA	Power	Ground.
6	**A6**	DP2_M2C_P	B2B Connector 2	C35	GTYP_RXP2_205	205	J45	I, DIFF	GTYP Bank205 channel2 High speed differential receiver positive.
7	**A7**	DP2_M2C_N	B2B Connector 2	C36	GTYP_RXN2_205	205	J46	I, DIFF	GTYP Bank205 channel2 High speed differential receiver negative.
8	**A8**	GND4	NA	NA	GND	NA	NA	Power	Ground.
9	**A9**	GND5	NA	NA	GND	NA	NA	Power	Ground.
10	**A10**	DP3_M2C_P	B2B Connector 2	D33	GTYP_RXP3_205	205	G45	I, DIFF	GTYP Bank205 channel3 High speed differential receiver positive.
11	**A11**	DP3_M2C_N	B2B Connector 2	D34	GTYP_RXN3_205	205	G46	I, DIFF	GTYP Bank205 channel3 High speed differential receiver negative.
12	**A12**	GND6	NA	NA	GND	NA	NA	Power	Ground.
13	**A13**	GND7	NA	NA	GND	NA	NA	Power	Ground.
14	**A14**	DP4_M2C_P	B2B Connector 3	A35	GTYP_RXP0_206	206	B44	I, DIFF	GTYP Bank206 channel0 High speed differential receiver positive.
15	**A15**	DP4_M2C_N	B2B Connector 3	A36	GTYP_RXN0_206	206	A44	I, DIFF	GTYP Bank206 channel0 High speed differential receiver negative.
16	**A16**	GND8	NA	NA	GND	NA	NA	Power	Ground.
17	**A17**	GND9	NA	NA	GND	NA	NA	Power	Ground.
18	**A18**	DP5_M2C_P	B2B Connector 3	B33	GTYP_RXP1_206	206	B42	I, DIFF	GTYP Bank206 channel1 High speed differential receiver positive.
19	**A19**	DP5_M2C_N	B2B Connector 3	B34	GTYP_RXN1_206	206	A42	I, DIFF	GTYP Bank206 channel1 High speed differential receiver negative.
20	**A20**	GND10	NA	NA	GND	NA	NA	Power	Ground.
21	**A21**	GND11	NA	NA	GND	NA	NA	Power	Ground.
22	**A22**	DP1_C2M_P	B2B Connector 2	B37	GTYP_TXP1_205	205	M42	O, DIFF	GTYP Bank205 channel1 High speed differential transmitter positive.
23	**A23**	DP1_C2M_N	B2B Connector 2	B38	GTYP_TXN1_205	205	M43	O, DIFF	GTYP Bank205 channel1 High speed differential transmitter negative.
24	**A24**	GND12	NA	NA	GND	NA	NA	Power	Ground.
25	**A25**	GND13	NA	NA	GND	NA	NA	Power	Ground.
26	**A26**	DP2_C2M_P	B2B Connector 2	C39	GTYP_TXP2_205	205	K42	O, DIFF	GTYP Bank205 channel2 High speed differential transmitter positive.
27	**A27**	DP2_C2M_N	B2B Connector 2	C40	GTYP_TXN2_205	205	K43	O, DIFF	GTYP Bank205 channel2 High speed differential transmitter negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
28	**A28**	GND14	NA	NA	GND	NA	NA	Power	Ground.
29	**A29**	GND15	NA	NA	GND	NA	NA	Power	Ground.
30	**A30**	DP3_C2M_P	B2B Connector 2	D37	GTYP_TXP3_205	205	H42	O, DIFF	GTYP Bank205 channel3 High speed differential transmitter positive.
31	**A31**	DP3_C2M_N	B2B Connector 2	D38	GTYP_TXN3_205	205	H43	O, DIFF	GTYP Bank205 channel3 High speed differential transmitter negative.
32	**A32**	GND16	NA	NA	GND	NA	NA	Power	Ground.
33	**A33**	GND17	NA	NA	GND	NA	NA	Power	Ground.
34	**A34**	DP4_C2M_P	B2B Connector 3	B14	GTYP_TXP0_206	206	E45	O, DIFF	GTYP Bank206 channel0 High speed differential transmitter positive.
35	**A35**	DP4_C2M_N	B2B Connector 3	B13	GTYP_TXN0_206	206	D45	O, DIFF	GTYP Bank206 channel0 High speed differential transmitter negative.
36	**A36**	GND18	NA	NA	GND	NA	NA	Power	Ground.
37	**A37**	GND19	NA	NA	GND	NA	NA	Power	Ground.
38	**A38**	DP5_C2M_P	B2B Connector 3	A16	GTYP_TXP1_206	206	E43	O, DIFF	GTYP Bank206 channel1 High speed differential transmitter positive.
39	**A39**	DP5_C2M_N	B2B Connector 3	A15	GTYP_TXN1_206	206	D43	O, DIFF	GTYP Bank206 channel1 High speed differential transmitter negative.
40	**A40**	GND20	NA	NA	GND	NA	NA	Power	Ground.
41	**B1**	CLK_DIR	NA	NA	NA	NA	NA	O, 3.3V	CLK-DIR This Pin is connected to 4th pin of IO Expander (U47).
42	**B2**	GND1	NA	NA	GND	NA	NA	Power	Ground.
43	**B3**	GND2	NA	NA	GND	NA	NA	Power	Ground.
44	**B4**	DP9_M2C_P	B2B Connector 3	A23	GTYP_RXP1_207	207	B34	I, DIFF	GTYP Bank207 channel1 High speed differential receiver positive.
45	**B5**	DP9_M2C_N	B2B Connector 3	A24	GTYP_RXN1_207	207	A34	I, DIFF	GTYP Bank207 channel1 High speed differential receiver negative.
46	**B6**	GND3	NA	NA	GND	NA	NA	Power	Ground.
47	**B7**	GND4	NA	NA	GND	NA	NA	Power	Ground.
48	**B8**	DP8_M2C_P	B2B Connector 3	B21	GTYP_RXP0_207	207	B36	I, DIFF	GTYP Bank207 channel0 High speed differential receiver positive.
49	**B9**	DP8_M2C_N	B2B Connector 3	B22	GTYP_RXN0_207	207	A36	I, DIFF	GTYP Bank207 channel0 High speed differential receiver negative.
50	**B10**	GND5	NA	NA	GND	NA	NA	Power	Ground.
51	**B11**	GND6	NA	NA	GND	NA	NA	Power	Ground.
52	**B12**	DP7_M2C_P	B2B Connector 3	B29	GTYP_RXP3_206	206	B38	I, DIFF	GTYP Bank206 channel3 High speed differential receiver positive.
53	**B13**	DP7_M2C_N	B2B Connector 3	B30	GTYP_RXN3_206	206	A38	I, DIFF	GTYP Bank206 channel3 High speed differential receiver negative.
54	**B14**	GND7	NA	NA	GND	NA	NA	Power	Ground.
55	**B15**	GND8	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
56	**B16**	DP6_M2C_P	B2B Connector 3	A31	GTYP_RXP2_206	206	B40	I, DIFF	GTYP Bank206 channel2 High speed differential receiver positive.
57	**B17**	DP6_M2C_N	B2B Connector 3	A32	GTYP_RXN2_206	206	A40	I, DIFF	GTYP Bank206 channel2 High speed differential receiver negative.
58	**B18**	GND9	NA	NA	GND	NA	NA	Power	Ground.
59	**B19**	GND10	NA	NA	GND	NA	NA	Power	Ground.
60	**B20**	GBTCLK1_M2C_P	B2B Connector 3	D9	GTYP_REFCLKP0_206	206	L40	I, DIFF	GTYP Bank206 channel0 High speed differential reference clock0 positive.
61	**B21**	GBTCLK1_M2C_N	B2B Connector 3	D10	GTYP_REFCLKN0_206	206	L41	I, DIFF	GTYP Bank206 channel0 High speed differential reference clock0 negative.
62	**B22**	GND11	NA	NA	GND	NA	NA	Power	Ground.
63	**B23**	GND12	NA	NA	GND	NA	NA	Power	Ground.
64	**B24**	DP9_C2M_P	B2B Connector 3	A8	GTYP_TXP1_207	207	E35	O, DIFF	GTYP Bank207 channel1 High speed differential transmitter positive.
65	**B25**	DP9_C2M_N	B2B Connector 3	A7	GTYP_TXN1_207	207	D35	O, DIFF	GTYP Bank207 channel1 High speed differential transmitter negative.
66	**B26**	GND13	NA	NA	GND	NA	NA	Power	Ground.
67	**B27**	GND14	NA	NA	GND	NA	NA	Power	Ground.
68	**B28**	DP8_C2M_P	B2B Connector 3	B6	GTYP_TXP0_207	207	E37	O, DIFF	GTYP Bank207 channel0 High speed differential transmitter positive.
69	**B29**	DP8_C2M_N	B2B Connector 3	B5	GTYP_TXN0_207	207	D37	O, DIFF	GTYP Bank207 channel0 High speed differential transmitter negative.
70	**B30**	GND15	NA	NA	GND	NA	NA	Power	Ground.
71	**B31**	GND16	NA	NA	GND	NA	NA	Power	Ground.
72	**B32**	DP7_C2M_P	B2B Connector 3	A12	GTYP_TXP3_206	206	E39	O, DIFF	GTYP Bank206 channel3 High speed differential transmitter positive.
73	**B33**	DP7_C2M_N	B2B Connector 3	A11	GTYP_TXN3_206	206	D39	O, DIFF	GTYP Bank206 channel3 High speed differential transmitter negative.
74	**B34**	GND17	NA	NA	GND	NA	NA	Power	Ground.
75	**B35**	GND18	NA	NA	GND	NA	NA	Power	Ground.
76	**B36**	DP6_C2M_P	B2B Connector 3	B10	GTYP_TXP2_206	206	E41	O, DIFF	GTYP Bank206 channel2 High speed differential transmitter positive.
77	**B37**	DP6_C2M_N	B2B Connector 3	B9	GTYP_TXN2_206	206	D41	O, DIFF	GTYP Bank206 channel2 High speed differential transmitter negative.
78	**B38**	GND19	NA	NA	GND	NA	NA	Power	Ground.
79	**B39**	GND20	NA	NA	GND	NA	NA	Power	Ground.
80	**B40**	RES0	NA	NA	NA	NA	NA	NA	No Connect.
81	**C1**	GND1	NA	NA	GND	NA	NA	Power	Ground.
82	**C2**	DP0_C2M_P	B2B Connector 2	A39	GTYP_TXP0_205	205	P42	O, DIFF	GTYP Bank205 channel0 High speed differential transmitter positive.
83	**C3**	DP0_C2M_N	B2B Connector 2	A40	GTYP_TXN0_205	205	P43	O, DIFF	GTYP Bank205 channel0 High speed differential transmitter negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
84	**C4**	GND2	NA	NA	GND	NA	NA	Power	Ground.
85	**C5**	GND3	NA	NA	GND	NA	NA	Power	Ground.
86	**C6**	DP0_M2C_P	B2B Connector 2	A35	GTYP_RXP0_205	205	N45	I, DIFF	GTYP Bank205 channel0 High speed differential receiver positive.
87	**C7**	DP0_M2C_N	B2B Connector 2	A36	GTYP_RXN0_205	205	N46	I, DIFF	GTYP Bank205 channel0 High speed differential receiver negative.
88	**C8**	GND4	NA	NA	GND	NA	NA	Power	Ground.
89	**C9**	GND5	NA	NA	GND	NA	NA	Power	Ground.
90	**C10**	LA06_P	B2B Connector 1	C4	X5_BF38_LVDS710_L11P	710	BF38	IO, 1.2V	PL Bank710 IO11 differential positive.
91	**C11**	LA06_N	B2B Connector 1	C5	X5_BF39_LVDS710_L11N	710	BF39	IO, 1.2V	PL Bank710 IO11 differential negative.
92	**C12**	GND6	NA	NA	GND	NA	NA	Power	Ground.
93	**C13**	GND7	NA	NA	GND	NA	NA	Power	Ground.
94	**C14**	LA10_P	B2B Connector 1	B6	X5_BD43_LVDS710_L4P	710	BD43	IO, 1.2V	PL Bank710 IO4 differential positive.
95	**C15**	LA10_N	B2B Connector 1	B7	X5_BC44_LVDS710_L4N	710	BC44	IO, 1.2V	PL Bank710 IO4 differential negative.
96	**C16**	GND8	NA	NA	GND	NA	NA	Power	Ground.
97	**C17**	GND9	NA	NA	GND	NA	NA	Power	Ground.
98	**C18**	LA14_P	B2B Connector 1	C11	X5_BA35_LVDS711_L17P_XCC	711	BA35	IO, 1.2V	PL Bank711 IO17 differential positive.
99	**C19**	LA14_N	B2B Connector 1	C12	X5_AY35_LVDS711_L17N_XCC	711	AY35	IO, 1.2V	PL Bank711 IO17 differential negative.
100	**C20**	GND10	NA	NA	GND	NA	NA	Power	Ground.
101	**C21**	GND11	NA	NA	GND	NA	NA	Power	Ground.
102	**C22**	LA18_P_CC	B2B Connector 1	A6	X5_BF43_LVDS710_L5P_XCC	710	BF44	IO, 1.2V	PL Bank710 IO5 differential positive.
103	**C23**	LA18_N_CC	B2B Connector 1	A7	X5_BE43_LVDS710_L5N_XCC	710	BE45	IO, 1.2V	PL Bank710 IO5 differential negative.
104	**C24**	GND12	NA	NA	GND	NA	NA	Power	Ground.
105	**C25**	GND13	NA	NA	GND	NA	NA	Power	Ground.
106	**C26**	LA27_P	B2B Connector 1	D22	X5_BC41_LVDS711_L31P	711	BC41	IO, 1.2V	PL Bank711 IO31 differential positive.
107	**C27**	LA27_N	B2B Connector 1	D23	X5_BC42_LVDS711_L31N	711	BC42	IO, 1.2V	PL Bank711 IO31 differential negative.
108	**C28**	GND14	NA	NA	GND	NA	NA	Power	Ground.
109	**C29**	GND15	NA	NA	GND	NA	NA	Power	Ground.
110	**C30**	SCL	NA	NA	NA	NA	NA	O, 3.3V	FMC+ I2C Clock Signal. This Pin is connected from 10th pin of I2C Bus switch (U24).
111	**C31**	SDA	NA	NA	NA	NA	NA	IO, 3.3V	FMC+ I2C Data Signal. This Pin is connected from 9th pin of I2C Bus switch (U24).
112	**C32**	GND16	NA	NA	GND	NA	NA	Power	Ground.
113	**C33**	GND17	NA	NA	GND	NA	NA	Power	Ground.
114	**C34**	GA0	NA	NA	NA	NA	NA	1K, PD	Geographical address 0
115	**C35**	12P0V	NA	NA	NA	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
116	**C36**	GND18	NA	NA	GND	NA	NA	Power	Ground.
117	**C37**	12P0V	NA	NA	NA	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
118	**C38**	GND19	NA	NA	GND	NA	NA	Power	Ground.
119	**C39**	3P3V	NA	NA	NA	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
120	**C40**	GND20	NA	NA	GND	NA	NA	Power	Ground.
121	**D1**	PG_C2M	NA	NA	NA	NA	NA	O, 3.3V	Power Good Signal from Carrier to FMC Module. This Pin is connected to 8th pin of IO Expander (U47).
122	**D2**	GND1	NA	NA	GND	NA	NA	Power	Ground.
123	**D3**	GND2	NA	NA	GND	NA	NA	Power	Ground.
124	**D4**	GBTCLK0_M2C_P	B2B Connector 2	A31	GTYP_REFCLKP0_205	205	N40	I, DIFF	GTYP Bank205 channel0 High speed differential reference clock0 positive.
125	**D5**	GBTCLK0_M2C_N	B2B Connector 2	A32	GTYP_REFCLKN0_205	205	N41	I, DIFF	GTYP Bank205 channel0 High speed differential reference clock0 negative.
126	**D6**	GND3	NA	NA	GND	NA	NA	Power	Ground.
127	**D7**	GND4	NA	NA	GND	NA	NA	Power	Ground.
128	**D8**	LA01_P_CC	B2B Connector 1	D11	X5_BD46_LVDS710_L2P	710	BD46	IO, 1.2V	PL Bank710 IO2 differential positive.
129	**D9**	LA01_N_CC	B2B Connector 1	D12	X5_BC46_LVDS710_L2N	710	BC46	IO, 1.2V	PL Bank710 IO2 differential negative.
130	**D10**	GND5	NA	NA	GND	NA	NA	Power	Ground.
131	**D11**	LA05_P	B2B Connector 1	C2	X5_BF36_LVDS710_L14P	710	BF36	IO, 1.2V	PL Bank710 IO14 differential positive.
132	**D12**	LA05_N	B2B Connector 1	C3	X5_BF37_LVDS710_L14N	710	BF37	IO, 1.2V	PL Bank710 IO14 differential negative.
133	**D13**	GND6	NA	NA	GND	NA	NA	Power	Ground.
134	**D14**	LA09_P	B2B Connector 1	B4	X5_BF40_LVDS710_L8P	710	BF40	IO, 1.2V	PL Bank710 IO8 differential positive.
135	**D15**	LA09_N	B2B Connector 1	B5	X5_BF41_LVDS710_L8N	710	BF41	IO, 1.2V	PL Bank710 IO8 differential negative.
136	**D16**	GND7	NA	NA	GND	NA	NA	Power	Ground.
137	**D17**	LA13_P	B2B Connector 1	C9	X5_BF44_LVDS710_L0P	710	BF44	IO, 1.2V	PL Bank710 IO0 differential positive.
138	**D18**	LA13_N	B2B Connector 1	C10	X5_BE45_LVDS710_L0N	710	BE45	IO, 1.2V	PL Bank710 IO0 differential negative.
139	**D19**	GND8	NA	NA	GND	NA	NA	Power	Ground.
140	**D20**	LA17_P_CC	B2B Connector 1	A4	X5_BF42_LVDS710_L7P	710	BF42	IO, 1.2V	PL Bank710 IO7 differential positive.
141	**D21**	LA17_N_CC	B2B Connector 1	A5	X5_BE42_LVDS710_L7N	710	BE42	IO, 1.2V	PL Bank710 IO7 differential negative.
142	**D22**	GND9	NA	NA	GND	NA	NA	Power	Ground.
143	**D23**	LA23_P	B2B Connector 1	C15	X5_AY45_LVDS711_L27P	711	AY45	IO, 1.2V	PL Bank711 IO27 differential positive.
144	**D24**	LA23_N	B2B Connector 1	C16	X5_AW46_LVDS711_L27N	711	AW46	IO, 1.2V	PL Bank711 IO27 differential negative.
145	**D25**	GND10	NA	NA	GND	NA	NA	Power	Ground.
146	**D26**	LA26_P	B2B Connector 1	D20	X5_AY44_LVDS711_L28P	711	AY44	IO, 1.2V	PL Bank711 IO28 differential positive.
147	**D27**	LA26_N	B2B Connector 1	D21	X5_AW45_LVDS711_L28N	711	AW45	IO, 1.2V	PL Bank711 IO28 differential negative.
148	**D28**	GND11	NA	NA	GND	NA	NA	Power	Ground.
149	**D29**	TCK	B2B Connector 2	A9	JTAG_TCK	503	R19	I, 3.3V CMOS	JTAG Test Clock. This Pin is connected to A9 pin of Board-to-Board Connector2 (J11) through Voltage level translator.
150	**D30**	TDI	B2B Connector 2	A11	JTAG_TDO	503	T21	O, 3.3V CMOS	FMC+ Test Data Output. This pin is connected from D31st pin of FMC+ Connector

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
151	**D31**	TDO	NA	NA	NA	NA	NA	O, 3.3V CMOS	NC.
152	**D32**	3P3VAUX	NA	NA	NA	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
153	**D33**	TMS	B2B Connector 2	A10	JTAG_TMS	503	N21	I, 3.3V CMOS/ 49.9K PU	JTAG Test Mode Select. This Pin is connected to A10th pin of Board-to-Board Connector2 (J11) through Voltage level translator.
154	**D34**	TRST_L	NA	NA	NA	NA	NA	NA	No Connect
155	**D35**	GA1	NA	NA	NA	NA	NA	1K, PD	Geographical address 1
156	**D36**	3P3V	NA	NA	NA	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
157	**D37**	GND12	NA	NA	GND	NA	NA	Power	Ground.
158	**D38**	3P3V	NA	NA	NA	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
159	**D39**	GND13	NA	NA	GND	NA	NA	Power	Ground.
160	**D40**	3P3V	NA	NA	NA	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
161	**E1**	GND1	NA	NA	GND	NA	NA	Power	Ground.
162	**E2**	HA01_P_CC	B2B Connector 1	D25	X5_AV46_LVDS712_L3P_GC	712	AV46	IO, 1.2V	PL Bank712 IO3 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
163	**E3**	HA01_N_CC	B2B Connector 1	D26	X5_AU46_LVDS712_L3N_GC	712	AU46	IO, 1.2V	PL Bank712 IO3 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
164	**E4**	GND2	NA	NA	GND	NA	NA	Power	Ground.
165	**E5**	GND3	NA	NA	GND	NA	NA	Power	Ground.
166	**E6**	HA05_P	B2B Connector 1	C27	X5_AU38_LVDS712_L11P	712	AU38	IO, 1.2V	PL Bank712 IO11 differential positive.
167	**E7**	HA05_N	B2B Connector 1	C28	X5_AU39_LVDS712_L11N	712	AU39	IO, 1.2V	PL Bank712 IO11 differential negative.
168	**E8**	GND4	NA	NA	GND	NA	NA	Power	Ground.
169	**E9**	HA09_P	B2B Connector 1	B29	X5_AT37_LVDS712_L13P_XCC	712	AT37	IO, 1.2V	PL Bank712 IO13 differential positive.
170	**E10**	HA09_N	B2B Connector 1	B30	X5_AR37_LVDS712_L13N_XCC	712	AR37	IO, 1.2V	PL Bank712 IO13 differential negative.
171	**E11**	GND5	NA	NA	GND	NA	NA	Power	Ground.
172	**E12**	HA13_P	B2B Connector 1	D31	X5_AL39_LVDS713_L21P_XCC	713	AL39	IO, 1.2V	PL Bank713 IO21 differential positive.
173	**E13**	HA13_N	B2B Connector 1	D32	X5_AM40_LVDS713_L21N_XCC	713	AM40	IO, 1.2V	PL Bank713 IO21 differential negative.
174	**E14**	GND6	NA	NA	GND	NA	NA	Power	Ground.
175	**E15**	HA16_P	B2B Connector 3	D14	HDIO_R45_BANK402_L0P	402	R45	IO, 1.8V	PL Bank402 IO0 differential positive.
176	**E16**	HA16_N	B2B Connector 3	D15	HDIO_R46_BANK402_L0N	402	R46	IO, 1.8V	PL Bank402 IO0 differential negative.
177	**E17**	GND7	NA	NA	GND	NA	NA	Power	Ground.
178	**E18**	HA20_P	B2B Connector 3	C14	HDIO_Y45_BANK400_L1P	400	Y45	IO, 1.8V	PL Bank400 IO1 differential positive.
179	**E19**	HA20_N	B2B Connector 3	C15	HDIO_Y46_BANK400_L1N	400	Y46	IO, 1.8V	PL Bank400 IO1 differential negative.
180	**E20**	GND8	NA	NA	GND	NA	NA	Power	Ground.
181	**E21**	HB03_P	B2B Connector 3	C21	HDIO_Y40_BANK400_L7P	400	Y40	IO, 1.8V	PL Bank400 IO7 differential positive.
182	**E22**	HB03_N	B2B Connector 3	C22	HDIO_W41_BANK400_L7N	400	W41	IO, 1.8V	PL Bank400 IO7 differential negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
183	**E23**	GND9	NA	NA	GND	NA	NA	Power	Ground.
184	**E24**	HB05_P	B2B Connector 3	C28	HDIO_T44_BANK402_L2P	402	T44	IO, 1.8V	PL Bank402 IO2 differential positive.
185	**E25**	HB05_N	B2B Connector 3	C29	HDIO_T45_BANK402_L2N	402	T45	IO, 1.8V	PL Bank402 IO2 differential negative.
186	**E26**	GND10	NA	NA	GND	NA	NA	Power	Ground.
187	**E27**	HB09_P	B2B Connector 3	D35	HDIO_U40_BANK402_L7P	402	U40	IO, 1.8V	PL Bank402 IO7 differential positive.
188	**E28**	HB09_N	B2B Connector 3	D36	HDIO_U41_BANK402_L7N	402	U41	IO, 1.8V	PL Bank402 IO7 differential negative.
189	**E29**	GND11	NA	NA	GND	NA	NA	Power	Ground.
190	**E30**	HB13_P	B2B Connector 3	C37	X5_AT22_LVDS707_L16P	707	AT22	IO, 1.2V	PL Bank707 IO16 differential positive.
191	**E31**	HB13_N	B2B Connector 3	C38	X5_AU21_LVDS707_L16N	707	AU21	IO, 1.2V	PL Bank707 IO16 differential negative.
192	**E32**	GND12	NA	NA	GND	NA	NA	Power	Ground.
193	**E33**	HB19_P	B2B Connector 3	B39	X5_BD20_LVDS707_L26N	707	BD20	IO, 1.2V	PL Bank707 IO26 differential negative.
194	**E34**	HB19_N	B2B Connector 3	B40	X5_BD19_LVDS707_L26P	707	BD19	IO, 1.2V	PL Bank707 IO26 differential positive.
195	**E35**	GND13	NA	NA	GND	NA	NA	Power	Ground.
196	**E36**	HB21_P	NA	NA	NA	NA	NA	NA	No Connect
197	**E37**	HB21_N	NA	NA	NA	NA	NA	NA	No Connect
198	**E38**	GND14	NA	NA	GND	NA	NA	Power	Ground.
199	**E39**	VADJ	NA	NA	NA	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
200	**E40**	GND15	NA	NA	GND	NA	NA	Power	Ground.
201	**F1**	PG_M2C	NA	NA	NA	NA	NA	I, 3.3V	Power Good Signal from FMC Module to Carrier. This Pin is connected to 5th pin of IO Expander (U47).
202	**F2**	GND1	NA	NA	GND	NA	NA	Power	Ground.
203	**F3**	GND2	NA	NA	GND	NA	NA	Power	Ground.
204	**F4**	HA00_P_CC	B2B Connector 1	A22	X5_AV40_LVDS712_L7P	712	AV40	IO, 1.2V	PL Bank712 IO7 differential positive.
205	**F5**	HA00_N_CC	B2B Connector 1	A23	X5_AV41_LVDS712_L7N	712	AV41	IO, 1.2V	PL Bank712 IO7 differential negative.
206	**F6**	GND3	NA	NA	GND	NA	NA	Power	Ground.
207	**F7**	HA04_P	B2B Connector 1	C25	X5_AU41_LVDS712_L8P	712	AU41	IO, 1.2V	PL Bank712 IO8 differential positive.
208	**F8**	HA04_N	B2B Connector 1	C26	X5_AU42_LVDS712_L8N	712	AU42	IO, 1.2V	PL Bank712 IO8 differential negative.
209	**F9**	GND4	NA	NA	GND	NA	NA	Power	Ground.
210	**F10**	HA08_P	B2B Connector 1	B27	X5_AU36_LVDS712_L14P	712	AU36	IO, 1.2V	PL Bank712 IO14 differential positive.
211	**F11**	HA08_N	B2B Connector 1	B28	X5_AT36_LVDS712_L14N	712	AT36	IO, 1.2V	PL Bank712 IO14 differential negative.
212	**F12**	GND5	NA	NA	GND	NA	NA	Power	Ground.
213	**F13**	HA12_P	B2B Connector 1	A29	X5_AM38_LVDS713_L20P	712	AM38	IO, 1.2V	PL Bank712 IO20 differential positive.
214	**F14**	HA12_N	B2B Connector 1	A30	X5_AL38_LVDS713_L20N	712	AL38	IO, 1.2V	PL Bank712 IO20 differential negative.
215	**F15**	GND6	NA	NA	GND	NA	NA	Power	Ground.
216	**F16**	HA15_P	B2B Connector 1	B31	X5_AP41_LVDS713_L23P	713	AP41	IO, 1.2V	PL Bank712 IO23 differential positive.
217	**F17**	HA15_N	B2B Connector 1	B32	X5_AP42_LVDS713_L23N	713	AP42	IO, 1.2V	PL Bank712 IO23 differential negative.
218	**F18**	GND7	NA	NA	GND	NA	NA	Power	Ground.
219	**F19**	HA19_P	B2B Connector 3	D18	HDIO_W44_BANK400_L3P	400	W44	IO, 1.8V	PL Bank400 IO3 differential positive.
220	**F20**	HA19_N	B2B Connector 3	D19	HDIO_W45_BANK400_L3N	400	W45	IO, 1.8V	PL Bank400 IO3 differential negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
221	**F21**	GND8	NA	NA	GND	NA	NA	Power	Ground.
222	**F22**	HB02_P	B2B Connector 3	D25	HDIO_AA39_BANK400_L8P	400	AA39	IO, 1.8V	PL Bank400 IO8 differential positive.
223	**F23**	HB02_N	B2B Connector 3	D26	HDIO_AA40_BANK400_L8N	400	AA40	IO, 1.8V	PL Bank400 IO8 differential negative.
224	**F24**	GND9	NA	NA	GND	NA	NA	Power	Ground.
225	**F25**	HB04_P	B2B Connector 3	D32	HDIO_V42_BANK402_L4P	402	V42	IO, 1.8V	PL Bank402 IO4 differential positive.
226	**F26**	HB04_N	B2B Connector 3	D33	HDIO_V43_BANK402_L4N	402	V43	IO, 1.8V	PL Bank402 IO4 differential negative.
227	**F27**	GND10	NA	NA	GND	NA	NA	Power	Ground.
228	**F28**	HB08_P	B2B Connector 3	C32	HDIO_V44_BANK402_L3P	402	V44	IO, 1.8V	PL Bank402 IO3 differential positive.
229	**F29**	HB08_N	B2B Connector 3	C33	HDIO_U44_BANK402_L3N	402	U44	IO, 1.8V	PL Bank402 IO3 differential negative.
230	**F30**	GND11	NA	NA	GND	NA	NA	Power	Ground.
231	**F31**	HB12_P	B2B Connector 3	C35	HDIO_T38_BANK402_L10P	402	T38	IO, 1.8V	PL Bank402 IO10 differential positive.
232	**F32**	HB12_N	B2B Connector 3	C36	HDIO_T39_BANK402_L10N	402	T39	IO, 1.8V	PL Bank402 IO10 differential negative.
233	**F33**	GND12	NA	NA	GND	NA	NA	Power	Ground.
234	**F34**	HB16_P	NA	NA	NA	NA	NA	NA	No Connect
235	**F35**	HB16_N	NA	NA	NA	NA	NA	NA	No Connect
236	**F36**	GND13	NA	NA	GND	NA	NA	Power	Ground.
237	**F37**	HB20_P	B2B Connector 3	B37	X5_BB22_LVDS707_L21N	707	BB22	IO, 1.2V	PL Bank707 IO21 differential negative.
238	**F38**	HB20_N	B2B Connector 3	B38	X5_BB21_LVDS707_L21P	707	BB21	IO, 1.2V	PL Bank707 IO21 differential positive.
239	**F39**	GND14	NA	NA	GND	NA	NA	Power	Ground.
240	**F40**	VADJ	NA	NA	NA	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
241	**G1**	GND1	NA	NA	GND	NA	NA	Power	Ground.
242	**G2**	CLK1_M2C_P	B2B Connector 3	D30	HDIO_T42_BANK402_HDGC_L5P	402	T42	IO, 1.8V	PL Bank402 IO5 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
243	**G3**	CLK1_M2C_N	B2B Connector 3	D31	HDIO_T43_BANK402_HDGC_L5N	402	T43	IO, 1.8V	PL Bank402 IO5 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
244	**G4**	GND2	NA	NA	GND	NA	NA	Power	Ground.
245	**G5**	GND3	NA	NA	GND	NA	NA	Power	Ground.
246	**G6**	LA00_P_CC	B2B Connector 1	D9	X5_BB45_LVDS710_L3P_GC	710	BB45	IO, 1.2V	PL Bank710 IO3 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
247	**G7**	LA00_N_CC	B2B Connector 1	D10	X5_BB46_LVDS710_L3N_GC	710	BB46	IO, 1.2V	PL Bank710 IO3 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
248	**G8**	GND4	NA	NA	GND	NA	NA	Power	Ground.
249	**G9**	LA03_P	B2B Connector 1	D4	X5_BB37_LVDS710_L12P	710	BB37	IO, 1.2V	PL Bank710 IO12 differential positive.
250	**G10**	LA03_N	B2B Connector 1	D5	X5_BC38_LVDS710_L12N	710	BC38	IO, 1.2V	PL Bank710 IO12 differential negative.
251	**G11**	GND5	NA	NA	GND	NA	NA	Power	Ground.
252	**G12**	LA08_P	B2B Connector 1	B2	X5_BE39_LVDS710_L9P_XCC	710	BE39	IO, 1.2V	PL Bank710 IO9 differential positive.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
253	**G13**	LA08_N	B2B Connector 1	B3	X5_BE40_LVDS710_L9N_XCC	710	BE40	IO, 1.2V	PL Bank710 IO9 differential negative.
254	**G14**	GND6	NA	NA	GND	NA	NA	Power	Ground.
255	**G15**	LA12_P	B2B Connector 1	D13	X5_BD44_LVDS710_L1P_XCC	710	BD44	IO, 1.2V	PL Bank710 IO1 differential positive.
256	**G16**	LA12_N	B2B Connector 1	D14	X5_BC45_LVDS710_L1N_XCC	710	BC45	IO, 1.2V	PL Bank710 IO1differential positive.
257	**G17**	GND7	NA	NA	GND	NA	NA	Power	Ground.
258	**G18**	LA16_P	B2B Connector 1	B9	X5_AY36_LVDS711_L18P	711	AY36	IO, 1.2V	PL Bank711 IO18 differential positive.
259	**G19**	LA16_N	B2B Connector 1	B10	X5_BA37_LVDS711_L18N	711	BA37	IO, 1.2V	PL Bank711 IO18 differential negative.
260	**G20**	GND8	NA	NA	GND	NA	NA	Power	Ground.
261	**G21**	LA20_P	B2B Connector 1	B13	X5_AW40_LVDS711_L22P	711	AW40	IO, 1.2V	PL Bank711 IO22 differential positive.
262	**G22**	LA20_N	B2B Connector 1	B14	X5_AY41_LVDS711_L22N	711	AY41	IO, 1.2V	PL Bank711 IO22 differential negative.
263	**G23**	GND9	NA	NA	GND	NA	NA	Power	Ground.
264	**G24**	LA22_P	B2B Connector 1	D15	X5_BA41_LVDS711_L25P_XCC	711	BA41	IO, 1.2V	PL Bank711 IO25 differential positive.
265	**G25**	LA22_N	B2B Connector 1	D16	X5_AY42_LVDS711_L25N_XCC	711	AY42	IO, 1.2V	PL Bank711 IO25 differential negative.
266	**G26**	GND10	NA	NA	GND	NA	NA	Power	Ground.
267	**G27**	LA25_P	B2B Connector 1	D18	X5_BB42_LVDS711_L24P	711	BB42	IO, 1.2V	PL Bank711 IO24 differential positive.
268	**G28**	LA25_N	B2B Connector 1	D19	X5_BA43_LVDS711_L24N	711	BA43	IO, 1.2V	PL Bank711 IO24 differential negative.
269	**G29**	GND11	NA	NA	GND	NA	NA	Power	Ground.
270	**G30**	LA29_P	B2B Connector 1	C20	X5_BB43_LVDS711_L29P_XCC	711	BB43	IO, 1.2V	PL Bank711 IO29 differential positive.
271	**G31**	LA29_N	B2B Connector 1	C21	X5_BA44_LVDS711_L29N_XCC	711	BA44	IO, 1.2V	PL Bank711 IO29 differential negative.
272	**G32**	GND12	NA	NA	GND	NA	NA	Power	Ground.
273	**G33**	LA31_P	B2B Connector 1	B18	X5_AT46_LVDS712_L2P	712	AT46	IO, 1.2V	PL Bank712 IO2 differential positive.
274	**G34**	LA31_N	B2B Connector 1	B19	X5_AR46_LVDS712_L2N	712	AR46	IO, 1.2V	PL Bank712 IO2 differential negative.
275	**G35**	GND13	NA	NA	GND	NA	NA	Power	Ground.
276	**G36**	LA33_P	B2B Connector 1	B22	X5_AT40_LVDS712_L6P	712	AT40	IO, 1.2V	PL Bank712 IO6 differential positive.
277	**G37**	LA33_N	B2B Connector 1	B23	X5_AR40_LVDS712_L6N	712	AR40	IO, 1.2V	PL Bank712 IO6 differential negative.
278	**G38**	GND14	NA	NA	GND	NA	NA	Power	Ground.
279	**G39**	VADJ	NA	NA	NA	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
280	**G40**	GND15	NA	NA	GND	NA	NA	Power	Ground.
281	**H1**	VREF_A_M2C	NA	NA	NA	NA	NA	NA	NC
282	**H2**	PRSNT_M2C_L	NA	NA	NA	NA	NA	I, 3.3V	Module Present Signal. This Pin is connected to 6th pin of IO Expander (U47).
283	**H3**	GND1	NA	NA	GND	NA	NA	Power	Ground.
284	**H4**	CLK0_M2C_P	B2B Connector 1	D27	X5_AR38_LVDS712_L10P	712	AR38	IO, 1.2V	PL Bank712 IO10 differential positive.
285	**H5**	CLK0_M2C_N	B2B Connector 1	D28	X5_AT39_LVDS712_L10N	712	AT39	IO, 1.2V	PL Bank712 IO10 differential negative.
286	**H6**	GND2	NA	NA	GND	NA	NA	Power	Ground.
287	**H7**	LA02_P	B2B Connector 1	D2	X5_BE36_LVDS710_L15P	710	BE36	IO, 1.2V	PL Bank710 IO15 differential positive.
288	**H8**	LA02_N	B2B Connector 1	D3	X5_BE37_LVDS710_L15N	710	BE37	IO, 1.2V	PL Bank710 IO15 differential negative.
289	**H9**	GND3	NA	NA	GND	NA	NA	Power	Ground.
290	**H10**	LA04_P	B2B Connector 1	D6	X5_BC36_LVDS710_L13P_XCC	710	BC36	IO, 1.2V	PL Bank710 IO13 differential positive.
291	**H11**	LA04_N	B2B Connector 1	D7	X5_BB36_LVDS710_L13N_XCC	710	BB36	IO, 1.2V	PL Bank710 IO13 differential negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
292	H12	GND4	NA	NA	GND	NA	NA	Power	Ground.
293	H13	LA07_P	B2B Connector 1	C6	X5_BD37_LVDS710_L10P	710	BD37	IO, 1.2V	PL Bank710 IO10 differential positive.
294	H14	LA07_N	B2B Connector 1	C7	X5_BD38_LVDS710_L10N	710	BD38	IO, 1.2V	PL Bank710 IO10 differential negative.
295	H15	GND5	NA	NA	GND	NA	NA	Power	Ground.
296	H16	LA11_P	B2B Connector 1	A2	X5_BD40_LVDS710_L6P	710	BD40	IO, 1.2V	PL Bank710 IO6 differential positive.
297	H17	LA11_N	B2B Connector 1	A3	X5_BD41_LVDS710_L6N	710	BD41	IO, 1.2V	PL Bank710 IO6 differential negative.
298	H18	GND6	NA	NA	GND	NA	NA	Power	Ground.
299	H19	LA15_P	B2B Connector 1	C13	X5_BB34_LVDS711_L16P	711	BB34	IO, 1.2V	PL Bank711 IO16 differential positive.
300	H20	LA15_N	B2B Connector 1	C14	X5_BA34_LVDS711_L16N	711	BA34	IO, 1.2V	PL Bank711 IO16 differential negative.
301	H21	GND7	NA	NA	GND	NA	NA	Power	Ground.
302	H22	LA19_P	B2B Connector 1	B11	X5_AY39_LVDS711_L20P	711	AY39	IO, 1.2V	PL Bank711 IO20 differential positive.
303	H23	LA19_N	B2B Connector 1	B12	X5_AW39_LVDS711_L20N	711	AW39	IO, 1.2V	PL Bank711 IO20 differential negative.
304	H24	GND8	NA	NA	GND	NA	NA	Power	Ground.
305	H25	LA21_P	NA	NA	NA	NA	NA	NA	NC
306	H26	LA21_N	NA	NA	NA	NA	NA	NA	NC
307	H27	GND9	NA	NA	GND	NA	NA	Power	Ground.
308	H28	LA24_P	B2B Connector 1	B15	X5_AW42_LVDS711_L26P	711	AW42	IO, 1.2V	PL Bank711 IO26 differential positive.
309	H29	LA24_N	B2B Connector 1	B16	X5_AW43_LVDS711_L26N	711	AW43	IO, 1.2V	PL Bank711 IO26 differential negative.
310	H30	GND10	NA	NA	GND	NA	NA	Power	Ground.
311	H31	LA28_P	B2B Connector 1	C18	X5_BA46_LVDS711_L30P	711	BA46	IO, 1.2V	PL Bank711 IO30 differential positive.
312	H32	LA28_N	B2B Connector 1	C19	X5_AY46_LVDS711_L30N	711	AY46	IO, 1.2V	PL Bank711 IO30 differential negative.
313	H33	GND11	NA	NA	GND	NA	NA	Power	Ground.
314	H34	LA30_P	B2B Connector 1	C22	X5_AU44_LVDS712_L0P	712	AU44	IO, 1.2V	PL Bank712 IO0 differential positive.
315	H35	LA30_N	B2B Connector 1	C23	X5_AU45_LVDS712_L0N	712	AU45	IO, 1.2V	PL Bank712 IO0 differential negative.
316	H36	GND12	NA	NA	GND	NA	NA	Power	Ground.
317	H37	LA32_P	B2B Connector 1	B20	X5_AR44_LVDS712_L1P_XCC	712	AR44	IO, 1.2V	PL Bank712 IO1 differential positive.
318	H38	LA32_N	B2B Connector 1	B21	X5_AT45_LVDS712_L1N_XCC	712	AT45	IO, 1.2V	PL Bank712 IO1 differential negative.
319	H39	GND13	NA	NA	GND	NA	NA	Power	Ground.
320	H40	VADJ	NA	NA	NA	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
321	J1	GND1	NA	NA	GND	NA	NA	Power	Ground.
322	J2	CLK3_BIDIR_P	B2B Connector 3	D5	X5_BB25_LVDS707_L20N	707	BB25	IO, 1.2V	PL Bank707 IO20 differential negative.
323	J3	CLK3_BIDIR_N	B2B Connector 3	D6	X5_BB24_LVDS707_L20P	707	BB24	IO, 1.2V	PL Bank707 IO20 differential positive.
324	J4	GND2	NA	NA	GND	NA	NA	Power	Ground.
325	J5	GND3	NA	NA	GND	NA	NA	Power	Ground.
326	J6	HA03_P	B2B Connector 1	D29	X5_AR41_LVDS712_L9P_XCC	712	AR41	IO, 1.2V	PL Bank712 IO9 differential positive.
327	J7	HA03_N	B2B Connector 1	D30	X5_AT42_LVDS712_L9N_XCC	712	AT42	IO, 1.2V	PL Bank712 IO9 differential negative.
328	J8	GND4	NA	NA	GND	NA	NA	Power	Ground.
329	J9	HA07_P	B2B Connector 1	B25	X5_AW36_LVDS712_L15P	712	AW36	IO, 1.2V	PL Bank712 IO15 differential positive.
330	J10	HA07_N	B2B Connector 1	B26	X5_AW37_LVDS712_L15N	712	AW37	IO, 1.2V	PL Bank712 IO15 differential negative.
331	J11	GND5	NA	NA	GND	NA	NA	Power	Ground.
332	J12	HA11_P	B2B Connector 1	A27	X5_AL36_LVDS713_L17P_XCC	713	AL36	IO, 1.2V	PL Bank713 IO17 differential positive.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
333	**J13**	HA11_N	B2B Connector 1	A28	X5_AM37_LVDS713_L17N_XCC	713	AM37	IO, 1.2V	PL Bank713 IO17 differential negative.
334	**J14**	GND6	NA	NA	GND	NA	NA	Power	Ground.
335	**J15**	HA14_P	B2B Connector 1	C31	X5_AN39_LVDS713_L22P	713	AN39	IO, 1.2V	PL Bank713 IO22 differential positive.
336	**J16**	HA14_N	B2B Connector 1	C32	X5_AN40_LVDS713_L22N	713	AN40	IO, 1.2V	PL Bank713 IO22 differential negative.
337	**J17**	GND7	NA	NA	GND	NA	NA	Power	Ground.
338	**J18**	HA18_P	B2B Connector 3	D16	HDIO_W46_BANK400_L0P	400	W46	IO, 1.8V	PL Bank400 IO0 differential positive.
339	**J19**	HA18_N	B2B Connector 3	D17	HDIO_V46_BANK400_L0N	400	V46	IO, 1.8V	PL Bank400 IO0 differential negative.
340	**J20**	GND8	NA	NA	GND	NA	NA	Power	Ground.
341	**J21**	HA22_P	B2B Connector 3	C18	HDIO_W39_BANK400_L9P	400	W39	IO, 1.8V	PL Bank400 IO9 differential positive.
342	**J22**	HA22_N	B2B Connector 3	C19	HDIO_W40_BANK400_L9N	400	W40	IO, 1.8V	PL Bank400 IO9 differential negative.
343	**J23**	GND9	NA	NA	GND	NA	NA	Power	Ground.
344	**J24**	HB01_P	B2B Connector 3	D23	HDIO_Y38_BANK400_L10P	400	Y38	IO, 1.8V	PL Bank400 IO10 differential positive.
345	**J25**	HB01_N	B2B Connector 3	D24	HDIO_W38_BANK400_L10N	400	W38	IO, 1.8V	PL Bank400 IO10 differential negative.
346	**J26**	GND10	NA	NA	GND	NA	NA	Power	Ground.
347	**J27**	HB07_P	B2B Connector 3	C30	HDIO_U45_BANK402_L1P	402	R45	IO, 1.8V	PL Bank402 IO1 differential positive.
348	**J28**	HB07_N	B2B Connector 3	C31	HDIO_U46_BANK402_L1N	402	R46	IO, 1.8V	PL Bank402 IO1 differential negative.
349	**J29**	GND11	NA	NA	GND	NA	NA	Power	Ground.
350	**J30**	HB11_P	B2B Connector 3	D39	HDIO_U39_BANK402_L8P	402	U39	IO, 1.8V	PL Bank402 IO8 differential positive.
351	**J31**	HB11_N	B2B Connector 3	D40	HDIO_T40_BANK402_L8N	402	T40	IO, 1.8V	PL Bank402 IO8 differential negative.
352	**J32**	GND12	NA	NA	GND	NA	NA	Power	Ground.
353	**J33**	HB15_P	B2B Connector 1	A11	X5_BB40_LVDS711_L23P	711	BB40	IO, 1.2V	PL Bank711 IO23 differential positive.
354	**J34**	HB15_N	B2B Connector 1	A12	X5_BA40_LVDS711_L23N	711	BA40	IO, 1.2V	PL Bank711 IO23 differential negative.
355	**J35**	GND13	NA	NA	GND	NA	NA	Power	Ground.
356	**J36**	HB18_P	B2B Connector 3	A38	X5_BD23_LVDS707_L25N	707	BD23	IO, 1.2V	PL Bank707 IO25 differential negative.
357	**J37**	HB18_N	B2B Connector 3	A39	X5_BD22_LVDS707_L25P	707	BD22	IO, 1.2V	PL Bank707 IO25 differential positive.
358	**J38**	GND14	NA	NA	GND	NA	NA	Power	Ground.
359	**J39**	VIO_B_M2C	NA	NA	NA	NA	NA	NA	No Connect
360	**J40**	GND15	NA	NA	GND	NA	NA	Power	Ground.
361	**K1**	VREF_B_M2C	NA	NA	NC	NA	NA	NA	No Connect.
362	**K2**	GND1	NA	NA	GND	NA	NA	Power	Ground.
363	**K3**	GND2	NA	NA	GND	NA	NA	Power	Ground.
364	**K4**	CLK2_BIDIR_P	NA	NA	NA	NA	NA	NA	No Connect.
365	**K5**	CLK2_BIDIR_N	NA	NA	NA	NA	NA	NA	No Connect.
366	**K6**	GND3	NA	NA	GND	NA	NA	Power	Ground.
367	**K7**	HA02_P	B2B Connector 1	A18	X5_AV43_LVDS712_L5P_XCC	712	AV43	IO, 1.2V	PL Bank712 IO5 differential positive.
368	**K8**	HA02_N	B2B Connector 1	A19	X5_AV44_LVDS712_L5N_XCC	712	AV44	IO, 1.2V	PL Bank712 IO5 differential negative.
369	**K9**	GND4	NA	NA	GND	NA	NA	Power	Ground.
370	**K10**	HA06_P	B2B Connector 1	C29	X5_AV37_LVDS712_L12P	712	AV37	IO, 1.2V	PL Bank712 IO12 differential positive.
371	**K11**	HA06_N	B2B Connector 1	C30	X5_AV38_LVDS712_L12N	712	AV38	IO, 1.2V	PL Bank712 IO12 differential negative.
372	**K12**	GND5	NA	NA	GND	NA	NA	Power	Ground.
373	**K13**	HA10_P	B2B Connector 1	A25	X5_AR35_LVDS713_L16P	713	AR35	IO, 1.2V	PL Bank713 IO16 differential positive.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
374	**K14**	HA10_N	B2B Connector 1	A26	X5_AP36_LVDS713_L16N	713	AP36	IO, 1.2V	PL Bank713 IO16 differential negative.
375	**K15**	GND6	NA	NA	GND	NA	NA	Power	Ground.
376	**K16**	HA17_P_CC	B2B Connector 1	A20	X5_AT43_LVDS712_L4P	712	AT43	IO, 1.2V	PL Bank712 IO4 differential positive.
377	**K17**	HA17_N_CC	B2B Connector 1	A21	X5_AR43_LVDS712_L4N	712	AR43	IO, 1.2V	PL Bank712 IO4 differential negative.
378	**K18**	GND7	NA	NA	GND	NA	NA	Power	Ground.
379	**K19**	HA21_P	B2B Connector 3	C16	HDIO_AA44_BANK400_L2P	400	AA44	IO, 1.8V	PL Bank400 IO2 differential positive.
380	**K20**	HA21_N	B2B Connector 3	C17	HDIO_AA45_BANK400_L2N	400	AA45	IO, 1.8V	PL Bank400 IO2 differential negative.
381	**K21**	GND8	NA	NA	GND	NA	NA	Power	Ground.
382	**K22**	HA23_P	B2B Connector 3	D21	HDIO_Y43_BANK400_L4P	400	Y43	IO, 1.8V	PL Bank400 IO4 differential positive.
383	**K23**	HA23_N	B2B Connector 3	D22	HDIO_W43_BANK400_L4N	400	W43	IO, 1.8V	PL Bank400 IO4 differential negative.
384	**K24**	GND9	NA	NA	GND	NA	NA	Power	Ground.
385	**K25**	HB00_P_CC	B2B Connector 3	C25	HDIO_AA42_BANK400_HDGC_L5P	400	AA42	IO, 1.8V	PL Bank400 IO5 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
386	**K26**	HB00_N_CC	B2B Connector 3	C26	HDIO_AA43_BANK400_HDGC_L5N	400	AA43	IO, 1.8V	PL Bank400 IO5 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
387	**K27**	GND10	NA	NA	GND	NA	NA	Power	Ground.
388	**K28**	HB06_P_CC	B2B Connector 3	D28	HDIO_V41_BANK402_HDGC_L6P	402	V41	IO, 1.8V	PL Bank402 IO6 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
389	**K29**	HB06_N_CC	B2B Connector 3	D29	HDIO_U42_BANK402_HDGC_L6N	402	U42	IO, 1.8V	PL Bank402 IO6 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
390	**K30**	GND11	NA	NA	GND	NA	NA	Power	Ground.
391	**K31**	HB10_P	B2B Connector 3	D37	HDIO_V38_BANK402_L9P	402	V38	IO, 1.8V	PL Bank402 IO9 differential positive.
392	**K32**	HB10_N	B2B Connector 3	D38	HDIO_V39_BANK402_L9N	402	V39	IO, 1.8V	PL Bank402 IO9 differential negative.
393	**K33**	GND12	NA	NA	GND	NA	NA	Power	Ground.
394	**K34**	HB14_P	B2B Connector 3	C39	X5_AW21_LVDS707_L17P	707	AW21	IO, 1.2V	PL Bank707 IO17 differential positive.
395	**K35**	HB14_N	B2B Connector 3	C40	X5_AY21_LVDS707_L17N	707	AY21	IO, 1.2V	PL Bank707 IO17 differential negative.
396	**K36**	GND13	NA	NA	GND	NA	NA	Power	Ground.
397	**K37**	HB17_P_CC	B2B Connector 3	C23	HDIO_Y41_BANK400_HDGC_L6P	400	Y41	IO, 1.8V	PL Bank400 IO6 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
398	**K38**	HB17_N_CC	B2B Connector 3	C24	HDIO_Y42_BANK400_HDGC_L6N	400	Y42	IO, 1.8V	PL Bank400 IO6 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
399	**K39**	GND14	NA	NA	GND	NA	NA	Power	Ground.
400	**K40**	VIO_B_M2C	NA	NA	NC	NA	NA	NA	No Connect.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
401	**L1**	RES1	NA	NA	NC	NA	NA	NA	No Connect.
402	**L2**	GND2	NA	NA	GND	NA	NA	Power	Ground.
403	**L3**	GND3	NA	NA	GND	NA	NA	Power	Ground.
404	**L4**	GBTCLK4_M2C_P	B2B Connector 3	D1	NA	NA	NA	NA	No Connect.
405	**L5**	GBTCLK4_M2C_N	B2B Connector 3	D2	NA	NA	NA	NA	No Connect.
406	**L6**	GND4	NA	NA	GND	NA	NA	Power	Ground.
407	**L7**	GND5	NA	NA	GND	NA	NA	Power	Ground.
408	**L8**	GBTCLK3_M2C_P	B2B Connector 3	C11	X5_BC21_LVDS707_L23N	707	BC21	IO, 1.2V	PL Bank707 IO23 differential negative.
409	**L9**	GBTCLK3_M2C_N	B2B Connector 3	C12	X5_BC20_LVDS707_L23P	707	BC20	IO, 1.2V	PL Bank707 IO23 differential positive.
410	**L10**	GND6	NA	NA	GND	NA	NA	Power	Ground.
411	**L11**	GND7	NA	NA	GND	NA	NA	Power	Ground.
412	**L12**	GBTCLK2_M2C_P	B2B Connector 3	C7	GTYP_REFCLKP0_207	207	J40	I, DIFF	GTYP Bank207 channel0 High speed differential reference clock0 positive.
413	**L13**	GBTCLK2_M2C_N	B2B Connector 3	C8	GTYP_REFCLKN0_207	207	J41	I, DIFF	GTYP Bank207 channel0 High speed differential reference clock0 negative.
414	**L14**	GND8	NA	NA	GND	NA	NA	Power	Ground.
415	**L15**	GND9	NA	NA	GND	NA	NA	Power	Ground.
416	**L16**	SYNC_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
417	**L17**	SYNC_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
418	**L18**	GND10	NA	NA	GND	NA	NA	Power	Ground.
419	**L19**	GND11	NA	NA	GND	NA	NA	Power	Ground.
420	**L20**	REFCLK_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
421	**L21**	REFCLK_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
422	**L22**	GND12	NA	NA	GND	NA	NA	Power	Ground.
423	**L23**	GND13	NA	NA	GND	NA	NA	Power	Ground.
424	**L24**	REFCLK_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
425	**L25**	REFCLK_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
426	**L26**	GND14	NA	NA	GND	NA	NA	Power	Ground.
427	**L27**	GND15	NA	NA	GND	NA	NA	Power	Ground.
428	**L28**	SYNC_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
429	**L29**	SYNC_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
430	**L30**	GND16	NA	NA	GND	NA	NA	Power	Ground.
431	**L31**	GND17	NA	NA	GND	NA	NA	Power	Ground.
432	**L32**	RES2	NA	NA	NA	NA	NA	NA	No Connect.
433	**L33**	RES3	NA	NA	NA	NA	NA	NA	No Connect.
434	**L34**	GND18	NA	NA	GND	NA	NA	Power	Ground.
435	**L35**	GND19	NA	NA	GND	NA	NA	Power	Ground.
436	**L36**	12P0V	NA	NA	VCC_12V_FMC+	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
437	**L37**	12P0V	NA	NA	VCC_12V_FMC+	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
438	**L38**	GND20	NA	NA	GND	NA	NA	Power	Ground.
439	**L39**	GND37	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
440	**L40**	12P0V	NA	NA	VCC_12V_FMC+	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
441	**M1**	GND1	NA	NA	GND	NA	NA	Power	Ground.
442	**M2**	DP23_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
443	**M3**	DP23_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
444	**M4**	GND2	NA	NA	GND	NA	NA	Power	Ground.
445	**M5**	GND3	NA	NA	GND	NA	NA	Power	Ground.
446	**M6**	DP22_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
447	**M7**	DP22_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
448	**M8**	GND4	NA	NA	GND	NA	NA	Power	Ground.
449	**M9**	GND5	NA	NA	GND	NA	NA	Power	Ground.
450	**M10**	DP21_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
451	**M11**	DP21_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
452	**M12**	GND6	NA	NA	GND	NA	NA	Power	Ground.
453	**M13**	GND7	NA	NA	GND	NA	NA	Power	Ground.
454	**M14**	DP20_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
455	**M15**	DP20_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
456	**M16**	GND8	NA	NA	GND	NA	NA	Power	Ground.
457	**M17**	GND9	NA	NA	GND	NA	NA	Power	Ground.
458	**M18**	DP14_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
459	**M19**	DP14_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
460	**M20**	GND10	NA	NA	GND	NA	NA	Power	Ground.
461	**M21**	GND11	NA	NA	GND	NA	NA	Power	Ground.
462	**M22**	DP15_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
463	**M23**	DP15_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
464	**M24**	GND12	NA	NA	GND	NA	NA	Power	Ground.
465	**M25**	GND13	NA	NA	GND	NA	NA	Power	Ground.
466	**M26**	DP16_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
467	**M27**	DP16_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
468	**M28**	GND14	NA	NA	GND	NA	NA	Power	Ground.
469	**M29**	GND15	NA	NA	GND	NA	NA	Power	Ground.
470	**M30**	DP17_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
471	**M31**	DP17_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
472	**M32**	GND16	NA	NA	GND	NA	NA	Power	Ground.
473	**M33**	GND17	NA	NA	GND	NA	NA	Power	Ground.
474	**M34**	DP18_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
475	**M35**	DP18_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
476	**M36**	GND18	NA	NA	GND	NA	NA	Power	Ground.
477	**M37**	GND19	NA	NA	GND	NA	NA	Power	Ground.
478	**M38**	DP19_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
479	**M39**	DP19_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
480	**M40**	GND20	NA	NA	GND	NA	NA	Power	Ground.
481	**Y1**	GND1	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
482	**Y2**	DP23_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
483	**Y3**	DP23_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
484	**Y4**	GND2	NA	NA	GND	NA	NA	Power	Ground.
485	**Y5**	GND3	NA	NA	GND	NA	NA	Power	Ground.
486	**Y6**	DP21_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
487	**Y7**	DP21_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
488	**Y8**	GND4	NA	NA	GND	NA	NA	Power	Ground.
489	**Y9**	GND5	NA	NA	GND	NA	NA	Power	Ground.
490	**Y10**	DP10_M2C_P	B2B Connector 3	B17	GTYP_RXP2_207	207	B32	I, DIFF	GTYP Bank207 channel2 High speed differential receiver positive.
491	**Y11**	DP10_M2C_N	B2B Connector 3	B18	GTYP_RXN2_207	207	A32	I, DIFF	GTYP Bank207 channel2 High speed differential receiver negative.
492	**Y12**	GND6	NA	NA	GND	NA	NA	Power	Ground.
493	**Y13**	GND7	NA	NA	GND	NA	NA	Power	Ground.
494	**Y14**	DP12_M2C_P	B2B Connector 3	B25	X5_AY24_LVDS707_L22N	707	AY24	IO, 1.2V	PL Bank707 IO22 differential negative.
495	**Y15**	DP12_M2C_N	B2B Connector 3	B26	X5_AY23_LVDS707_L22P	707	AY23	IO, 1.2V	PL Bank707 IO22 differential positive.
496	**Y16**	GND8	NA	NA	GND	NA	NA	Power	Ground.
497	**Y17**	GND9	NA	NA	GND	NA	NA	Power	Ground.
498	**Y18**	DP14_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
499	**Y19**	DP14_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
500	**Y20**	GND10	NA	NA	GND	NA	NA	Power	Ground.
501	**Y21**	GND11	NA	NA	GND	NA	NA	Power	Ground.
502	**Y22**	DP15_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
503	**Y23**	DP15_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
504	**Y24**	GND12	NA	NA	GND	NA	NA	Power	Ground.
505	**Y25**	GND13	NA	NA	GND	NA	NA	Power	Ground.
506	**Y26**	DP11_C2M_P	B2B Connector 3	B2	GTYP_TXP3_207	207	E31	O, DIFF	GTYP Bank207 channel3 High speed differential transmitter positive.
507	**Y27**	DP11_C2M_N	B2B Connector 3	B1	GTYP_TXN3_207	207	D31	O, DIFF	GTYP Bank207 channel3 High speed differential transmitter negative.
508	**Y28**	GND14	NA	NA	GND	NA	NA	Power	Ground.
509	**Y29**	GND15	NA	NA	GND	NA	NA	Power	Ground.
510	**Y30**	DP13_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
511	**Y31**	DP13_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
512	**Y32**	GND16	NA	NA	GND	NA	NA	Power	Ground.
513	**Y33**	GND17	NA	NA	GND	NA	NA	Power	Ground.
514	**Y34**	DP17_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
515	**Y35**	DP17_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
516	**Y36**	GND18	NA	NA	GND	NA	NA	NA	Ground.
517	**Y37**	GND19	NA	NA	GND	NA	NA	Power	Ground.
518	**Y38**	DP19_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
519	**Y39**	DP19_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
520	**Y40**	GND20	NA	NA	GND	NA	NA	Power	Ground.
521	**Z1**	HSPC_PRSNT_M2C_L	NA	NA	NA	NA	NA	I, 3.3V	FMC+ Module Present Signal. This Pin is connected to 7th pin of IO Expander 2 (U47).
522	**Z2**	GND2	NA	NA	GND	NA	NA	Power	Ground.
523	**Z3**	GND3	NA	NA	GND	NA	NA	Power	Ground.
524	**Z4**	DP22_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
525	**Z5**	DP22_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
526	**Z6**	GND6	NA	NA	GND	NA	NA	Power	Ground.
527	**Z7**	GND7	NA	NA	GND	NA	NA	Power	Ground.
528	**Z8**	DP20_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
529	**Z9**	DP20_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
530	**Z10**	GND8	NA	NA	GND	NA	NA	Power	Ground.
531	**Z11**	GND9	NA	NA	GND	NA	NA	Power	Ground.
532	**Z12**	DP11_M2C_P	B2B Connector 3	A19	GTYP_RXP3_207	207	B30	I, DIFF	GTYP Bank207 channel3 High speed differential receiver positive.
533	**Z13**	DP11_M2C_N	B2B Connector 3	A20	GTYP_RXN3_207	207	A30	I, DIFF	GTYP Bank207 channel3 High speed differential receiver negative.
534	**Z14**	GND10	NA	NA	GND	NA	NA	Power	Ground.
535	**Z15**	GND11	NA	NA	GND	NA	NA	Power	Ground.
536	**Z16**	DP13_M2C_P	B2B Connector 3	A27	X5_BC23_LVDS707_L24P	707	BC23	IO, 1.2V	PL Bank707 IO24 differential positive.
537	**Z17**	DP13_M2C_N	B2B Connector 3	A28	X5_BC24_LVDS707_L24N	707	BC24	IO, 1.2V	PL Bank707 IO24 differential negative.
538	**Z18**	GND12	NA	NA	GND	NA	NA	Power	Ground.
539	**Z19**	GND13	NA	NA	GND	NA	NA	Power	Ground.
540	**Z20**	GBTCLK5_M2C_P	B2B Connector 3	C3	NA	NA	NA	NA	No Connect.
541	**Z21**	GBTCLK5_M2C_N	B2B Connector 3	C4	NA	NA	NA	NA	No Connect.
542	**Z22**	GND14	NA	NA	GND	NA	NA	Power	Ground.
543	**Z23**	GND15	NA	NA	GND	NA	NA	Power	Ground.
544	**Z24**	DP10_C2M_P	B2B Connector 3	A4	GTYP_TXP2_207	207	E33	O, DIFF	GTYP Bank207 channel2 High speed differential transmitter positive.
545	**Z25**	DP10_C2M_N	B2B Connector 3	A3	GTYP_TXN2_207	207	D33	O, DIFF	GTYP Bank207 channel2 High speed differential transmitter negative.
546	**Z26**	GND16	NA	NA	GND	NA	NA	Power	Ground.
547	**Z27**	GND17	NA	NA	GND	NA	NA	Power	Ground.
548	**Z28**	DP12_C2M_P	NA	NA	NA	NA	NA	NA	No Connect.
549	**Z29**	DP12_C2M_N	NA	NA	NA	NA	NA	NA	No Connect.
550	**Z30**	GND18	NA	NA	GND	NA	NA	Power	Ground.
551	**Z31**	GND19	NA	NA	GND	NA	NA	Power	Ground.
552	**Z32**	DP16_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
553	**Z33**	DP16_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
554	**Z34**	GND20	NA	NA	GND	NA	NA	Power	Ground.
555	**Z35**	GND21	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Versal AI Edge Gen2 SOM (SSVA2112)			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination*	
556	**Z36**	DP18_M2C_P	NA	NA	NA	NA	NA	NA	No Connect.
557	**Z37**	DP18_M2C_N	NA	NA	NA	NA	NA	NA	No Connect.
558	**Z38**	GND22	NA	NA	GND	NA	NA	Power	Ground.
559	**Z39**	GND23	NA	NA	GND	NA	NA	Power	Ground.
560	**Z40**	3P3V	NA	NA	NA	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.

2.7.7 Pmod Host Port Connector

Pmod interface or Peripheral Module interface is a standard defined by Digilent Inc. The Pmod interface is used to connect low frequency, low I/O pin count peripheral modules to host controller boards.

The Versal AI Edge Gen2 development board supports one 12pin Pmod host port connector for plugging Pmod module. Since Pmod interface specification requires 3.3V IO level, the signals from Board-to-Board connector are connected to Pmod Connectors through Voltage level translator. Pmod Host port connector (J22) is physically located at the bottom of the board as shown below.

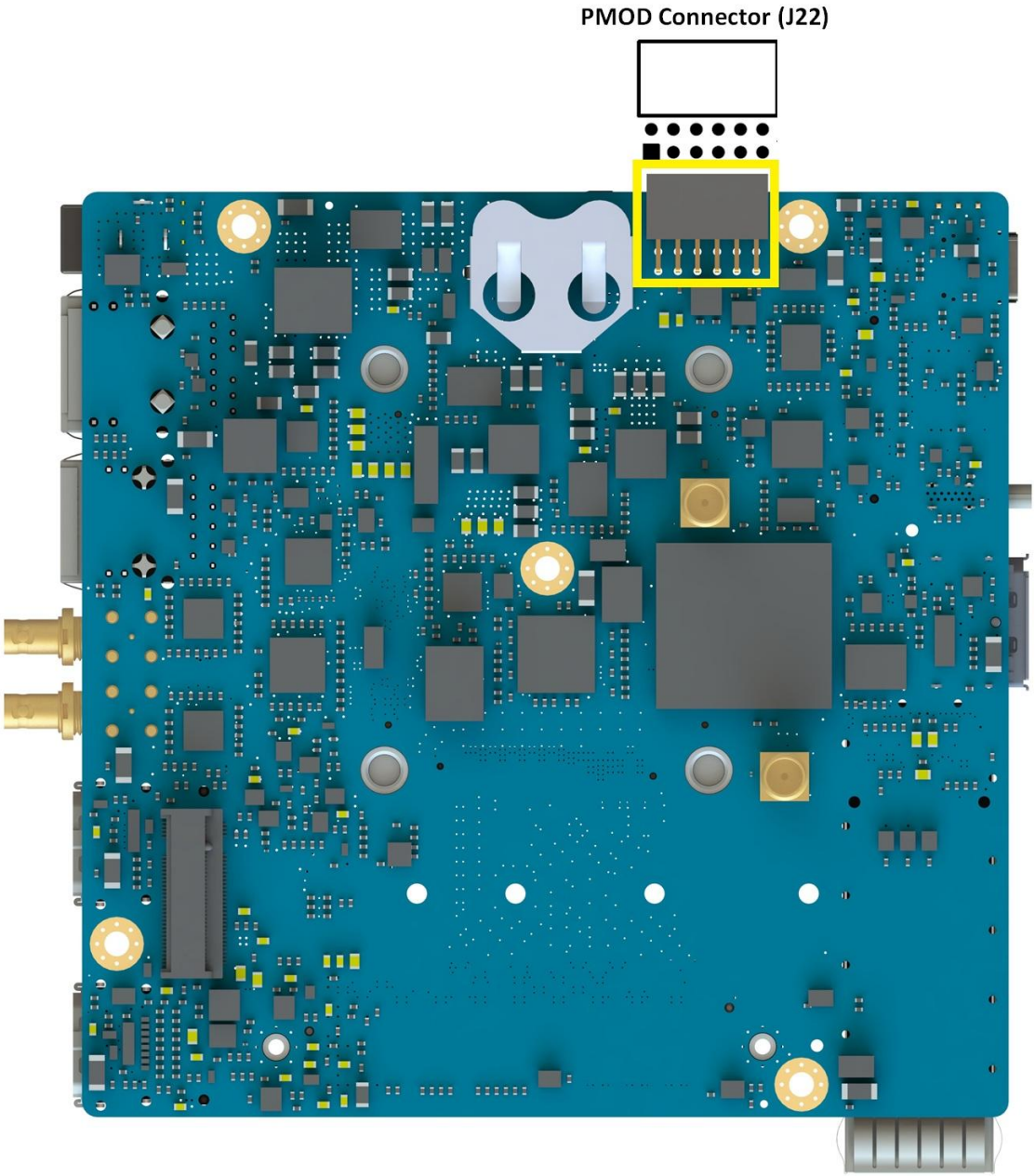


Figure 17: PMOD Host Connector

Table 10: PMOD Connector Pin Assignment

Pin No	Signal Name	SoC Pin Name	SoC Pin Number	Signal Type/ Termination	Description
1	BANK2_IO11N_GCIN2N	IO_L2N_H0O0P5_706	BE15	IO, 3V3 LVCMOS	General purpose Input Output
2	BANK2_IO12N_GCIN0N	IO_L3N_GC_H0O0P7_706	BC15	IO, 3V3 LVCMOS	General purpose Input Output
3	BANK2_IO8N	IO_L28N_H1O3P1_M3P121_713	AL44	IO, 3V3 LVCMOS	General purpose Input Output
4	BANK2_IO7N	IO_L30N_H1O3P5_M3P125_713	AM46	IO, 3V3 LVCMOS	General purpose Input Output
5	GND	NA	NA	Power	Ground.
6	VCC_3V3	NA	NA	O, 3.3V Power	3V3 Supply Voltage.
7	BANK2_IO11P_GCIN2P	IO_L2P_H0O0P4_706	BD16	IO, 3V3 LVCMOS	General purpose Input Output
8	BANK2_IO12P_GCIN0P	IO_L3P_GC_H0O0P6_706	BC14	IO, 3V3 LVCMOS	General purpose Input Output
9	BANK2_IO8P	IO_L28P_H1O3P0_M3P120_713	AM44	IO, 3V3 LVCMOS	General purpose Input Output
10	BANK2_IO7P	IO_L30P_H1O3P4_M3P124_713	AN45	IO, 3V3 LVCMOS	General purpose Input Output
11	GND	NA	NA	Power	Ground.
12	VCC_3V3	NA	NA	O, 3.3V Power	3V3 Supply Voltage.

2.8 PS Interface Features

The features which are supported from Versal AI Edge Gen2 processor is explained in the following section. The PS-GTR Lane selection switch (SW2) setting and corresponding interface selection option is explained below.

PS-GTR Lanes	PS-GTR Lane Selection Switch (SW2)		
	Switch Bit Number	Switch Bit Position	
		OFF	ON
Lane0	**-**	PS-GTR Lane0 is connected to Lane0 of PCIe x4 connector	
Lane1	**Bit2.1**	-	PS-GTR Lane1 is connected to USB3.0 connector (default)
Lane2	**Bit2.2**	-	PS-GTR Lane2 is connected to MUX/DEMUX IC (U38) (default)
Lane3		-	PS-GTR Lane3 is connected Lane0 of DP Connector (default)
-	**Bit2.3**	-	PS GTR Lane2 is connected to Lane1 of DP Connector.

2.8.1 PCIe x4 Connector

The Versal AI Edge Gen2 development board supports one PCIe x4 connector through PS-GTYP Transceivers of Versal AI Edge Gen2 SOM. Only the first lane of PS-GTYP transceiver, Bank 105 from Board-to-Board Connector is connected to PCIe x4 connector (J6) to support x1 PCIe devices. The devkit supports Root port mode and endpoint mode. In root port mode transceiver and PCIe connector clock, 100MHz is provided from on board Clock Synthesizer. In the Endpoint mode, connector clock is connected to transceiver reference clock. Dedicated reset from LS_PCIe_RSTn pin from board to connector2 is used for PCIe reset, this pin is from MIO bank 501 (PMC_MIO30_501).

The devkit supports both PCIe Root port and End point configuration and change the SW2 status as per below table to support the configuration.

PCIe Select Switch (SW2)		
Mode	**SW2.4**	**Switch Position Image**
End Point	1	
Root Port	0	

This PCIe x4 connector (J6) is physically located at the top of the board as shown below.

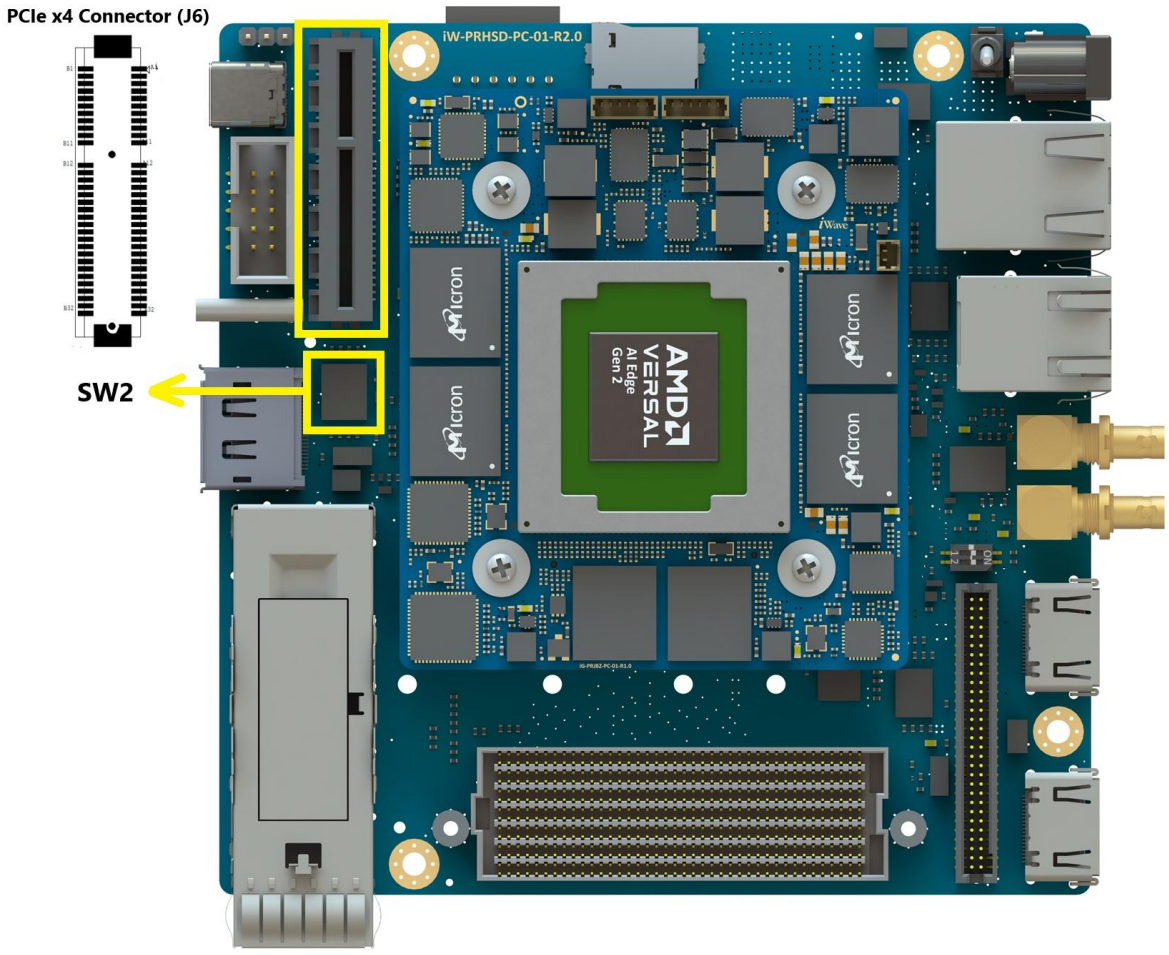


Figure 18: PCIe x4 Connector

Table 11: PCIe x4 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
A1	PRSNT1_N	PRSNT1	O, 3.3V CMOS	Present pin, default Grounded
A2	+12V	VCC_12V_PCIex4	O, 12V Power	12V Supply Voltage
A3	+12V	VCC_12V_PCIex4	O, 12V Power	12V Supply Voltage
A4	GND	GND	Power	Ground
A5	JTAG_TCK	NA	NA	NC
A6	JTAG_TDI	NA	NA	NC
A7	JTAG_TDO	NA	NA	NC
A8	JTAG_TMS	NA	NA	NC
A9	+3_3V	VCC_3V3_PCIex4	O, 3.3V Power	3.3V Supply Voltage
A10	+3_3V	VCC_3V3_PCIex4	O, 3.3V Power	3.3V Supply Voltage
A11	PERST_N	B_LS_PCIe_RSTn	IO, 3.3V LVCMOS	PCIe Reset through MIO Bank 501 IO. *Note: This signal is output from SOM to PCIe connector in root port mode and input to SOM from PCIe connector in Endpoint mode.*

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
A12	GND	GND	Power	Ground
A13	REFCLK+	PS_PCIex4_REFCLKP	IO, DIFF	100MHz PCIe Reference Clock positive *Note: This 100MHz clock is Input to PCIe connector for Root Port application from clock generator and output from PCIe connector to SOM for Endpoint application*
A14	REFCLK	PS_PCIex4_REFCLKn	IO, DIFF	100MHz PCIe Reference Clock negative *Note: This 100MHz clock is Input to PCIe connector for Root Port application from clock generator and output from PCIe connector to SOM for Endpoint application*
A15	GND	GND	Power	Ground
A16	PER0P	GTYP_MMI_RXP0_105	I, DIFF	PCIe Lane0 Receive pair positive.
A17	PER0N	GTYP_MMI_RXN0_105	I, DIFF	PCIe Lane0 Receive pair negative.
A18	GND	GND	Power	Ground
A19	RSVD2	NC	NA	NA
A20	GND	GND	Power	Ground
A21	PER1P	NC	NA	NA
A22	PER1N	NC	NA	NA
A23	GND	GND	Power	Ground
A24	GND	GND	Power	Ground
A25	PER2P	NC	NA	NA
A26	PER2N	NC	NA	NA
A27	GND	GND	Power	Ground
A28	GND	GND	Power	Ground
A29	PER3P	NC	NA	NA
A30	PER3N	NC	NA	NA
A31	GND	GND	Power	Ground
A32	RSVD4	NC	NA	NA
B1	+12V	VCC_12V_PCIex4	O, 12V Power	12V Supply Voltage.
B2	+12V	VCC_12V_PCIex4	O, 12V Power	12V Supply Voltage.
B3	RSVD1	NC	NA	NA
B4	GND	GND	Power	Ground
B5	SMCLK	NC	NA	NA
B6	SMDAT	NC	NA	NA
B7	GND	GND	Power	Ground
B8	+3_3V	VCC_3V3_PCIex4	O, 3.3V Power	3.3V Supply Voltage
B9	JTAG_TRSTN	NC	NA	NA
B10	+3_3VAUX	VCC_3V3_PCIex4	O, 3.3V Power	3.3V Supply Voltage
B11	WAKE_N	B_PCI_Wake	O, 3.3V CMOS	PCIe Wake. This pin is connected from P17th pin of IO Expander 2

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
B12	RSVD1	NC	NA	NA
B13	GND	GND	Power	Ground
B14	PET0P	GTYP_MMI_TXP0_105	O, DIFF	PCIe Lane0 Transmit pair positive
B15	PET0N	GTYP_MMI_TXN0_105	O, DIFF	PCIe Lane0 Transmit pair negative
B16	GND	GND	Power	Ground
B17	PRSNT2n_X1	PS_PCIe_PRSNTX1	NA	This signal is pulled up to 3.3V.
B18	GND	GND	Power	Ground
B19	PET1P	NC	NA	NA
B20	PET1N	NC	NA	NA
B21	GND	GND	Power	Ground
B22	GND	GND	Power	Ground
B23	PET2P	NC	NA	NA
B24	PET2N	NC	NA	NA
B25	GND	GND	Power	Ground
B26	GND	GND	Power	Ground
B27	PET3P	NC	NA	NA
B28	PET3N	NC	NA	NA
B29	GND	GND	Power	Ground
B30	RSVD3	NC	NA	NA
B31	PRSNT2n_X4	PS_PCIe_PRSNTX4	NA	This signal is pulled up to 3.3V.
B32	GND	GND	Power	Ground

2.8.2 Display Port Connector

The Versal AI Edge Gen2 SOM development board supports one Display port connector through dedicated Lanes of Versal AI Edge Gen2's PS-GTR. The PS-GTR Lane3 & Lane2 from Board-to-Board Connector1 is connected to Display port connector to support single or dual lane display port. The PS-GTR Lane selection to Display port connector is done through PS-GTR Lane Selection Switch (SW2). Make sure SW2.2 and SW2.3 is in ON position.

The Display port connector supports AUX+ & AUX- signals from the PS-DIO Bank 504. Also, it supports Hot plug detect signal and connected to IO Expander 1 (U18) P17th pin. This Display Port connector (J12) is physically located at the top of the board as shown below.

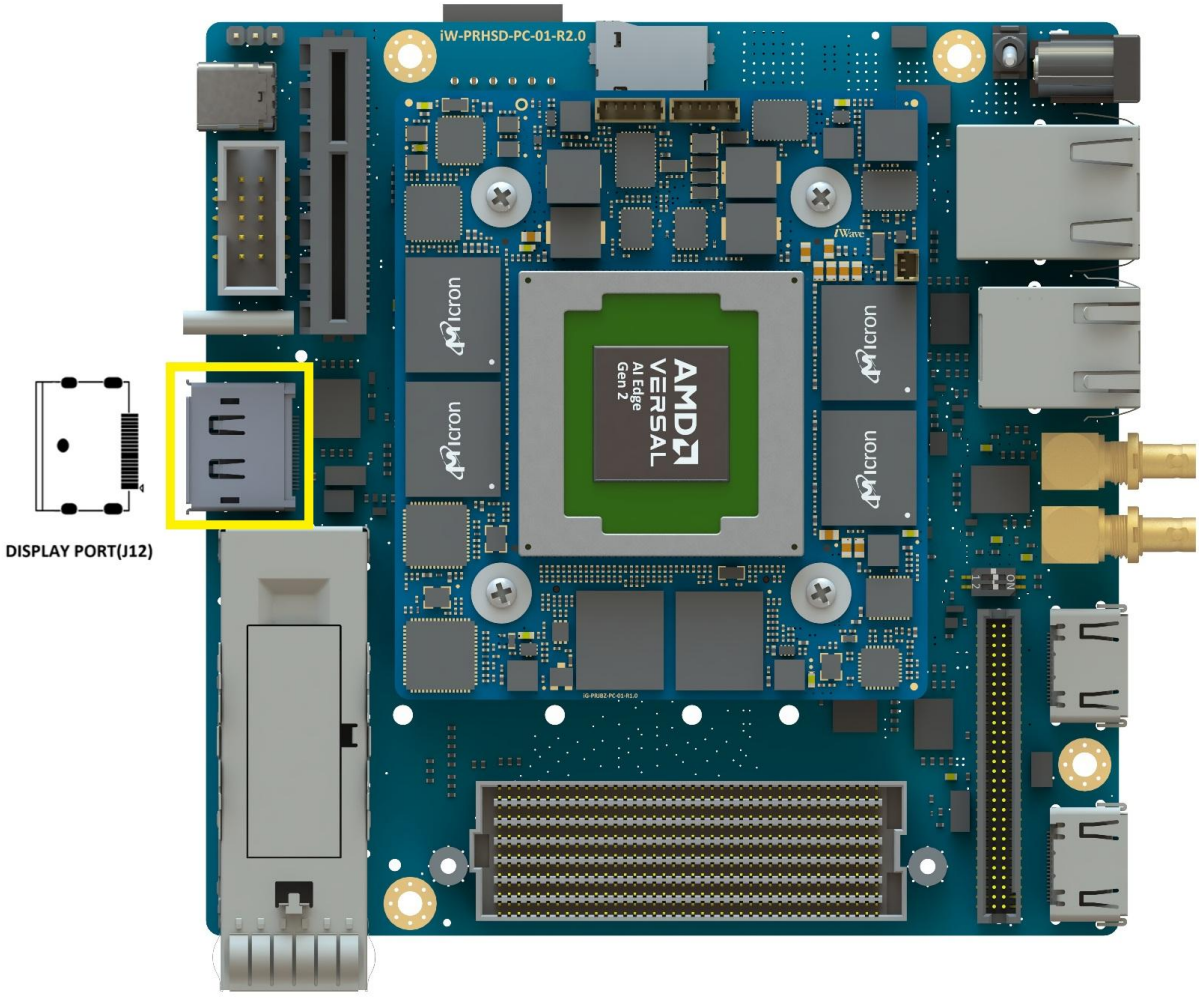


Figure 19: PCIe x4 Connector

2.8.3 USB Type-C Connector

The Versal AI Edge Gen2 Development Board supports one Super Speed USB3.0/USB2.0 High Speed OTG interface through USB2 Controller of Versal processor. This USB3.0/USB2.0 OTG interface is supported through USB Type-C connector (J4). The Versal AI Edge Gen2 SOM development board supports USB3.0 through dedicated Lanes of Versal AI Edge Gen2's PS-GTR. The PS-GTR Lane0 & Lane1 from Board-to-Board Connector1 is connected to USB Type-C connector (J4). The PS-GTR Lane selection to USB3.0 is done through PS-GTR Lane Selection Switch (SW2). Make sure SW2.1 is in ON position.

The Versal AI Edge Gen2 development board supports "FUSB302" USB Type-C controller for port detection & cable orientation and controlled through I2C0 from Port 0 of I2C Bus switch to support double-way plug in on USB Type-C connector. The "FUSB302" IC interrupt connected to IO Expander1 pin P07. The USB C Controller Lane is connected to "FUSB340" 2:1 data Switch which is further connected to USB Type-C connector. The lane selection to Type-C connector (top or bottom port) is controlled through IO Expander1. The VBUS power of this USB2.0 Type-C connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 500mA in host mode. The USB PHY transceiver in Versal detects the USB functionality through USB_OTG_ID pin (B17th pin of B2B-2) and controls the power using the USB_PWR_EN pin (B16th pin of B2B-2). This USB2.0 OTG connector (J4) is physically located at the top of the board as shown below.

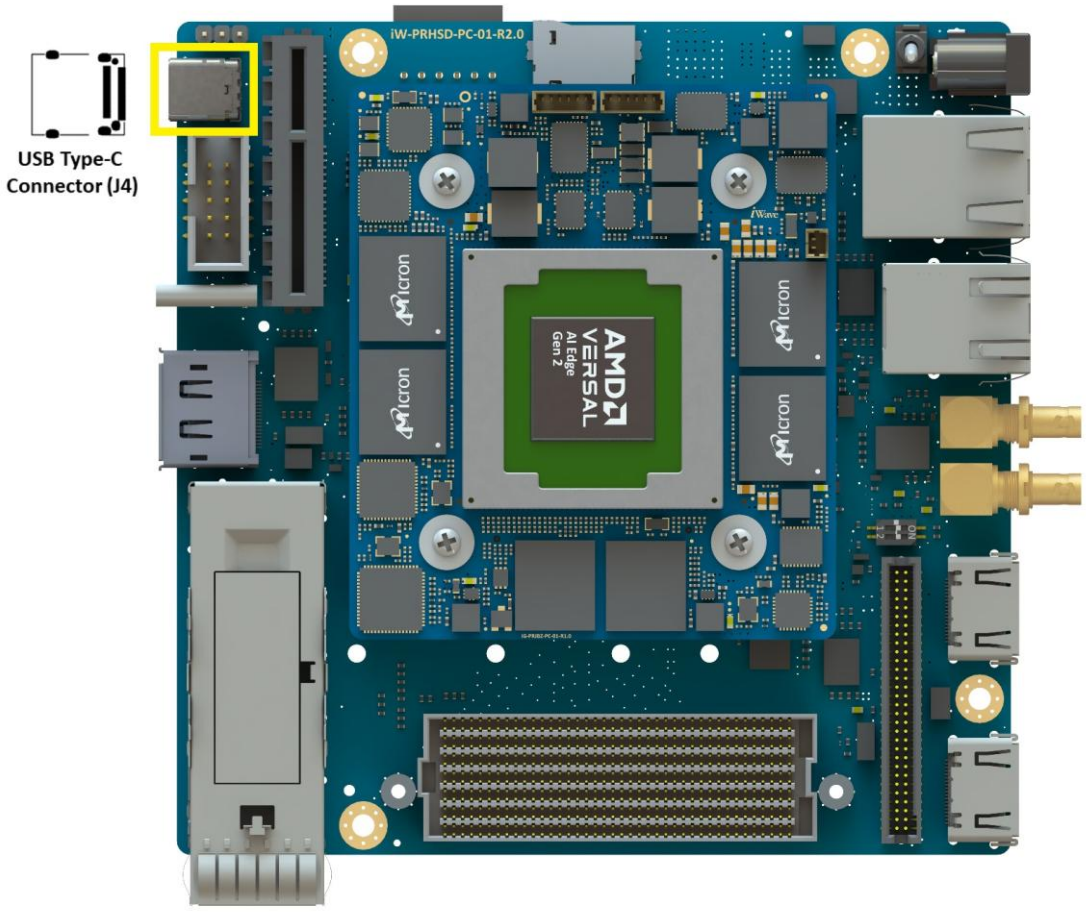


Figure 20:USB OTG Connector

2.8.4 Gigabit Ethernet Port1

The Versal AI Edge Gen2 SOM development board supports Ethernet port through GEM0 interface of Versal AI Edge Gen2 PS. Ethernet PHY output signals from Board-to-Board connector2 is directly connected to RJ45 MagJack (J5). The Ethernet supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 MagJack connector. This RJ45 MagJack connector (J5) is physically located at the top of the board as shown below.

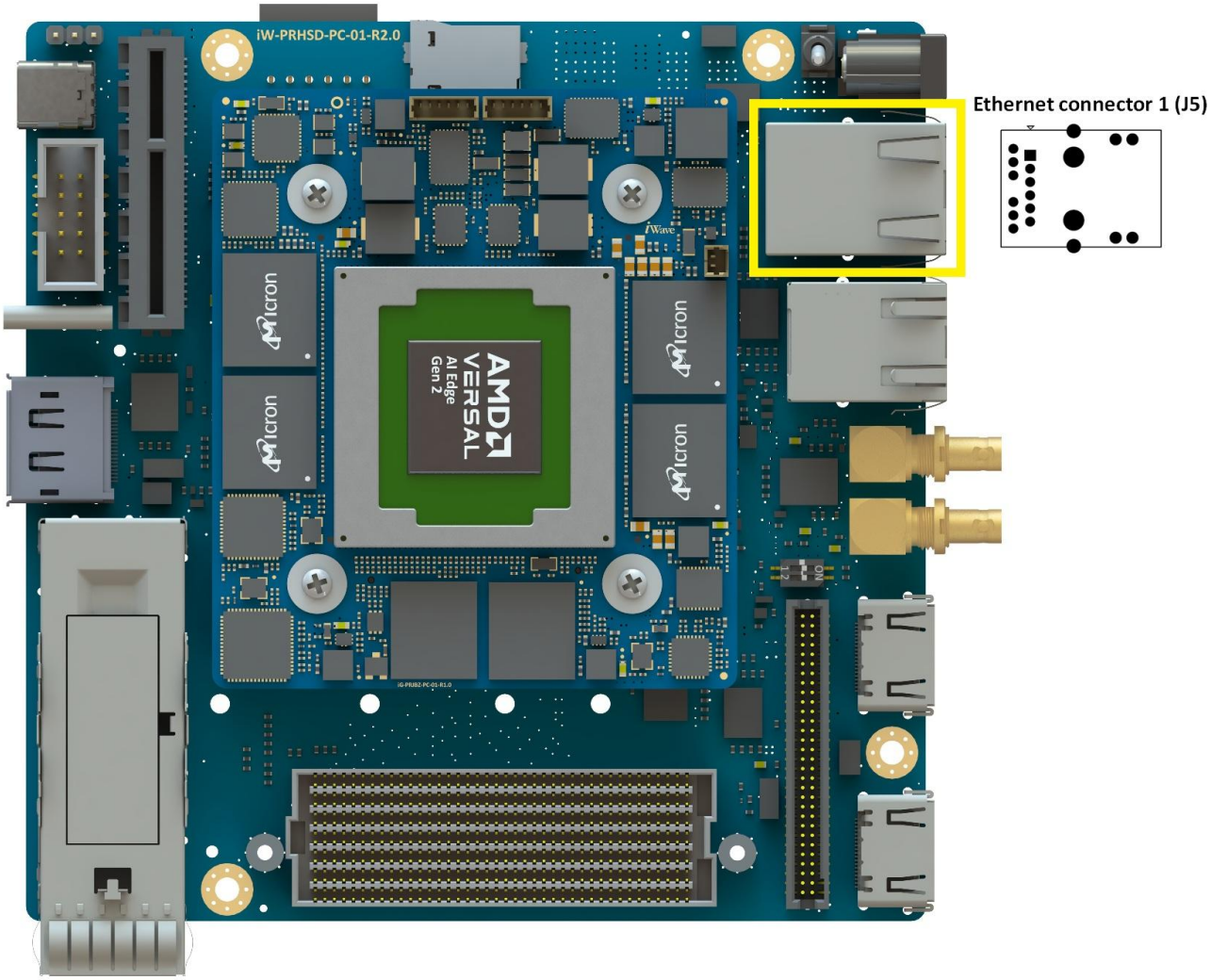


Figure 21:Gigabit Ethernet Connector1

2.8.5 Gigabit Ethernet Port2

The Versal AI Edge Gen2 SOM development board support Ethernet port through GEM1 interface of Versal AI Edge Gen2 PS. The MAC is integrated in the Versal AI Edge Gen2 SOM PS and connected to the external Gigabit Ethernet PHY “AR8031-AL1B” on development Board through Board-to-Board Connector2. This PHY is interfaced with GEM1 interface of Versal’s PS through MIO pins and works at 1.8V IO voltage level.

The Gigabit Ethernet PHY also supports MDC, MDIO, Reset and Interrupt Signals for control. These MDC, MDIO and Interrupt signals are used through PS Bank MIO pins from Board-to-Board Connector2 pins C12, C13 & C14 respectively and reset from MIO Bank from Board-to-Board Connector2 pin B10. Ethernet PHY output is directly connected to RJ45 MagJack (J9). Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 MagJack connector. This RJ45 MagJack connector is physically located at the top of the board as shown below.

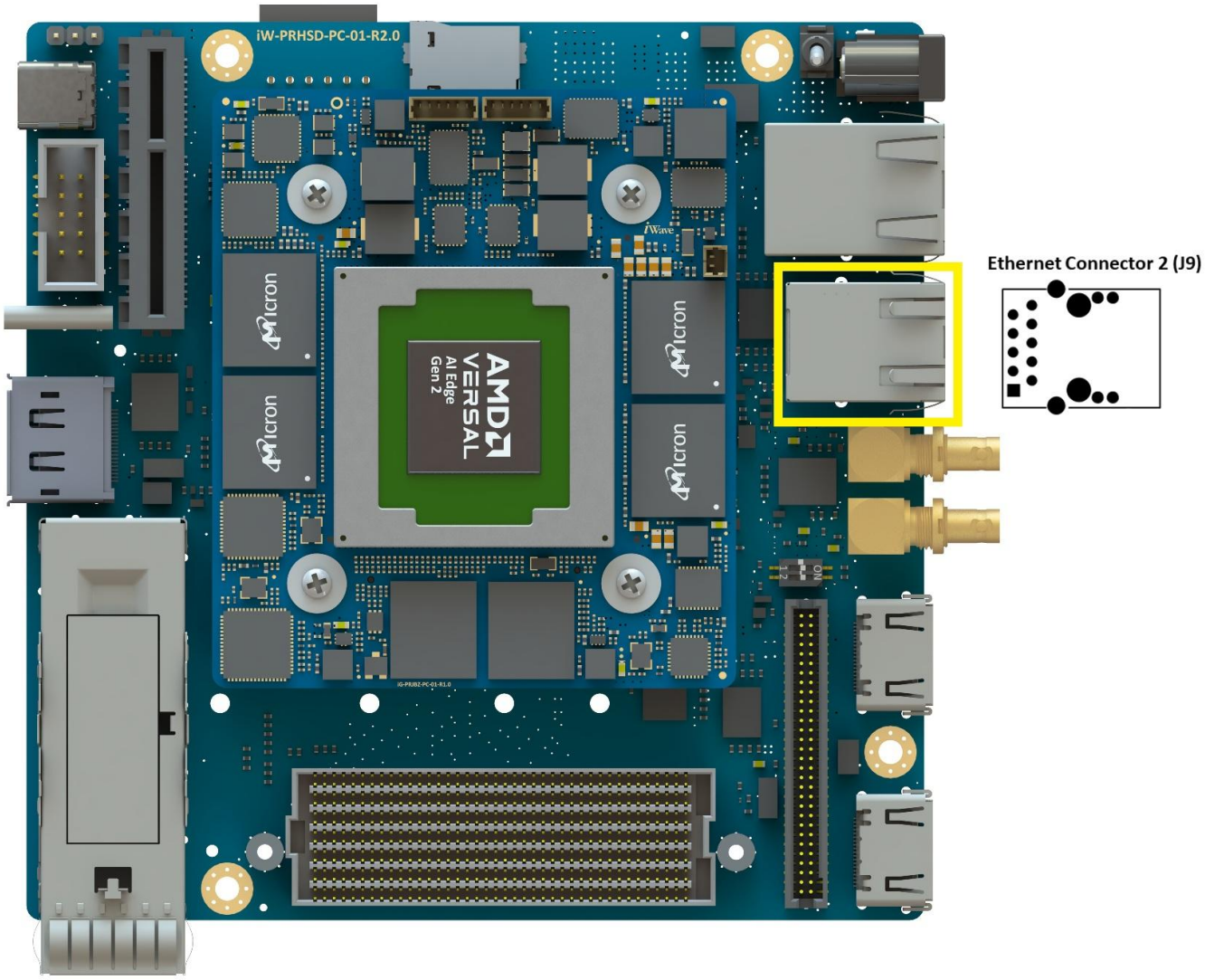


Figure 22:Gigabit Ethernet Connector2

2.8.6 USB Type-C for Debug UART and JTAG

The Versal AI Edge Gen2 development board supports a JTAG/UART to USB Module Host through USB Type-C Connector “KUSBX-SL-CS1N14-B”. This interface supports JTAG and Debug UART interface with a single Type-C connector from PS. To support JTAG from same Type-C connector make sure switch SW3 is in OFF state. The JTAG-SMT4 module is a compact, complete, and fully self-contained surface-mount programming module for Xilinx FPGAs. The module can be accessed directly from all Xilinx Tools, including Vivado, and Vitis.

The JTAG-SMT4 uses a 3.3V main power supply (VDD). Since JTAG-SMT4 requires 3.3V IO level, these signals from Board-to-Board connector2 are connector to JTAG-SMT4 module through Voltage level translator. The module routes the USB D+ (DP) and D- (DM) signals directly to the USB Type-C connector. The USB Type-C connector (J8) is located at the top side of the board as shown below.

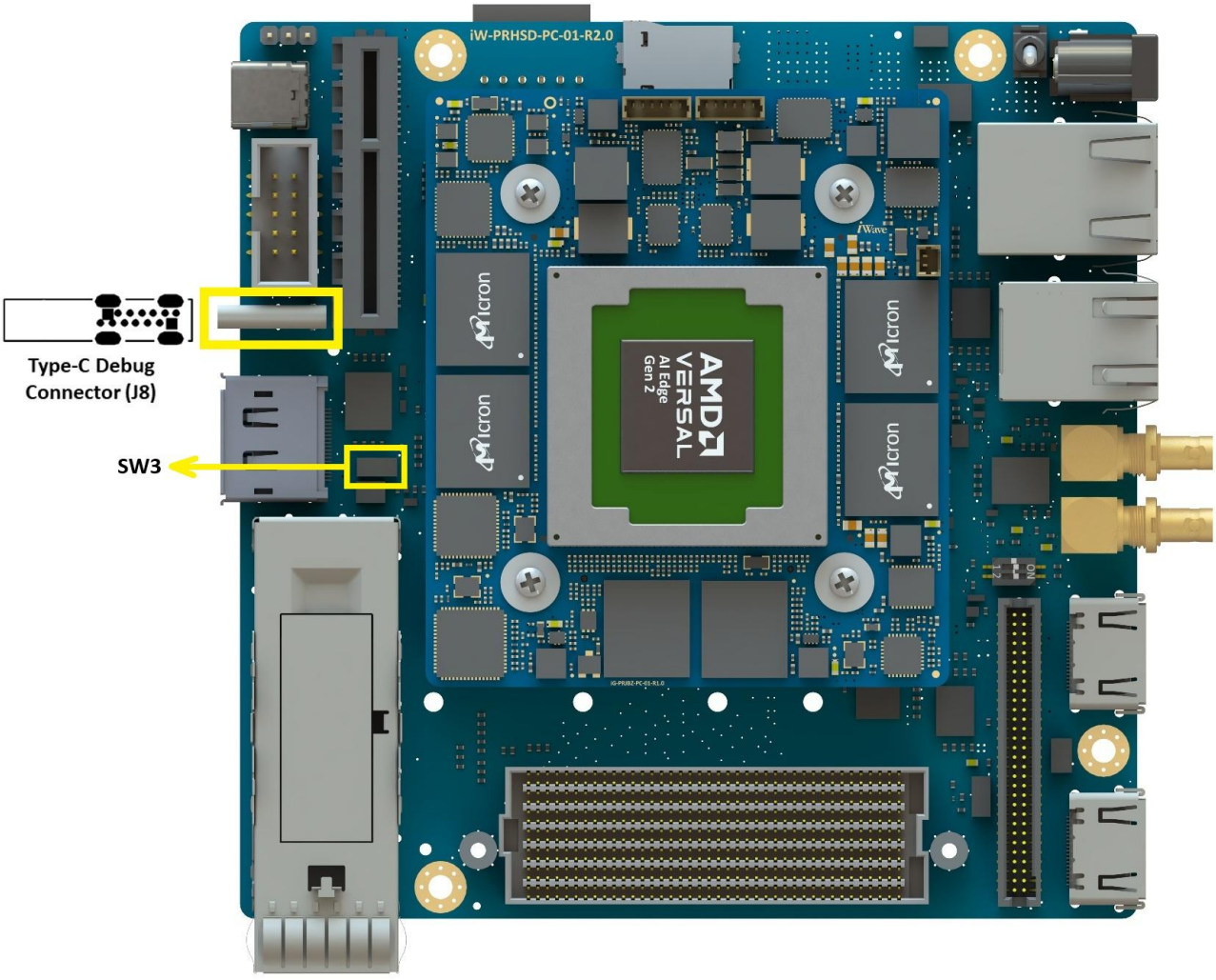


Figure 23:Debug Connector

2.8.7 Micro SD Port

The Versal AI Edge Gen2 Development Board supports one SD interface through SD interface of Versal AI Edge Gen2 PS. This SD signals from Board-to-Board connector2 are connected to Micro SD connector (J3) through auto-direction control memory card voltage level translator to support both 1.8V and 3.3V supported cards. It supports up to 4-Bit data transfer with card detect and write protect.

The memory card voltage level translator's voltage selection is controlled through SD1_PWR pin from Board-to-Board Connector2 pin B21. If SD1_PWR is set to low, then 3.3V IO level is selected for SD signals to SD connector. If SD1_PWR is set to high, then 1.8V IO level is selected for SD signals to SD connector. The Micro SD connector (J3) is physically located at the top of the board as shown below.

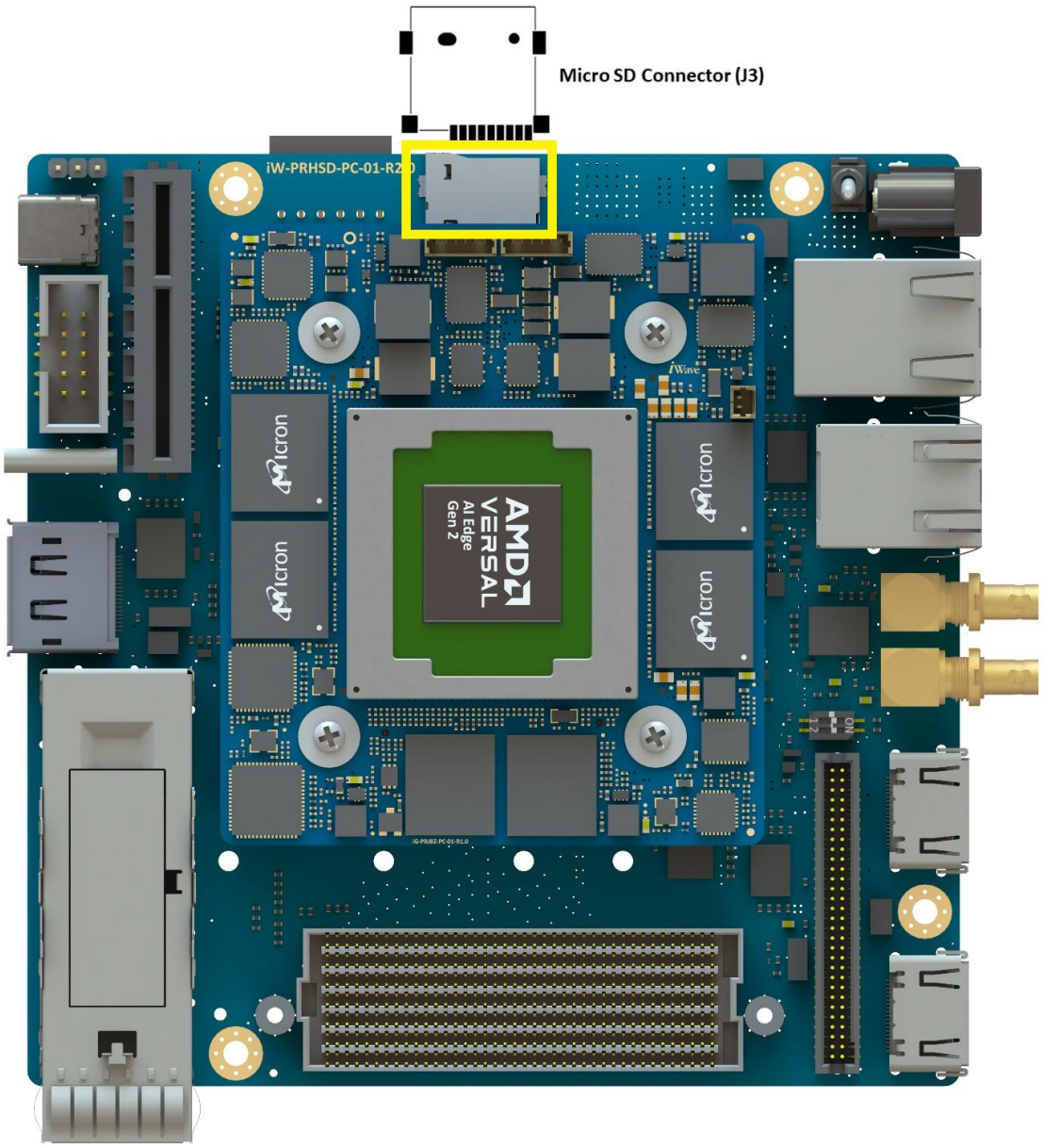


Figure 24:Micro SD Connector

2.9 Additional Features

2.9.1 Clock Synthesizers

The Versal AI Edge Gen2 development board supports two Clock Synthesizer “ZL30733LDG1” and “SI5332A-D-GM1” for on board clock distribution. This Clock Generator outputs are connected to GTYP clock on Board-to-Board Connectors through 0.01uF AC coupling capacitors. Also, the clock synthesizers are used for on-board interfaces clock distribution. An external 114.285MHz and 25MHz crystals are connected to this Clock Synthesizers for reference.

Table 12: Clock Synthesizer 1 Output Clocks

Pin No	Pin Name	Signal Name	SoC Pin Name	SoC Bank	SoC Pin No.	Programmed Frequency	Connected To
52	OUT0P	NC	NA	NA	NA	NA	NC
51	OUT0N	NC	NA	NA	NA		NC
55	OUT1P	10MHz_REFCLK_OUT	IO_L3P_GC_H0O0P6_M2P70_712	X5IO Bank 712	AV46	10MHz	No Connect. Optionally connected to B2B Connector 1 D25th Pin.
58	OUT2P	LS_PCIe_DEVCLK_P	NA	NA	NA	100MHz	PCIe x4 connector A13th Pin
57	OUT2N	LS_PCIe_DEVCLK_N	NA	NA	NA		PCIe x4 connector A14th Pin
61	OUT3P	LS_TXVR_REFCLK0_P	GTYP_MMI_REFCLKP0_105	PS-GTYP 105	L3	100MHz	B2B Connector1 D51st Pin
60	OUT3N	LS_TXVR_REFCLK0_N	GTYP_MMI_REFCLKN0_105	PS-GTYP 105	L2		B2B Connector1 D52nd Pin
64	OUT4P	SYS_SYNC_CLK_INP	NA	NA	NA	100MHz	B2B Connector1 A15th Pin
63	OUT4N	SYS_SYNC_CLK_INN	NA	NA	NA		B2B Connector1 A16th Pin
17	OUT5P	CLK_SYNTH2_IN_CLK_IN_P	NA	NA	NA	100MHz	Input Clock for clock synthesizer 2
18	OUT5N	CLK_SYNTH2_IN_CLK_IN_N	NA	NA	NA		
20	OUT6P	ETH2_XI_CLK25MHz	NA	NA	NA	25MHz	GEM1 Ethernet PHY Reference Clock
21	OUT6N	1PPS_REFCLK_OUT	IO_L19P_GC_H1O0P6_M1P166_705	X5IO Bank 712	BF12	1Hz	B2B Connector1 A47th Pin
23	OUT7P	NC	NA	NA	NA	NA	NC
24	OUT7N	NC	NA	NA	NA		NC
26	OUT8P	NC	NA	NA	NA	NA	NC
27	OUT8N	NC	NA	NA	NA		NC

Pin No	Pin Name	Signal Name	SoC Pin Name	SoC Bank	SoC Pin No.	Programmed Frequency	Connected To
29	OUT9P	HS_TXVR1_CLK0P	GTYP_REFCLKP0_106	PL-GTYP 106	G7	148.5 MHz	B2B Connector2 B41th Pin This clock is input to reference clock 0 of GTYP bank106
30	OUT9N	HS_TXVR1_CLK0N	GTYP_REFCLKN0_106	PL-GTYP 106	F7		B2B Connector2 B42th Pin. This clock is input to reference clock 0 of GTYP bank106

Table 13:Clock Synthesizer 2 Output Clocks

Pin No	Pin Name	Signal Name	SoC Pin Name	SoC Bank	SoC Pin No.	Programmed Frequency	Connected To
12	OUT0	NC	NA	NA	NA	NA	NC
11	OUT0b	NC	NA	NA	NA		NC
15	OUT1	HS_TXVR2_CLK0P	GTYP_REFCLKP0_107	PL-GTYP 107	G9	156.25 MHz	B2B Connector2 A51st Pin This clock is input to reference clock 0 of GTYP bank107
14	OUT1b	HS_TXVR2_CLK0N	GTYP_REFCLKN0_107	PL-GTYP 107	F9		B2B Connector2 A52nd Pin. This clock is input to reference clock 0 of GTYP bank107
19	OUT2	NC	NA	NA	NA	NA	NC
18	OUT2b	NC	NA	NA	NA		NC
22	OUT3	NC	NA	NA	NA	NA	NC
21	OUT3b	NC	NA	NA	NA		NC
27	OUT4	NC	NA	NA	NA	NA	NC
26	OUT4b	NC	NA	NA	NA		NC
31	OUT5	NC	NA	NA	NA	NA	NC
30	OUT5b	NC	NA	NA	NA		NC

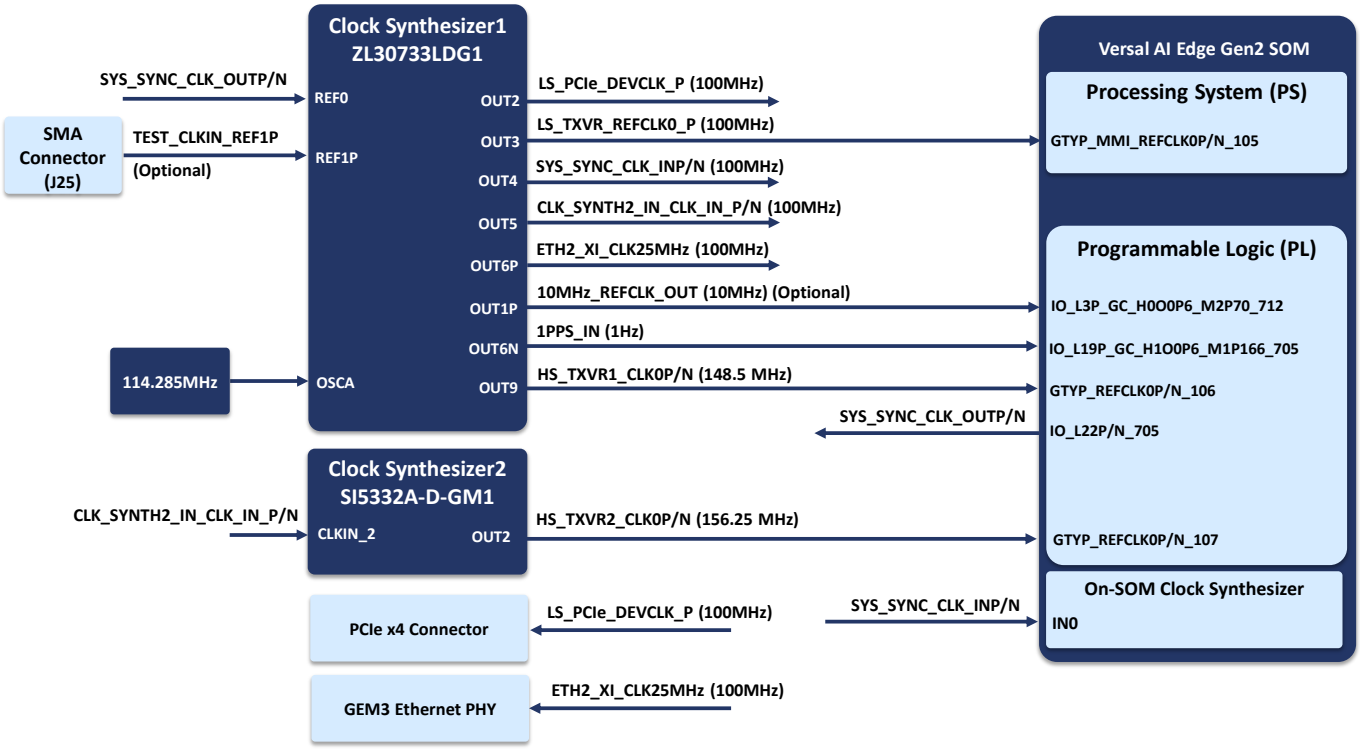


Figure 25: Clock Tree

2.9.2 IO Expanders

The Versal AI Edge Gen2 development board supports two GPIO 16-Bit port Expander. IO expanders are configured through I2C of development board I2C mux switch. IO expander 1 is connected to Channel0 of I2C MUX switch and IO expander 2 is connected to Channel1 of I2C MUX. Refer below table for IO Expander pin mapping.

Table 14: IO Expander 1 Output

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
IO EXPANDER 1 (TCA6416APWR) - I2C address: 0x20				
4	P00	IOEXP1_HDMITX_OE	O, 3.3V CMOS	Connected to HDMI OUT Re-timer IC
5	P01	IOEXP1_HDMITX_CEC	I, 3.3V CMOS	Connected to HDMI OUT Connector
6	P02	IOEXP1_HDMIRX_CEC	O, 3.3V CMOS	Connected to HDMI IN Connector
7	P03	IOEXP1_EEPROM_WCn	O, 3.3V CMOS/ 10K PU	Active Low Write enable for EEPROM
8	P04	IOEXP1_SDI_IN_CD_INT	I, 3.3V CMOS	Connected to SDI IN IC PLL lock status pin
9	P05	IOEXP1_SDI_CD_INT	I, 3.3V CMOS	Connected to SDI OUT PLL lock status pin
10	P06	IOEXP1_EXP2_INT	I, 3.3V CMOS/ 4.7K PU	IO Expander 2 Interrupt Output
11	P07	IOEXP1_USB3_C_INT	I, 3.3V CMOS/ 4.7K PU	USB3.0 Controller Interrupt
13	P10	IOEXP1_BRD_CONFIG0	I, 3.3V CMOS	No Connect.
14	P11	IOEXP1_BRD_CONFIG1	I, 3.3V CMOS	No Connect.
15	P12	IOEXP1_BRD_CONFIG2	I, 3.3V CMOS	No Connect.
16	P13	IOEXP1_BRD_CONFIG3	I, 3.3V CMOS	No Connect.
17	P14	IOEXP1_BRD_CONFIG4	I, 3.3V CMOS	No Connect.
18	P15	IOEXP1_BRD_CONFIG5	I, 3.3V CMOS	No Connect.
19	P16	IOEXP1_BRD_CONFIG6	I, 3.3V CMOS	No Connect.
20	P17	IOEXP1_DP_HPD	I, 3.3V CMOS	Connected to DP Connector Hotplug Detect

Table 15: IO Expander 2 Output

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
IO EXPANDER 2 (TCA6416APWR)- I2C address: 0x21				
4	P00	B_FMC+_CLK_DIR	I, 3.3V CMOS	FMC+ Clock DIR Pin
5	P01	B_FMC+_PG_M2C	I, 3.3V CMOS	Power Good Signal from FMC Module
6	P02	B_FMC+_PR_M2C_L	I, 3.3V CMOS/ 10K PU	FMC+ Module Present Signal.
7	P03	B_FMC+_HSPC_PRSNT_M2C_L	I, 3.3V CMOS/ 10K PU	FMC+ Module Present Signal.
8	P04	B_FMC+_PG_C2M	O, 3.3V CMOS/ 10K PD	Carrier board Power good signal to FMC+ Module
9	P05	B_FMC+_12V_EN	O, 3.3V CMOS/ 10K PD	FMC+ 12V Power enable
10	P06	B_FMC+_3V3_EN	O, 3.3V CMOS/ 10K PD	FMC+ 3.3V Power enable.
11	P07	B_FMC+_ADJ_EN	O, 3.3V CMOS/ 10K PD	Carrier board ADJ voltage enable.
13	P10	IOEXP2_Q_ModeSEL	O, 3.3V CMOS/ 4.7K PD	Connected to QSFP+ connector If MODESEL is low, then QSFP+ module respond to serial communication If MODESEL is High, then QSFP+ module will not respond to serial communication
14	P11	IOEXP2_Q_ResetL	O, 3.3V CMOS/ 4.7K PU	Connected to QSFP+ connector If Reset is Low, then QSFP+ module in reset state If Reset is High (3.3V), then QSFP+ module in out of reset state
15	P12	IOEXP2_Q_LPMode	O, 3.3V CMOS/ 4.7K PD	Connected to QSFP+ connector High for LpMode Low for TXDIS mode
16	P13	IOEXP2_Q_INTL	I, 3.3V CMOS/ 4.7K PU	Connected to QSFP+ connector Low - Operational fault High - Normal operation
17	P14	IOEXP2_Q_ModPrsl	I, 3.3V CMOS/ 4.7K PU	Connected to QSFP+ connector Low - When module is inserted High - When module is absent
18	P15	IOEXP1_USB3_SW_SEL	O, 3.3V CMOS/ 10K PU	USB3.0 Switch Select.
19	P16	IOEXP2_USB3_EN	O, 3.3V CMOS	USB3.0 Power Enable
20	P17	IO_EXP2_LS_PCIe_WAKE	O, 3.3V CMOS/ 10K PU	PCIe Wake for PCIe x4 Connector.

2.9.3 I2C Tree

The Versal AI Edge Gen2 development board supports two I2C interfaces from board-to-board connector2. These I2C is supported from Versal AI Edge Gen2 processor. To avoid the slave address conflicts the development board support I2C mux switch (PI4MSD5V9546ALEX) for I2C0 port of connector. I2C tree shown below represents the complete I2C connections of development kits

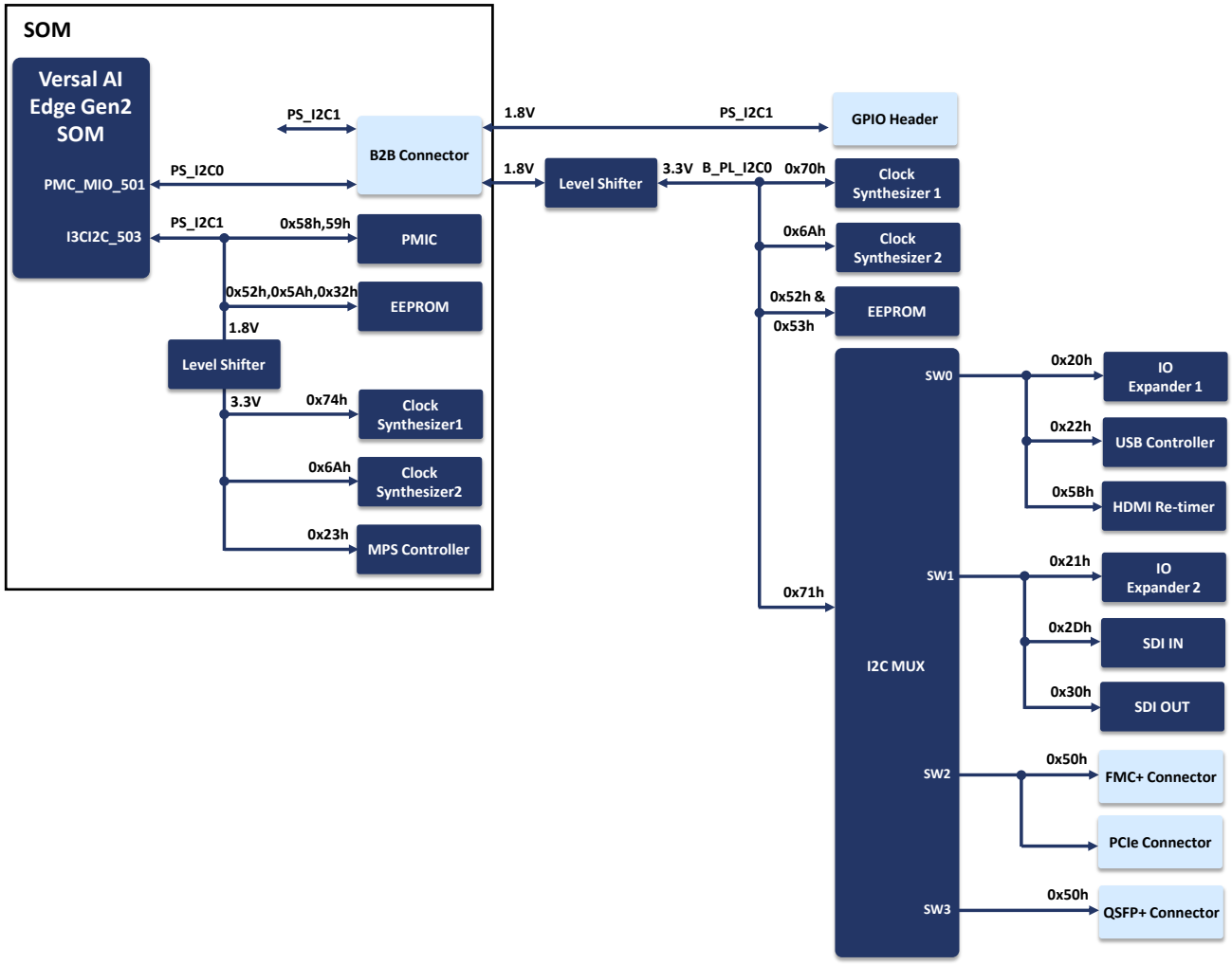


Figure 26: I2C Tree

2.9.4 DIP Switch

The Versal AI Edge Gen2 development board supports one DIP Switch for validating the two GPIOs from X5IO Bank 713. The GPIO DIP Switch is located at the top of carrier board as shown below.

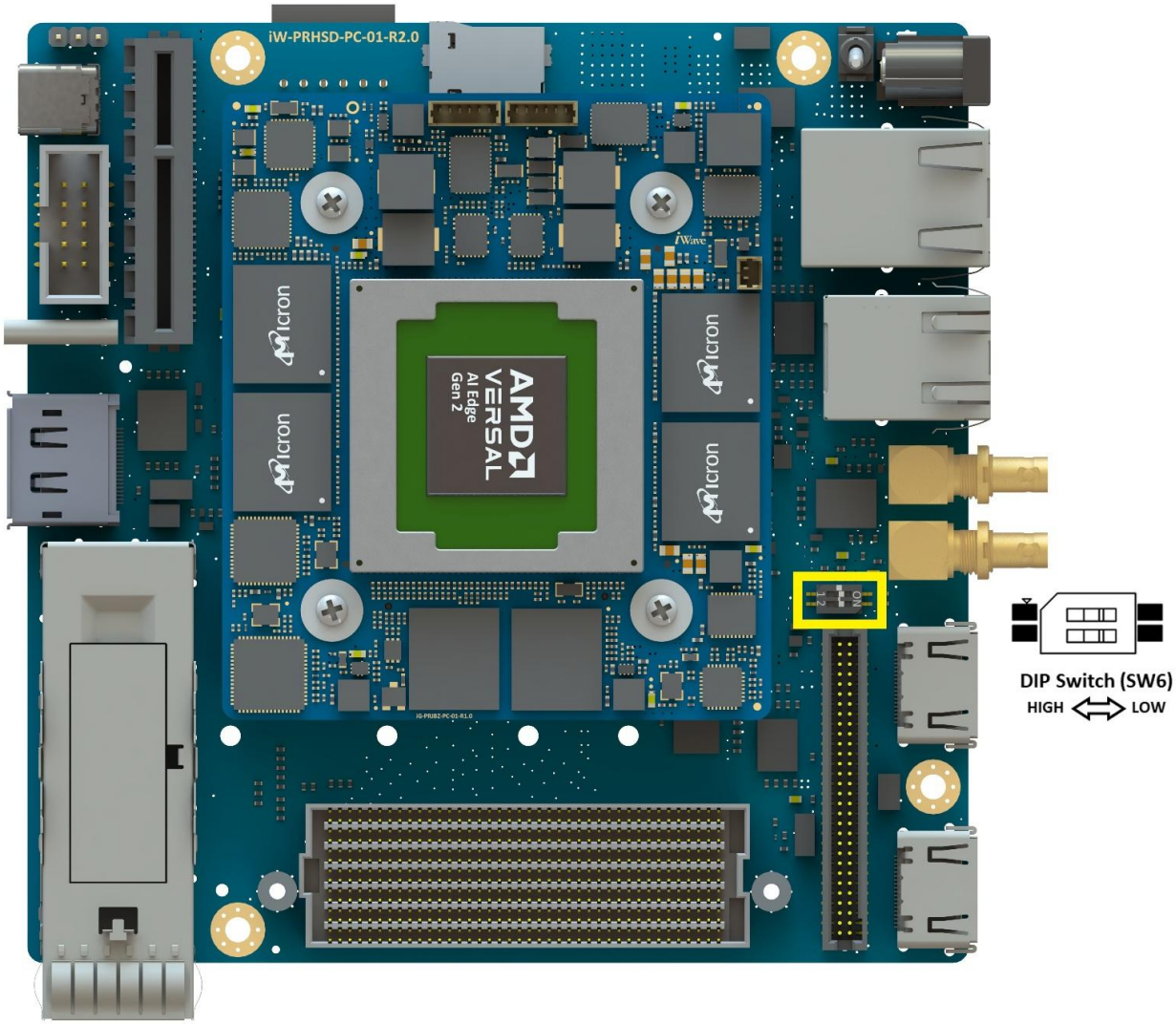


Figure 27: DIP Switch

Table 16: DIP Switch Pin Assignment

Pin No	Signal Name	SoC Pin Name	SoC Bank	SoC Pin No.	Signal Type/ Termination	Description
SW6.1	BANK2_IO5P	IO_L29P_XCC_H1O3P2_M3P122_713	X5IO Bank 713	AL45	I, 1.2V	PL X5IO Bank 713 IO29 Positive. SW6.1 ON – Logic LOW SW6.1 OFF – Logic High
SW6.2	BANK2_IO5N	IO_L29N_XCC_H1O3P3_M3P123_713	X5IO Bank 713	AL46	I, 1.2V	PL X5IO Bank 713 IO29 Negative. SW6.2 ON – Logic Low SW6.2 OFF – Logic High

2.9.5 User LEDs

The Versal AI Edge Gen2 development board supports two User LEDs from X5IO Bank 713. This User LEDs are configurable by the end user. The User LEDs are located at the top of carrier board as shown below.

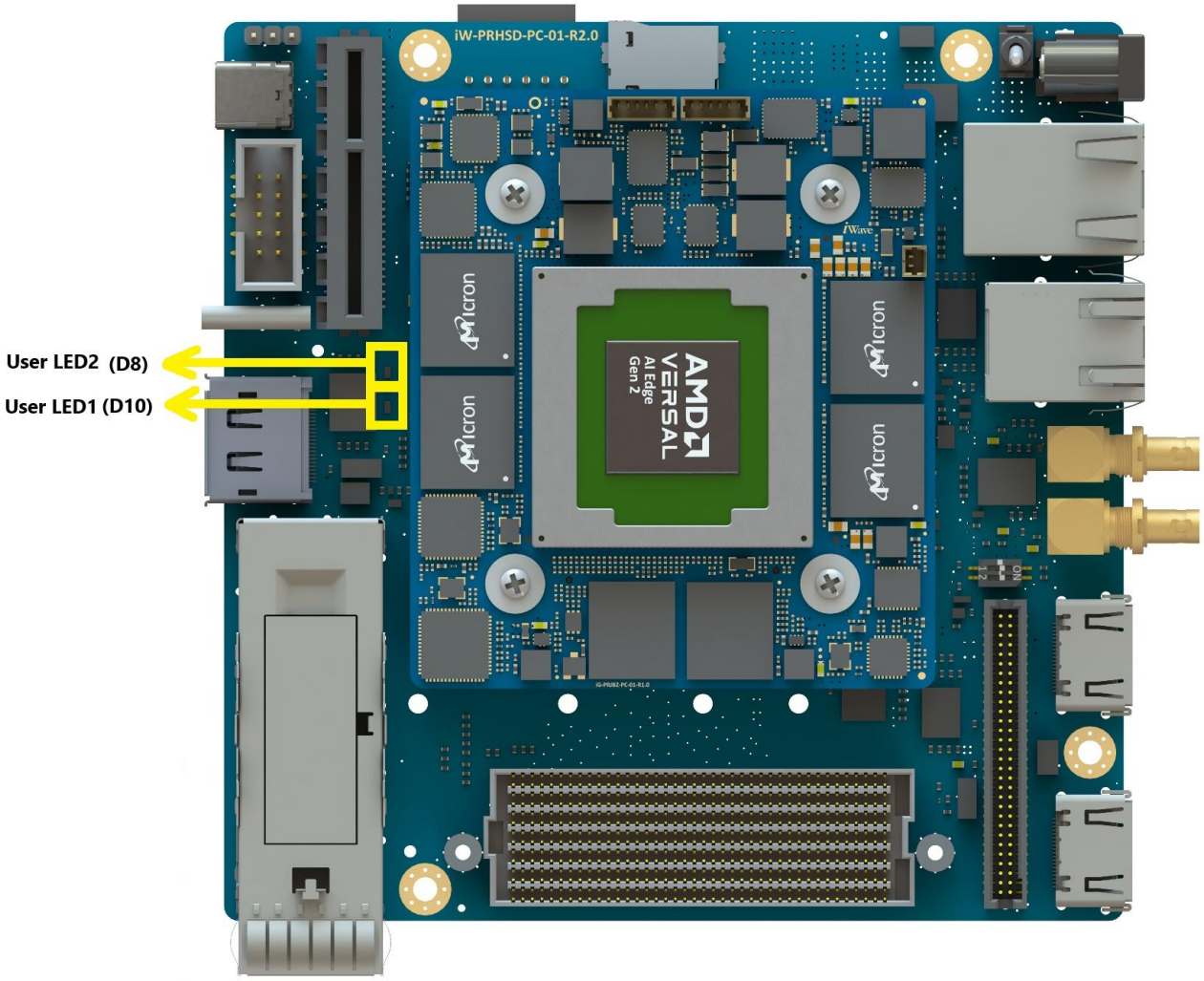


Figure 28: User LED

Table 17: User LEDs Pin Assignment

Pin No	Signal Name	SoC Pin Name	SoC Bank	SoC Pin No.	Signal Type/ Termination	Description
LED1	BANK2_IO4P	IO_L27P_H1O2P6 _M3P118_713	X5IO Bank 713	AP44	O, 1.2V	Connected to User LED 1 – D10, By default high
LED2	BANK2_IO4N	IO_L27N_H1O2P7 _M3P119_713	X5IO Bank 713	AP45	O, 1.2V	Connected to User LED 2 – D8, By default high.

2.9.6 EEPROM

The Versal AI Edge Gen2 development board supports 4Kb EEPROM for storing Carrier Board configuration. The I2C module of Versal AI Edge Gen2 PS is used for EEPROM interface through MIO pins with I2C address 0x52, 0x53. This device operates at 3.3V voltage level. The write enable pin of EEPROM is connected to the P03 pin of IO Expander 1 (U18).

2.9.7 GPIO Header

The Versal AI Edge Gen2 development board supports one GPIO Header (J19) for General Purpose. These Header signals are directly connected from Board-to-Board connector 2. These header supports I2C, SPI, CAN, PS GPIOs and PL IOs. These GPIO Header (J19) is physically located at the top of the board as shown below.

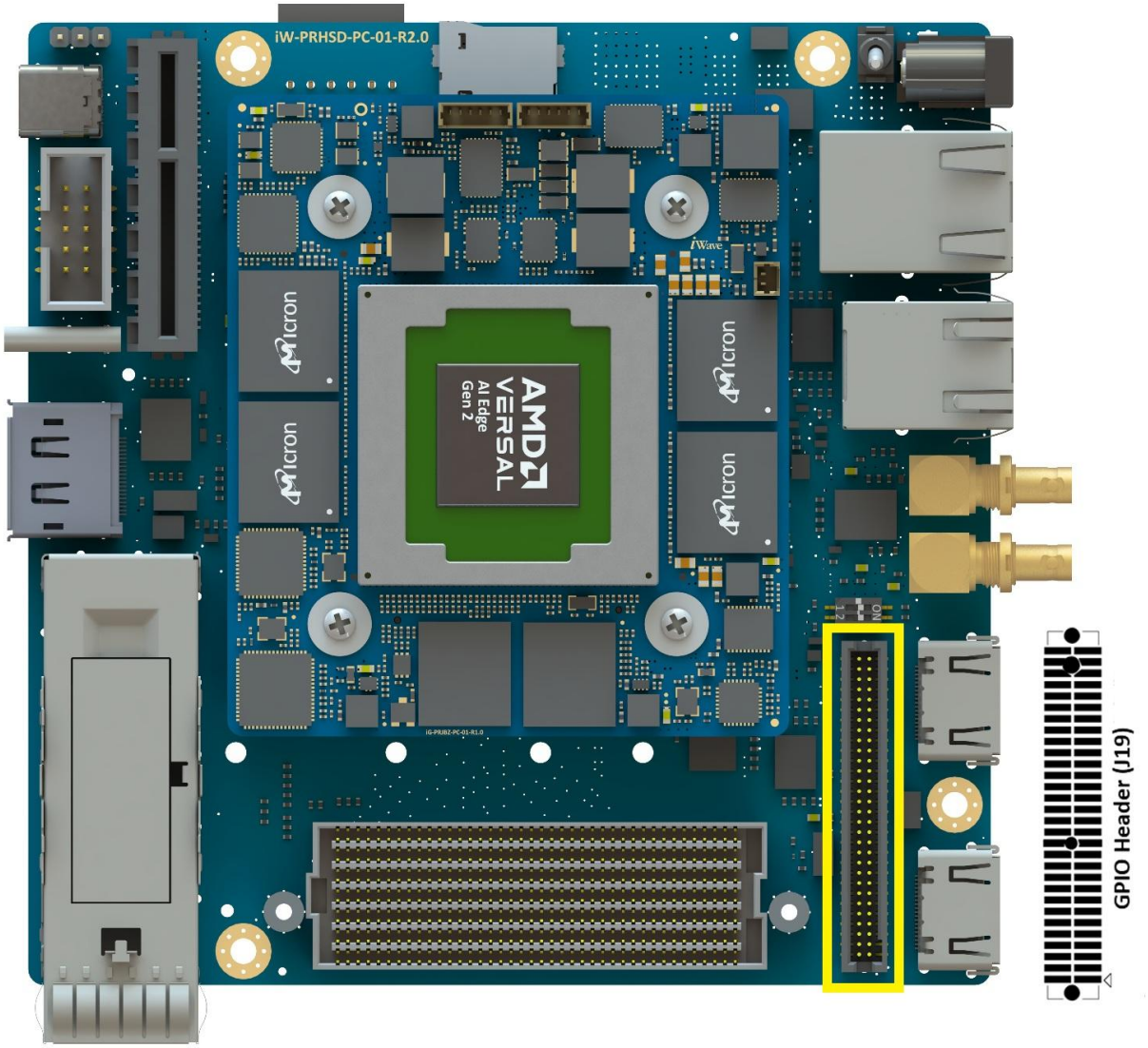


Figure 29:GPIO Header

Table 18:GPIO Header Pin Assignment

Pin No	Signal Name	Soc Pin Name	Soc Pin No.	Signal Type/ Termination	Description
1	VCC_5V	NA	NA	O, 5V Power	5V Supply Voltage.
2	VCC_5V	NA	NA	O, 5V Power	5V Supply Voltage.
3	BANK2_IO13P/GCIN1P	IO_L6P_H0O1P4_706	BA19	IO, 1.2V	PL Bank706 IO6 differential positive.
4	BANK2_IO16P	IO_L7P_H0O1P6_706	BB18	IO, 1.2V	PL Bank706 IO7 differential positive.
5	BANK2_IO13N/GCIN1N	IO_L6N_H0O1P5_706	BB19	IO, 1.2V	PL Bank706 IO6 differential negative.
6	BANK2_IO16N	IO_L7N_H0O1P7_706	BC18	IO, 1.2V	PL Bank706 IO7 differential negative.
7	BANK2_IO14P/GCIN3P	IO_L4P_H0O1P0_706	BC17	IO, 1.2V	PL Bank706 IO4 differential positive.
8	BANK2_IO17P	IO_L5P_XCC_H0O1P2_706	BE16	IO, 1.2V	PL Bank706 IO5 differential positive.
9	BANK2_IO14N/GCIN3N	IO_L4N_H0O1P1_706	BD17	IO, 1.2V	PL Bank706 IO4 differential negative.
10	BANK2_IO17N	IO_L5N_XCC_H0O1P3_706	BF17	IO, 1.2V	PL Bank706 IO5 differential negative.
11	NC	NA	NA	NA	NC
12	BANK2_IO18P	IO_L8P_H0O2P0_706	BB15	IO, 1.2V	PL Bank706 IO8 differential positive.
13	NC	NA	NA	NA	NC
14	BANK2_IO18N	IO_L8N_H0O2P1_706	BB16	IO, 1.2V	PL Bank706 IO8 differential negative.
15	GND	GND	NA	Power	Ground
16	GND	GND	NA	Power	Ground
17	BANK2_IO19P	IO_L9P_XCC_H0O2P2_706	AY15	IO, 1.2V	PL Bank706 IO9 differential positive.
18	BANK2_IO22P	IO_L12P_H0O3P0_706	AW15	IO, 1.2V	PL Bank706 IO12 differential positive.
19	BANK2_IO19N	IO_L9N_XCC_H0O2P3_706	BA16	IO, 1.2V	PL Bank706 IO9 differential negative.
20	BANK2_IO22N	IO_L12N_H0O3P1_706	AW16	IO, 1.2V	PL Bank706 IO12 differential negative.
21	BANK2_IO20P	IO_L11P_H0O2P6_706	AW18	IO, 1.2V	PL Bank706 IO11 differential positive.
22	BANK2_IO23P	IO_L13P_XCC_H0O3P2_706	AT19	IO, 1.2V	PL Bank706 IO13 differential positive.
23	BANK2_IO20N	IO_L11N_H0O2P7_706	AY18	IO, 1.2V	PL Bank706 IO11 differential negative.
24	BANK2_IO23N	IO_L13N_XCC_H0O3P3_706	AU18	IO, 1.2V	PL Bank706 IO13 differential negative.

Pin No	Signal Name	Soc Pin Name	Soc Pin No.	Signal Type/ Termination	Description
25	BANK2_IO21P	IO_L10P_H0O2P4_706	AY17	IO, 1.2V	PL Bank706 IO10 differential positive.
26	BANK2_IO24P	IO_L14P_H0O3P4_706	AT16	IO, 1.2V	PL Bank706 IO14 differential positive.
27	BANK2_IO21N	IO_L10N_H0O2P5_706	BA17	IO, 1.2V	PL Bank706 IO10 differential negative.
28	BANK2_IO24N	O_L14N_H0O3P5_706	AU17	IO, 1.2V	PL Bank706 IO14 differential negative.
29	GND	NA	NA	Power	Ground
30	VCC_1V8	NA	NA	O, 1.8V Power	1.8V Supply Voltage.
31	NC	NA	NA	NA	NC
32	BANK2_IO9P	IO_L0P_H0O0P0_706	BE18	IO, 1.2V	PL Bank706 IO0 differential positive.
33	NC	NA	NA	NA	NC
34	BANK2_IO9N	IO_L0N_H0O0P1_706	BF18	IO, 1.2V	PL Bank706 IO0 differential negative.
35	NC	NA	NA	NA	NC
36	BANK2_IO10P	IO_L1P_XCC_H0O0P2_706	BF15	IO, 1.2V	PL Bank706 IO1 differential positive.
37	NC	NA	NA	NA	NC
38	BANK2_IO10N	IO_L1N_XCC_H0O0P3_706	BF16	IO, 1.2V	PL Bank706 IO1 differential negative.
39	BANK2_IO27P	IO_L15P_H0O3P6_706	AT15	IO, 1.2V	PL Bank706 IO15 differential positive.
40	VIO_BANK2	NA	NA	O, Power	Bank2 Supply Voltage.
41	BANK2_IO27N	IO_L15N_H0O3P7_706	AU15		PL Bank706 IO15 differential negative.
42	I2C1_SCL	I3CI2C_SCL_503	H16	O, 1.8V LVCMOS	I2C1 Clock. This Pin is connected to C10th pin of Board-to-Board Connector2.
43	CAN1_RX/UART2_RX	IO_L16P_H1O0P0_M1P160_705	BD13	I, 1.8V LVCMOS	CAN Receive Data. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D29th pin of Board-to-Board Connector2.
44	I2C1_SDA	I3CI2C_SDA_503	J16	IO, 1.8V LVCMOS	I2C1 Data. This Pin is connected to C11th pin of Board-to-Board Connector2.
45	CAN1_TX/UART2_TX	IO_L16N_H1O0P1_M1P161_705	BC12	O, 1.8V LVCMOS	CAN Transmit Data. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D30th pin of Board-to-Board Connector2.

Pin No	Signal Name	Soc Pin Name	Soc Pin No.	Signal Type/ Termination	Description
46	CAN0_TX/UART3_TX	PMC_MIO39_501	G22	O, 1.8V LVCMOS	CAN2 Transmit Data. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D28th pin of Board-to-Board Connector2.
47	UART1_RTS/Bank 3_IO26N	IO_L20P_H1O1P0_M1P168_705	BF14	O, 1.8V LVCMOS	UART Request to send. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D26th pin of Board-to-Board Connector2.
48	CAN0_RX/UART3_RX	PMC_MIO38_501	G23	I, 1.8V LVCMOS	CAN2 Receive Data. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D27th pin of Board-to-Board Connector2.
49	UART1_CTS/Bank3_IO26P	IO_L20N_H1O1P1_M1P169_705	BF13	I, 1.8V LVCMOS	UART Clear to send. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D25th pin of Board-to-Board Connector2.
50	UART1_TX/Bank3_IO25P	IO_L23N_H1O1P7_M1P175_705	BF9	O, 1.8V LVCMOS	UART Transmit Data. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D23rd pin of Board-to-Board Connector2.
51	SPI_SS1_IO3/Bank 3_IO24P	PMC_MIO33_501	F25	O, 1.8V LVCMOS	SPI1 Chip select 1. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D20th pin of Board-to-Board Connector2.
52	UART1_RX/Bank3_IO25N	IO_L23P_H1O1P6_M1P174_705	BF10	I, 1.8V LVCMOS	UART Receive Data. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D24th pin of Board-to-Board Connector2.
53	SPI_SCLK/Bank3_IO22P	PMC_MIO32_501	G25	O, 1.8V LVCMOS	SPI1 Clock. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D16th pin of Board-to-Board Connector2.
54	SPI_SS2_IO2/Bank 3_IO23N	PMC_MIO34_501	G24	O, 1.8V LVCMOS	SPI1 Chip select 2. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D19th pin of Board-to-Board Connector2.

Pin No	Signal Name	Soc Pin Name	Soc Pin No.	Signal Type/ Termination	Description
55	SPI_SS0/Bank3_IO24N	PMC_MIO35_501	H24	O, 1.8V LVCMOS	SPI1 Chip select 0. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D21st pin of Board-to-Board Connector2.
56	GND	NA	NA	Power	Ground
57	SPI_MOSI_IO0/Bank3_IO22N	PMC_MIO37_501	J23	O, 1.8V LVCMOS	SPI1 Master Out Slave Input. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D17th pin of Board-to-Board Connector2.
58	NC	NA	NA	NA	NC
59	SPI_MISO_IO1/Bank3_IO23P	PMC_MIO36_501	J24	I, 1.8V LVCMOS	SPI1 Master In Slave Out. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to D18th pin of Board-to-Board Connector2.
60	NC	NA	NA	NA	NC

2.9.8 Power ON/OFF Switch

The Versal AI Edge Gen2 development board has power ON/OFF switch (SW1) to control the Main power Input ON/OFF functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

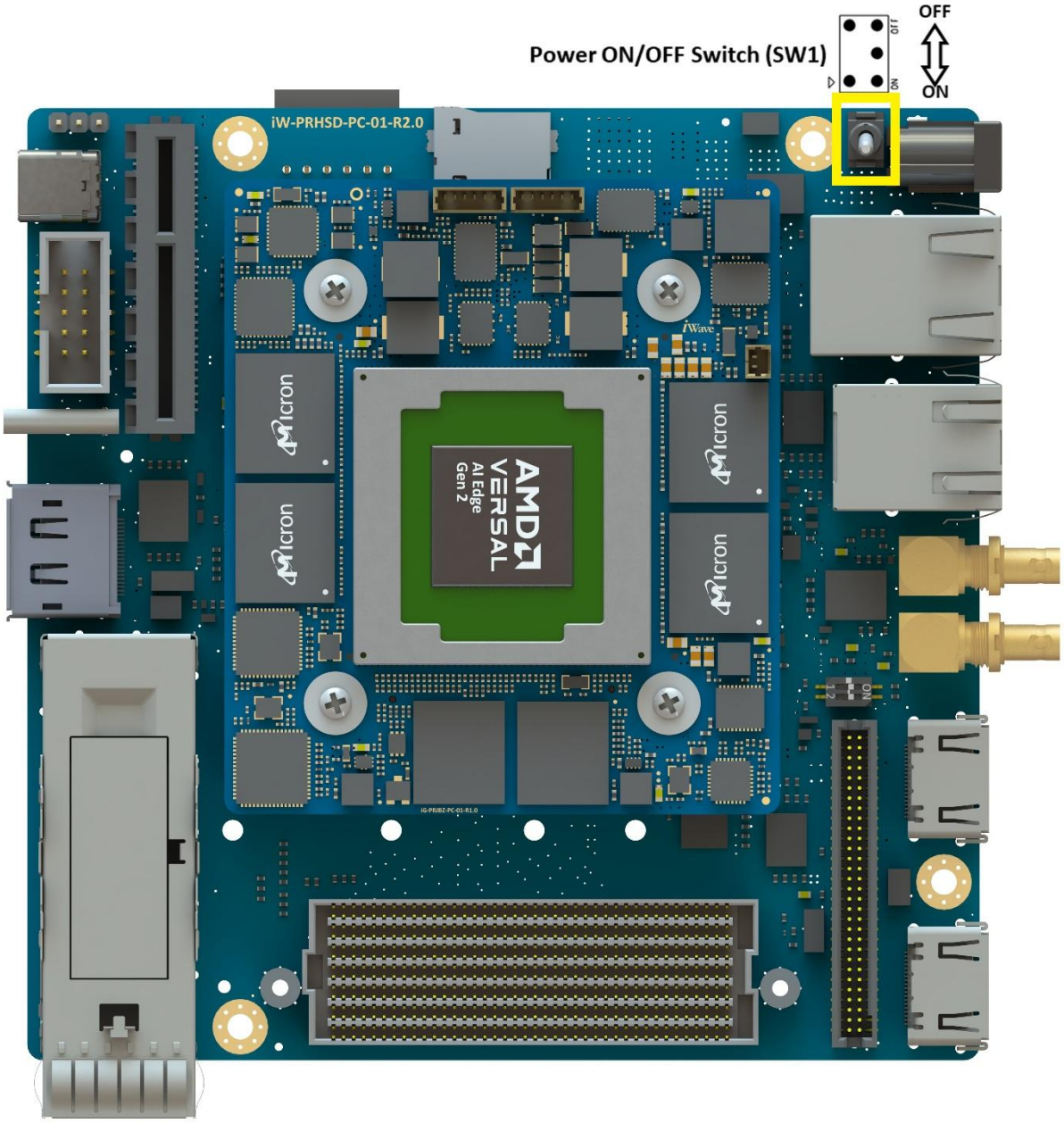


Figure 30: Power On/Off Switch

2.9.9 Reset Switch

The Versal AI Edge Gen2 development board supports Push button switch (SW5) to reset the Versal AI Edge Gen2 FPGA. Reset signal of Board-to-Board connector2 Pin B11 is directly connected from Reset Push button switch. This Reset Push button switch (SW5) is physically located at the top of the board as shown below.

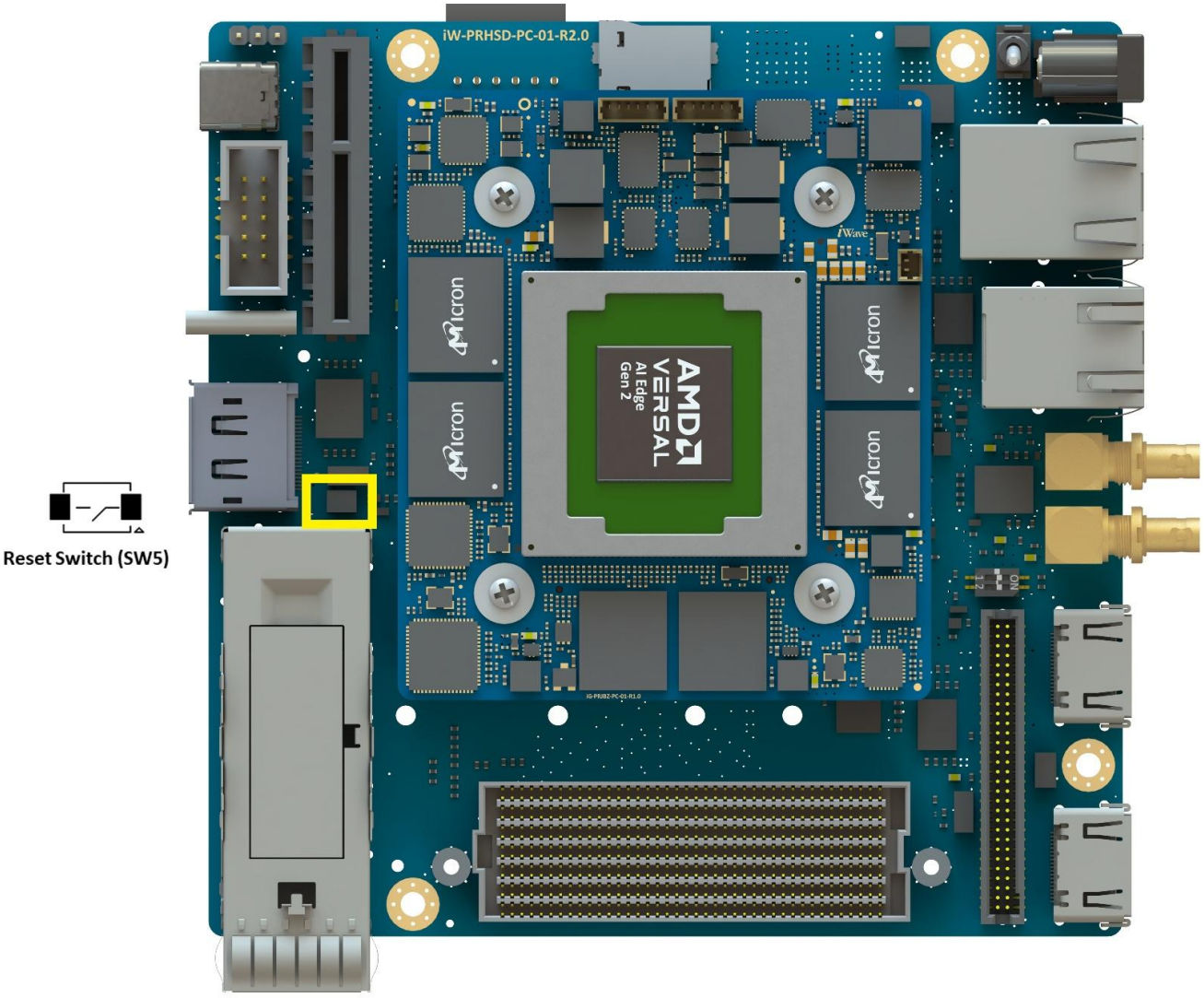


Figure 31: Reset Switch

2.9.10 RTC Coin Cell Holder

The Versal AI Edge Gen2 development board supports Coin Cell Holder to connect “2032” series 3V coin cell. This coin cell voltage is connected to Versal AI Edge Gen2 SOM for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J23) is physically located at the bottom of the board as shown below.

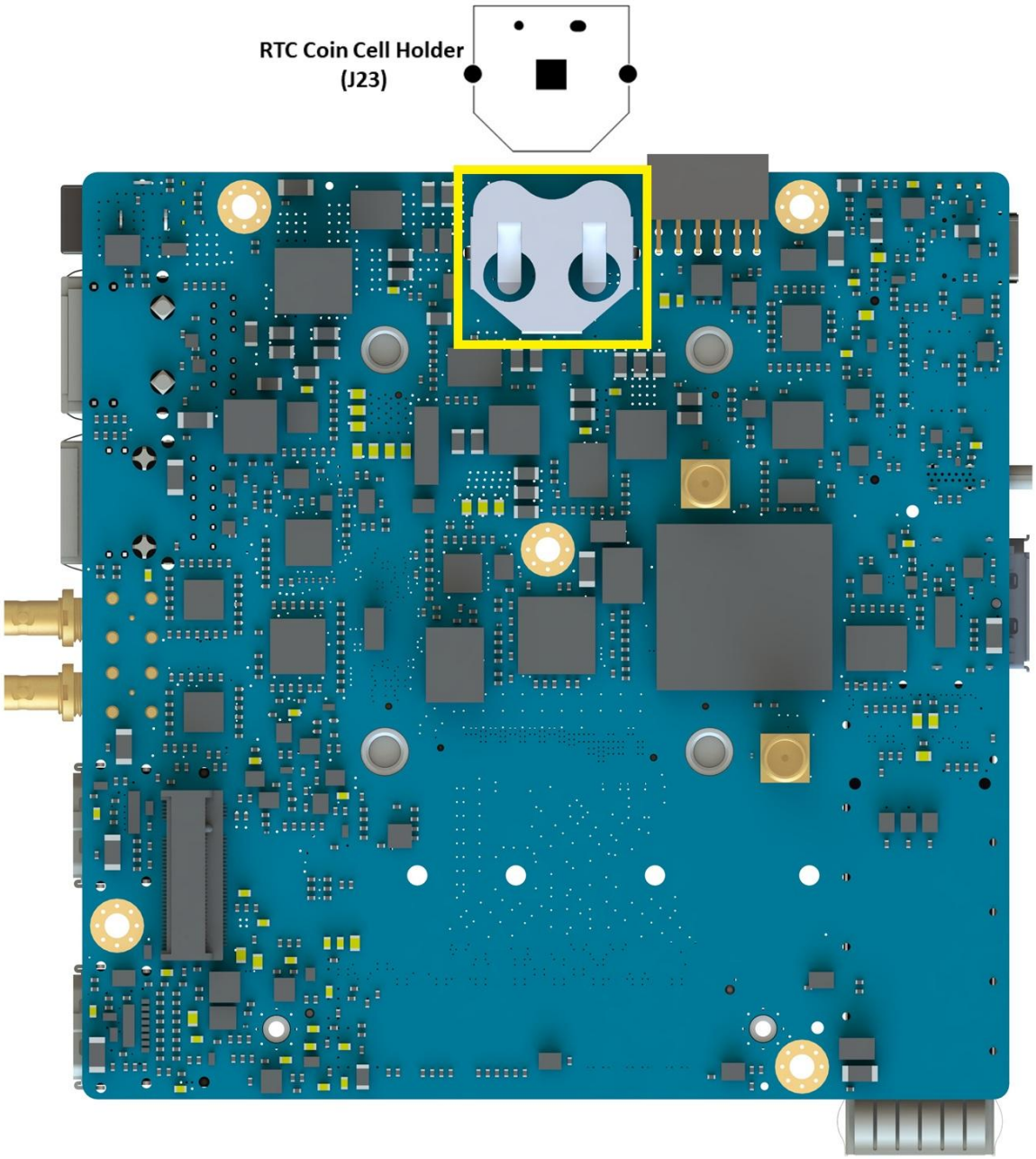


Figure 32: RTC Coin Cell Holder

2.9.11 Power and Program Done LED

The Versal AI Edge Gen2 development board supports Power LED and Config Done LED to indicate all powers and programs are successfully completed. The Red LED(D16) indicates all the powers are stable in the development board and Green LED(D5) to indicate programs are successfully flashed to FPGA. These LEDs are physically located at the top of the board as shown below.

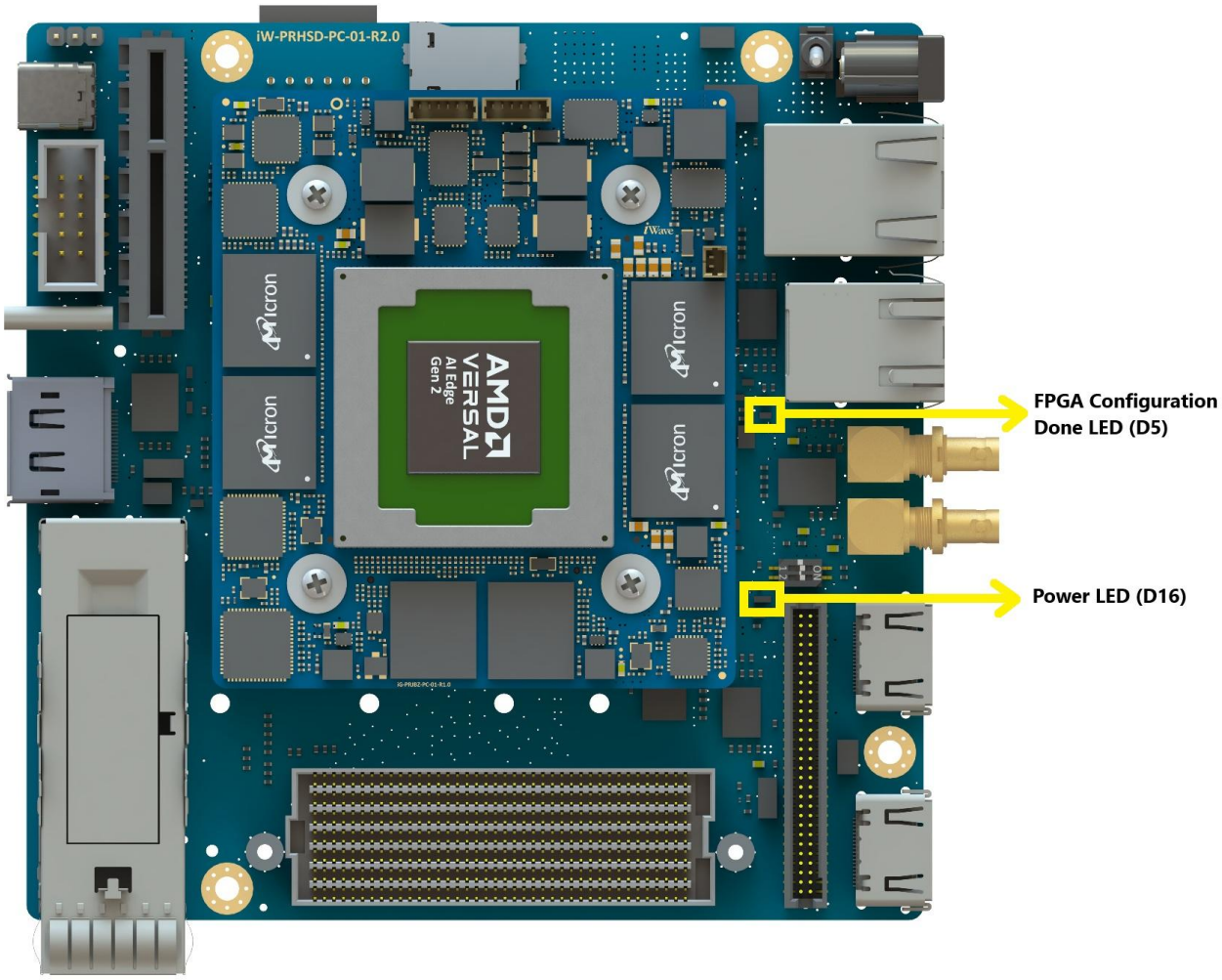


Figure 33: Power and Program Done LED

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Versal AI Edge Gen2 Development Board technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The Versal AI Edge Gen2 Development Board is designed to work with 12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the Versal AI Edge Gen2 Development Board through Power Jack (J2). This connector is physically placed at the top of the board as shown below.

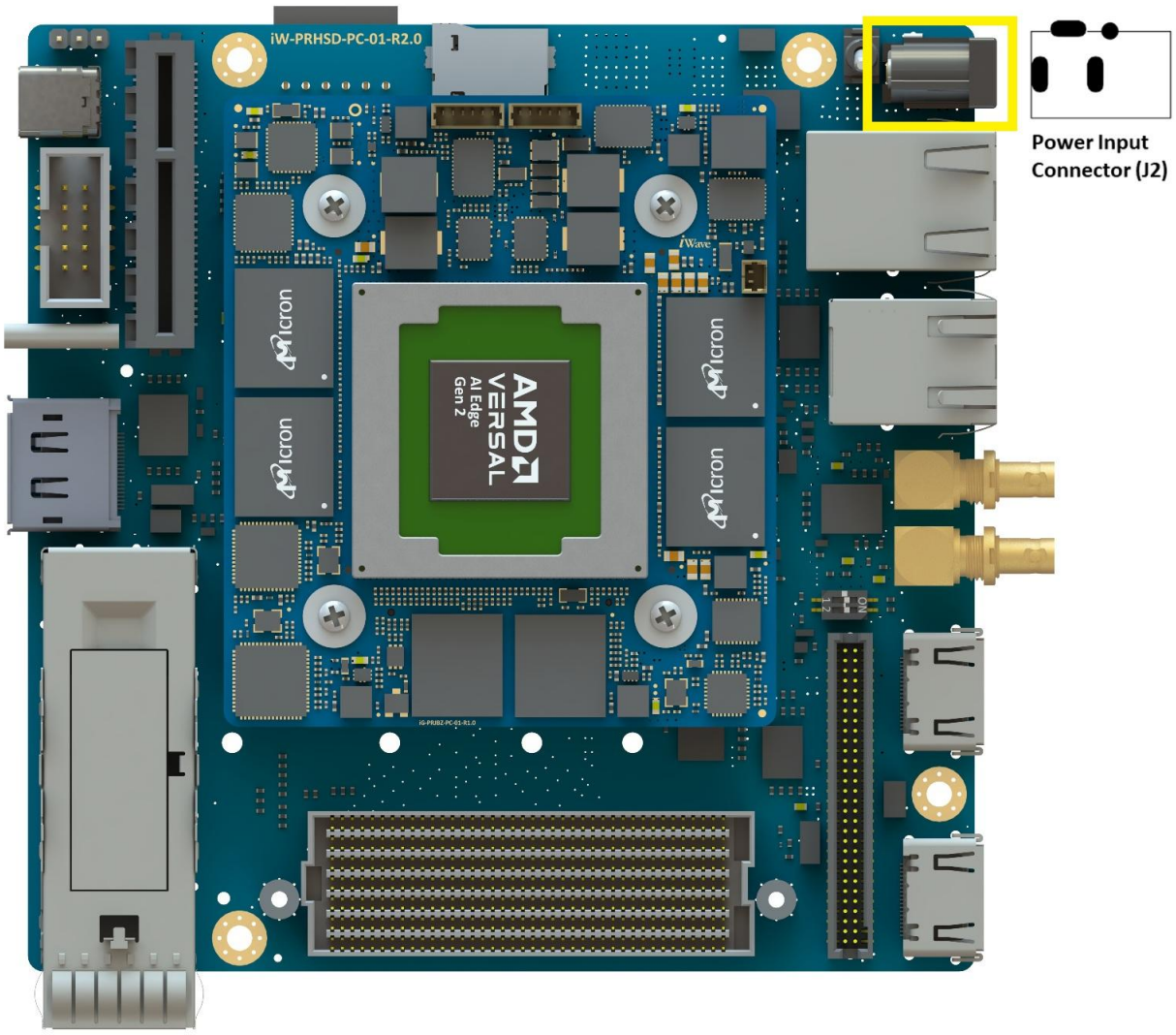


Figure 34: Power Jack

The below table provides the Power Input Requirement Versal AI Edge Gen2 Development Board.

Table 19: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.4	12V	12.6V	±50mV
2	VRTC_3V0[1]	0	3V	3.15V	±20mV

[1] The Versal AI Edge Gen2 Devkit uses this voltage as backup power source to On-SOM PMIC RTC controller when VCC is off.

3.2 Power Output Specification

The Versal AI Edge Gen2 SOM development Board has dedicated power regulator to provide +5V power to SOM for VCC power supply. Also +3V RTC power from coin cell holder is provided for Real time clock support.

The Versal AI Edge Gen2 SOM development Board also shares different on-board power to FMC+ connector, Pmod connector, QSFP+ Connector and GPIO Headers for its Add-On Module power.

Table 20: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current
To Board-to-Board Connector2 (for Versal AI Edge Gen2 SOM)					
1	VCC_5V	4.85V	5V	5.15V	25A
2	VRTC_3V0	0V	3V	3.15V	-
To FMC+ Connectors					
1	VCC_FMC+_ADJ	0.95	1.2	1.26	4A
2	VCC_3V3	3.135	3.3	3.465	3A
3	3P3VAUX	3.135	3.3	3.465	100mA
4	VCC_12V	11.4	12V	12.6V	1A
To Pmod Connector					
1	VCC_3V3	3.15	3.3	3.45	100mA
To QSFP+ Connector					
1	VCC_3V3	3.15	3.3	3.45	1A
To GPIO Header					
1	VCC_5V	4.85V	5V	5.15V	500mA
2	VCC_1V8	1.75	1.8	1.85	100mA
3	VIO_BANK2	1.14	1.2	1.26	40mA

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of Versal AI Edge Gen2 SOM Development platform.

Table 21: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	0°C	70°C

[1] *iWave only guarantees the component selection for the given operating temperature.*

3.3.2 RoHS Compliance

iWave's Versal AI Edge Gen2 SOM Development platform is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's Versal AI Edge Gen2 SOM Development platform is sensitive to electrostatic discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 Development Board Mechanical Dimensions

The REN Development board PCB form factor is 120mm x 120mm and Board mechanical dimension is shown below.

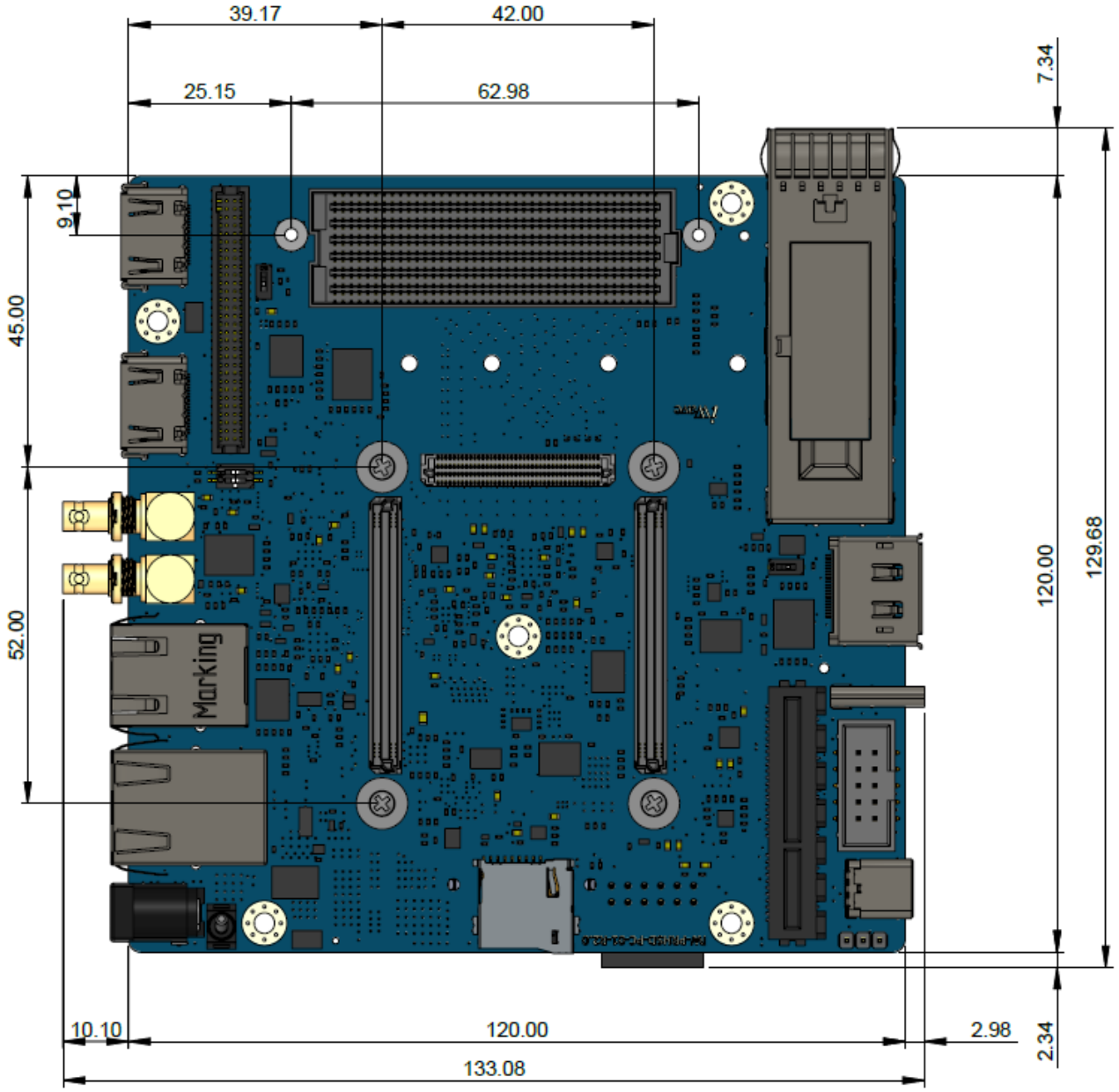


Figure 35: Development board Mechanical dimension – Top View

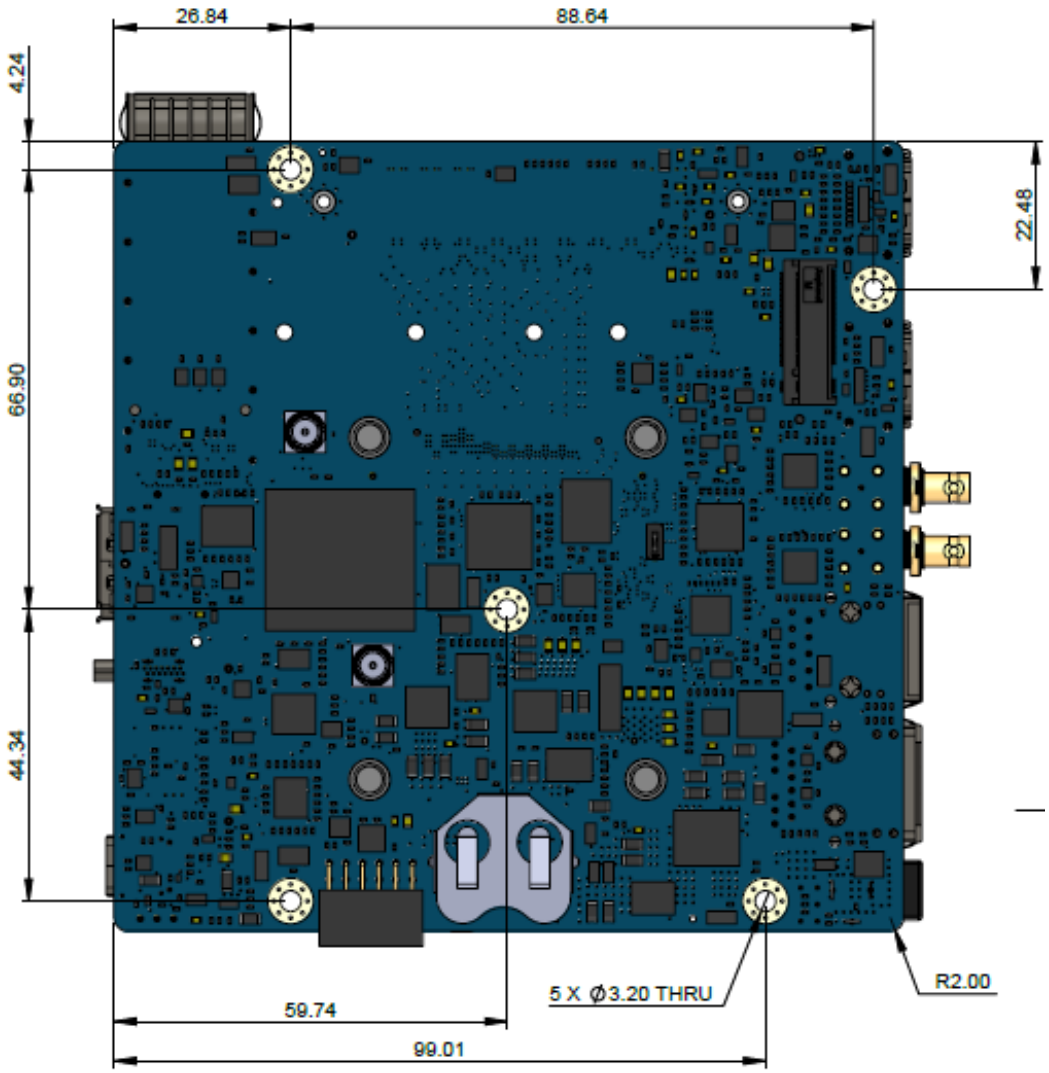


Figure 36: Development board Mechanical dimension – Bottom view

The REN Development board PCB thickness is 1.83mm±0.1mm, top side maximum height component is Ethernet MagJack Connector (15.27mm) and bottom side maximum height component is CMC (9.53mm). Please refer the below figure for height details of the Versal AI Edge Gen2 SOM development board.

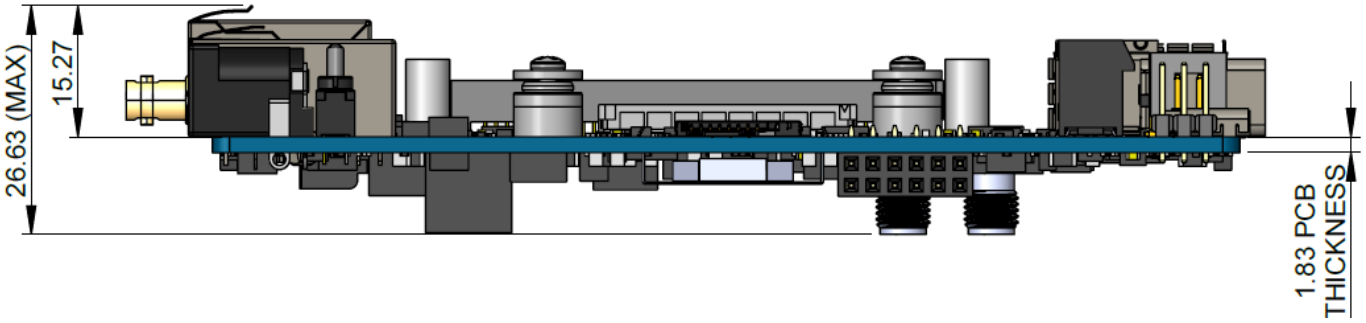


Figure 37: Development board Mechanical dimension – Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for Versal AI Edge Gen2 Development platform which includes Versal AI Edge Gen2 SOM and Development Board.

Table 22: Orderable Product Part Numbers

Product Part Number	Description	Temperature
TBD		

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.

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mktg@iwave-global.com

iWave
Bangalore, India

iWave USA
Campbell, California

iWave Global
Ras Al Khaimah, UAE

iWave Global GmbH
Ratingen, Germany

iWave Europe
Rotterdam, Netherlands

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