AS7150

Datasheet

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AS7150 Optical force sensing analog front end

1 General description

The AS7150 is a low noise, high dynamic range proximity detection analog front end that has been optimized for optical force sensing application for consumer market.

The device consists of two low-noise ADC channels capable of simultaneous acquisition of two photodiodes. The integrated LED driver and high integration factor with the small 1.67 mm x 1.67 mm WLCSP package is ideally suited for space constraint force and proximity applications where the optical front end needs to be decoupled from the analog front end.

The proximity function synchronizes IR emission and detection to sense nearby objects. The architecture of the engine features low noise, high dynamic range, ambient light subtraction, FIFO, and interrupt-driven I²C communication.

Sensitivity, power consumption, and noise can be optimized with adjustable LED timing and power. The proximity engine recognizes detect/release events and produces a configurable interrupt whenever the proximity result crosses the upper or lower threshold settings.

1.1 Key benefits & features

The benefits and features of AS7150, Optical force sensing analog front end are listed below:

Table 1: Added value of using AS7150

Benefits	Features
High measurement resolution OFS (5µm)	• 20-bit true current input analog to digital converter • High Signal to Noise ratio (90dB) • On-chip averaging support
Simultaneous proximity and force measurement	• State machine measurement range reconfiguration • Up to 3 photodiode inputs • Up to 3 LED input
Small system footprint	• Tiny 1.68 x 1.68 x 0.4mm Wafer-Level-Chip-Scale-Package (WLCSP) • Little external component count
Ultra low power consumption	• State machine triggered sleep mode • 1.8V chip supply with 1.8V I²C bus • Proximity IRQ function for MCU wakeup • On-chip FIFO memory

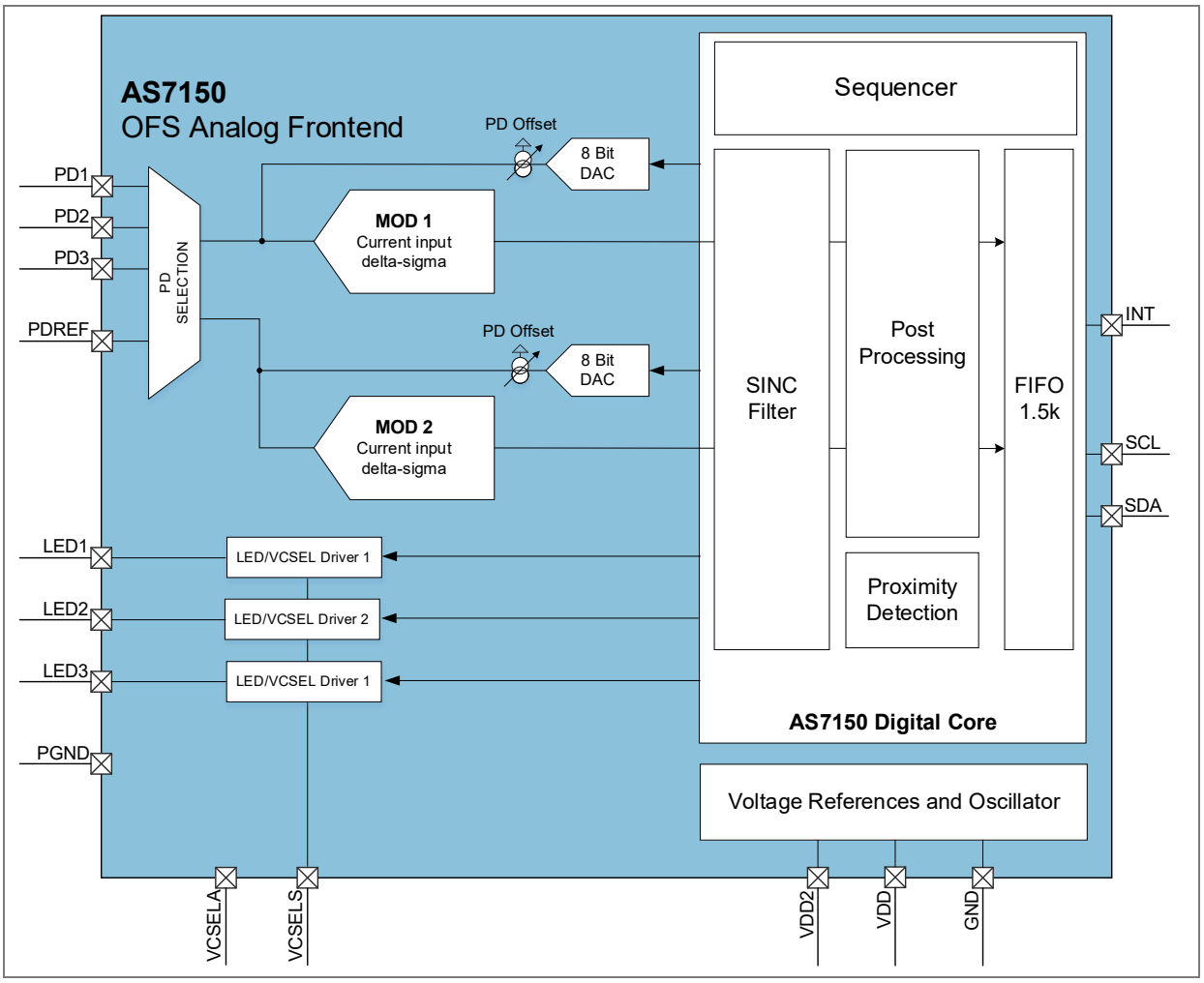
1.2 Applications

- Mobile phones
- Tablets
- Smart glasses
- Earbuds

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 1: Functional blocks of AS7150



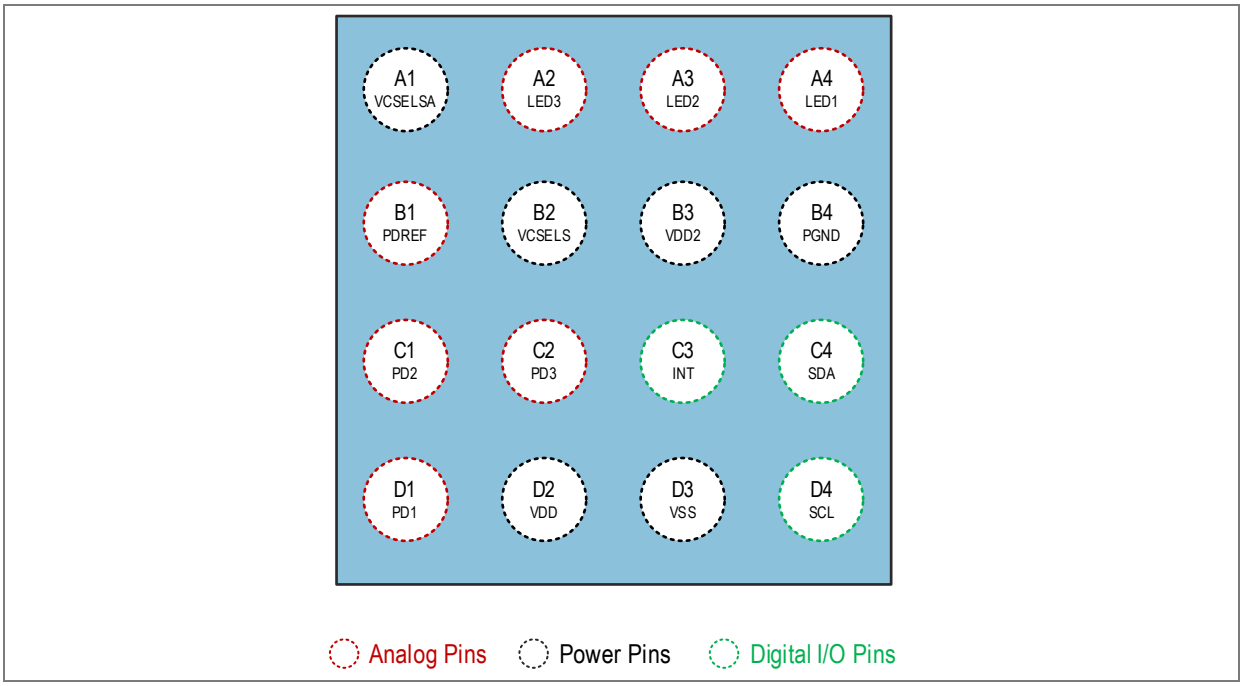
2 Ordering information

Ordering code	Product type	Description	Package	Delivery form	Delivery quantity
Q65115A0139	AS7150	AS7150 Optical Force Sensing AFE	WLCSP	Tape & reel	10000pcs/reel

3 Pin assignment

3.1 Pin diagram

Figure 2: Pin diagram of AS7150



3.2 Pin description

Table 2: Pin description of AS7150

Pin number	Pin name	Pin type(1)	Description
A1	VCSELA	AO	Pin must be left unconnected.
A2	LED3	AI	LED driver 3 current sink LED input pin.
A3	LED2	AI	LED driver 2 current sink LED input pin.
A4	LED1	AI	LED driver 1 current sink LED input pin.
B1	PDREF	AO	Reference voltage terminal for photodiodes.
B2	VCSELS	AI	LED driver supply input terminal. Mind that this pin must be connected the V_{LED} supply.
B3	VDD2	P	Digital supply input pin. This pin needs to be connected via a pull up resistor to V_{VDD} chip supply.
B4	PGND	G	Power ground terminal for integrated LED driver current sinks.
C1	PD2	AI	Photodiode input number 2.
C2	PD3	AI	Photodiode input number 3.
C3	INT	DO	Digital interrupt push pull output pin.
C4	SDA	DO	I²C data interface pin.
D1	PD1	AI	Photodiode input number 1.
D2	VDD	P	Positive supply terminal of AS7150.
D3	VSS	G	Negative supply terminal of AS7150.
D4	SCL	DI	I²C clock interface pin.

(1) Abbreviations:
DI Digital Input
DO Digital Output
AI Analog Input
AO Analog Output
P Power Supply
G Ground

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of AS7150

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameters					
V_{VDD_MAX}	Positive supply voltage	-0.3	1.98	V	VDD to VSS
V_{VDD2_MAX}	Analog supply voltage	-0.3	1.98	V	VDD2 to VSS
V_{VCSELS_MAX}	VCSELS supply voltage	-0.3	5.5	V	VCSELS to AGND
V_{VCSELA_MAX}	VCSELA pin voltage	-0.3	5.5	V	VCSELA to AGND
$V_{VCSELA-VCSELS}$	Voltage difference between pins VCSELA and VCSELS	-0.3	0.3	V	Internal diode to V_{VCSELS}
V_{LED_MAX}	LED pin voltage	-0.3	5.5	V	Applicable to pins LED1, LED2 and LED3
$V_{IN\_MAX\_MAX}$	Maximum analog and digital input voltage	-0.3	V_{VDD}+0.3 V max. 1.98 V	V	Applicable to pins PD1, PD2, PD3, SDA and SCL. Internal ESDD protection diode to VDD pin present on analog and digital input pins.
$V_{GND-PGND}$	Power to analog ground voltage difference	-0.3	0.3	V	
$I_{LED\_AVER\_}$	Average LED ON current		35	mA	DC current with all LEDs ON during all 8 time slots
I_{SCR}	Input current (latch-up immunity)	± 100		mA	JEDEC JESD78E
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM	± 2		kV	JS-001-2017
ESD_{CDM}	Electrostatic discharge CDM	± 500		V	JS-001-2017
Temperature ranges and storage conditions					
T_{AMB}	Operating ambient temperature	-30	85	°C	
T_{STRG}	Storage temperature range	-40	125	°C	

Symbol	Parameter	Min	Max	Unit	Comments
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level		1		According to JEDEC J-STD-020E Represents a max. floor life time of unlimited
$t_{STRG\ DOF}$	Storage time for DOF/Die or wafers on foil		3	months	Refers to indicated date of packing

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn)

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Conditions: T_A = 25 °C, V_{VDD} = 1.8 V; V_{VDD2} = 1.8 V

Table 4: Electrical characteristics of AS7150

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDD}	Supply voltage VDD pin		1.70	1.80	1.98	V
V_{VDD2}	Supply voltage VDD2 pin		1.70	1.80	1.98	V
V_{VCSELS}	VCSELS supply voltage	Voltage must not be below V_{LED}	1.75		5.50	V
Photodiode inputs						
C_{PD}	Total photodiode capacitance connected to MOD1 or MOD2	0 V reverse voltage			300	pF
I_{PD}	Photocurrent input				64	µA
MOD1 & MOD2 (PPG Channels)						
I_{PD}	Photodiode input current range	Configurable ADC input full scale current range via register **MODx_SEQx_IREF** with 1µA step size	1		64	µA
MOD_{RES}	ADC resolutions of MOD1 and MOD2			20		bit
f_{MOD_SAMPL}	Typical modulator sampling frequency		0.5	25	1000	Hz
C_{PD}	Total photodiode capacitance connected to PPG_ADC	0 V reserve voltage		60	300	pF
MOD_{DAC_OFF}	DAC ambient light cancellation offset current full-scale range for MOD1 or MOD2	**MODx_IOS_FS** = 0		1		µA
		MODx_IOS_FS = 1		2		
		MODx_IOS_FS = 2		4		
		MODx_IOS_FS = 3		8		
		MODx_IOS_FS = 4		16		
		MODx_IOS_FS = 5		32		
		MODx_IOS_FS = 6		64		

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		MODx_IOS_FS = 7		128		
LED driver						
LED_{RES23}	LED driver resolution	Applicable to LED2 and LED3 driver		7		Bit
LED_{RES1}	LED driver resolution	Applicable to VCSEL LED1 driver		6		Bit
I_{RANGE1}	LED1 current range			20		mA
V_{COMP_LED1}	LED1 driver compliance voltage	I_{LED}=20mA			0.3	V
$I_{RANGE23}$	LED2 and LED3 current range			200		mA
V_{COMP_LED23}	LED1 and LED2 driver compliance voltage	I_{LED}=200mA			0.4	V
Digital input SCL and SDA						
V_{IH}	Input high	Switching threshold while rising edge of the input signal is introduced	0.54		1.26	V
V_{IL}	Input low	Switching threshold while falling edge of the input signal is introduced	0.54		1.26	V
Digital output SDA						
V_{OH}	Output high	Pin's source load current is 6 mA condition: E2=E4="1" (full available driver strength)			V_{VDD}-0.4	V
V_{OL}	Output low	Pin's sink load current is 6 mA condition: E2=E4="1" (full available driver strength)			0.4	V
Digital output INT						
V_{OH}	Output high	Pin's source load current is 2 mA condition: E2=E4="1" (full available driver strength)			V_{VDD}-0.4	V
V_{OL}	Output low	Pin's sink load current is 2 mA condition: E2=E4="1" (full available driver strength)			0.4	V

5.1 Power consumption

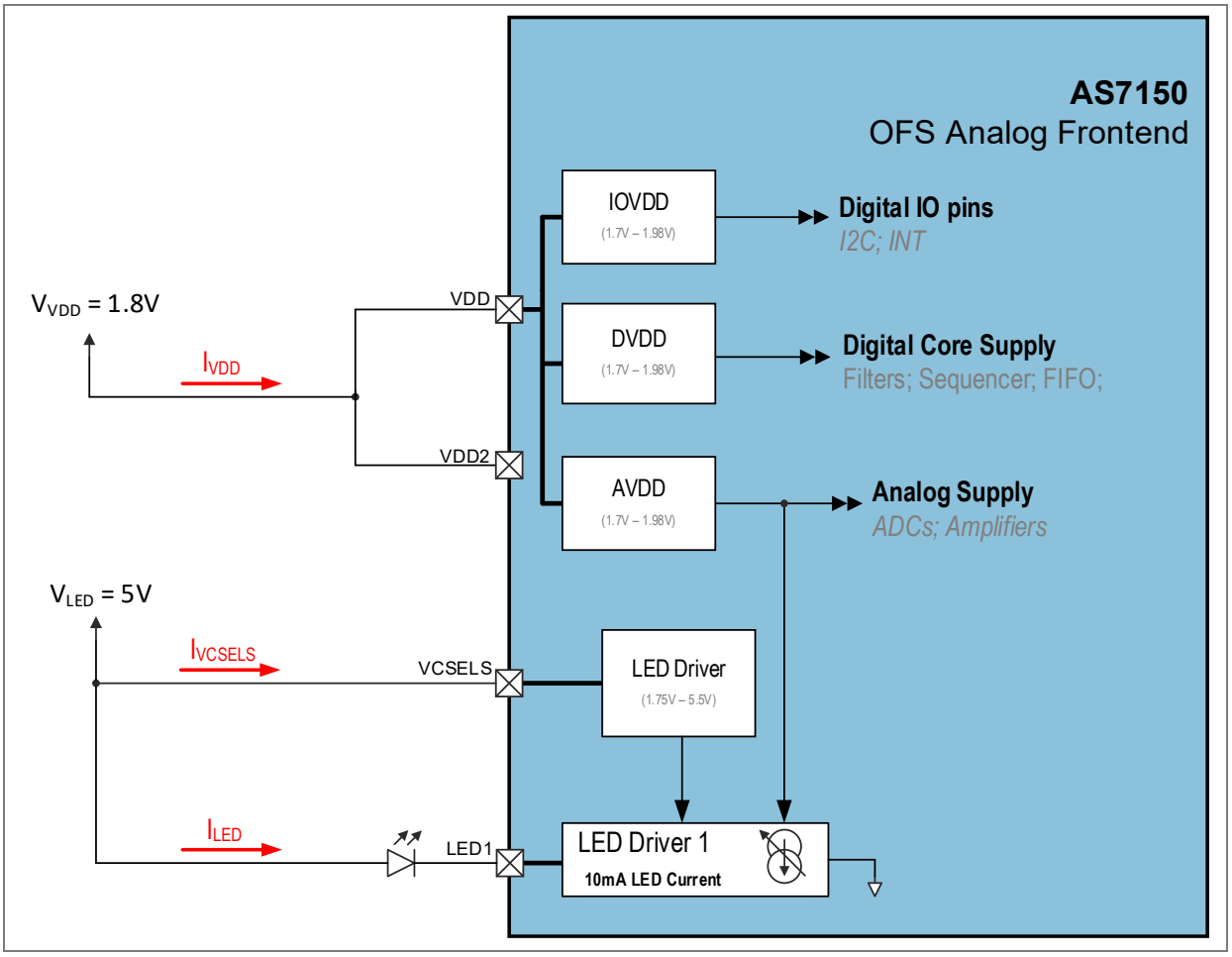
This chapter contains typical power consumption values for PPG and ECG measurements. The measurement setup is shown in Table 5.

Conditions: T_A = 25 °C, V_{VDD} = 1.8V, V_{VDD2} = 1.8V, V_{VCSELS} = 5V

Table 5: Typical power consumption

Symbol	Operation mode	Measurement conditions	Typ. I_{VDD}	Typ. I_{VCSELS}	Typ. I_{LED}	Unit
I_{PD}	Supply current in power down mode		1.1	-	-	µA
I_{IDLE}	Supply current in idle mode	If_osc_on=1	2.92	-	-	µA
I_{FORCE_25Hz}	Force current consumption; 25 Hz sample rate	Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; f_s=25 Hz; f_{MOD_CLK}=10 MHz; $t_{INTEGRATION}$=12.8 µs	10	0.01	3.2	µA
		Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; f_s=25 Hz; f_{MOD_CLK}=10 MHz; $t_{INTEGRATION}$=51.2 µs	14.4	0.01	12.8	µA
		Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; f_s=25 Hz; f_{MOD_CLK}=10 MHz; $t_{INTEGRATION}$=102.4 µs	20.2	0.01	25.6	µA
I_{FORCE_100Hz}	Force current consumption; 100 Hz sample rate	Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; f_s=100 Hz; f_{MOD_CLK}=10 MHz; $t_{INTEGRATION}$=12.8 µs	31.1	0.01	12.8	µA
		Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; f_s=100 Hz; f_{MOD_CLK}=10 MHz; $t_{INTEGRATION}$=51.2 µs	49.5	0.01	51.2	µA
		Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; f_s=100 Hz; f_{MOD_CLK}=10 MHz; $t_{INTEGRATION}$=102.4 µs	73	0.01	102	µA

Figure 3: Block diagram of power consumption measurement setup



6 Typical operating characteristics

Figure 4: SNR vs. PD current; ADC FS range = 64 µA; f_S = 200 Hz; t_{INT} = 27 µs

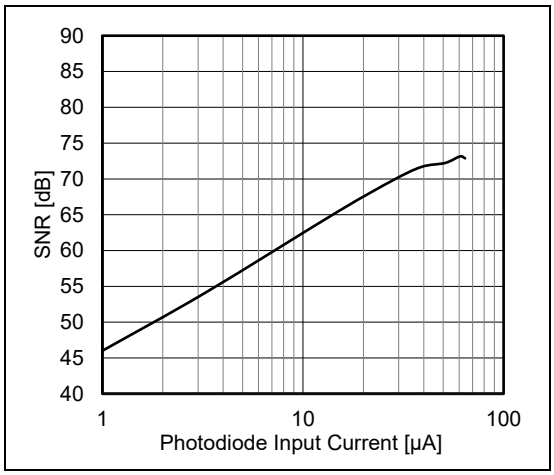


Figure 5: SNR vs. PD current; ADC FS range = 64 µA; f_S = 200 Hz; t_{INT} = 52 µs

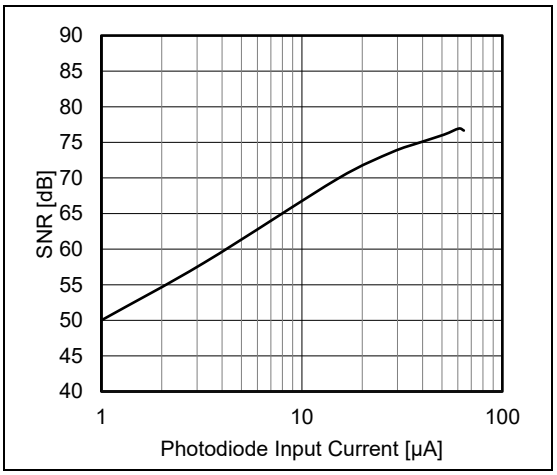


Figure 6: SNR vs. PD current; ADC FS range = 64 µA; f_S = 200 Hz; t_{INT} = 129 µs

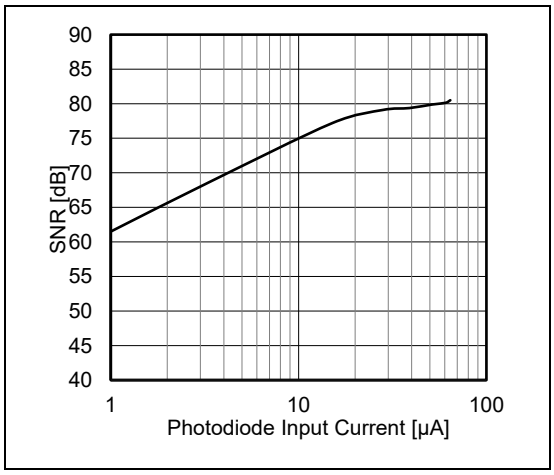


Figure 7: SNR vs. PD current; ADC FS range = 32 µA; f_S = 200 Hz; t_{INT} = 27 µs

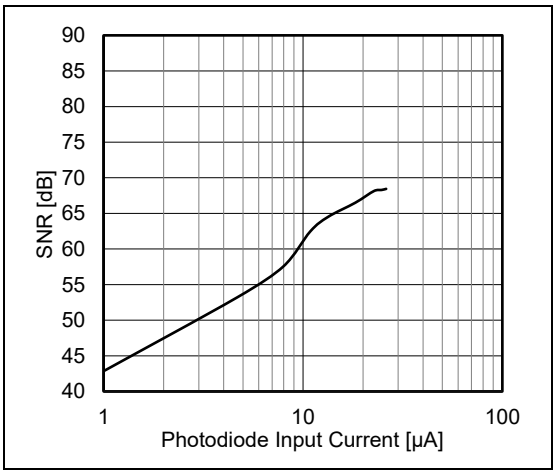


Figure 8: SNR vs. PD current; ADC FS range = 32 µA; f_S = 200 Hz; t_{INT} = 52 µs

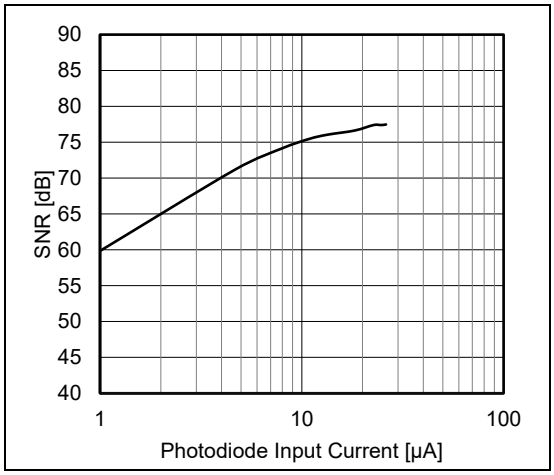
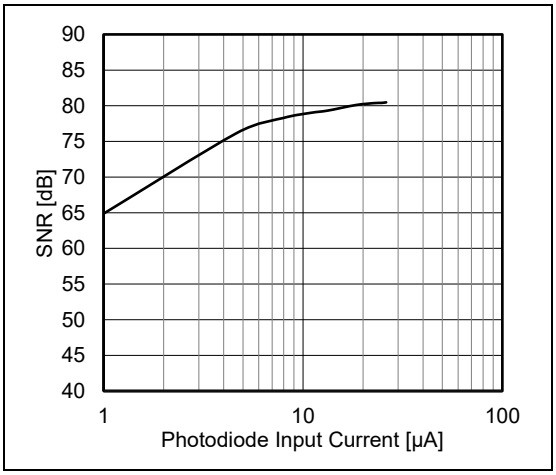


Figure 9: SNR vs. PD current; ADC FS range = 32 µA; f_S = 200 Hz; t_{INT} = 129µs



7 Functional description

The AS7150 is a low-power solution for optical force sensing (OFS) signal acquisition typically used in consumer applications for button and proximity detection. The AS7150 provides three low-noise LED current sinks along with two 20-bit ADCs featuring true simultaneously photodiode sampling.

The AS7150 is optimized for optical force sensing products with the following strengths:

- Low noise, high dynamic range optical force acquisition
- Simultaneous sampling of two photodiode channels
- Small system size
- Integrated 3 channel low side LED driver
- Proximity detection function
- Various different options for automatic offset cancellation
- Lowest power consumption

The AS7150 AFE contains two main blocks. An analog front-end for LED driving, signal acquisition, photodiode selection, and signal preconditioning. Moreover, a digital backend for signal filtering, balancing, and sampling. Furthermore, the digital block will handle the sensor configuration, control, and communication to the external MCU.

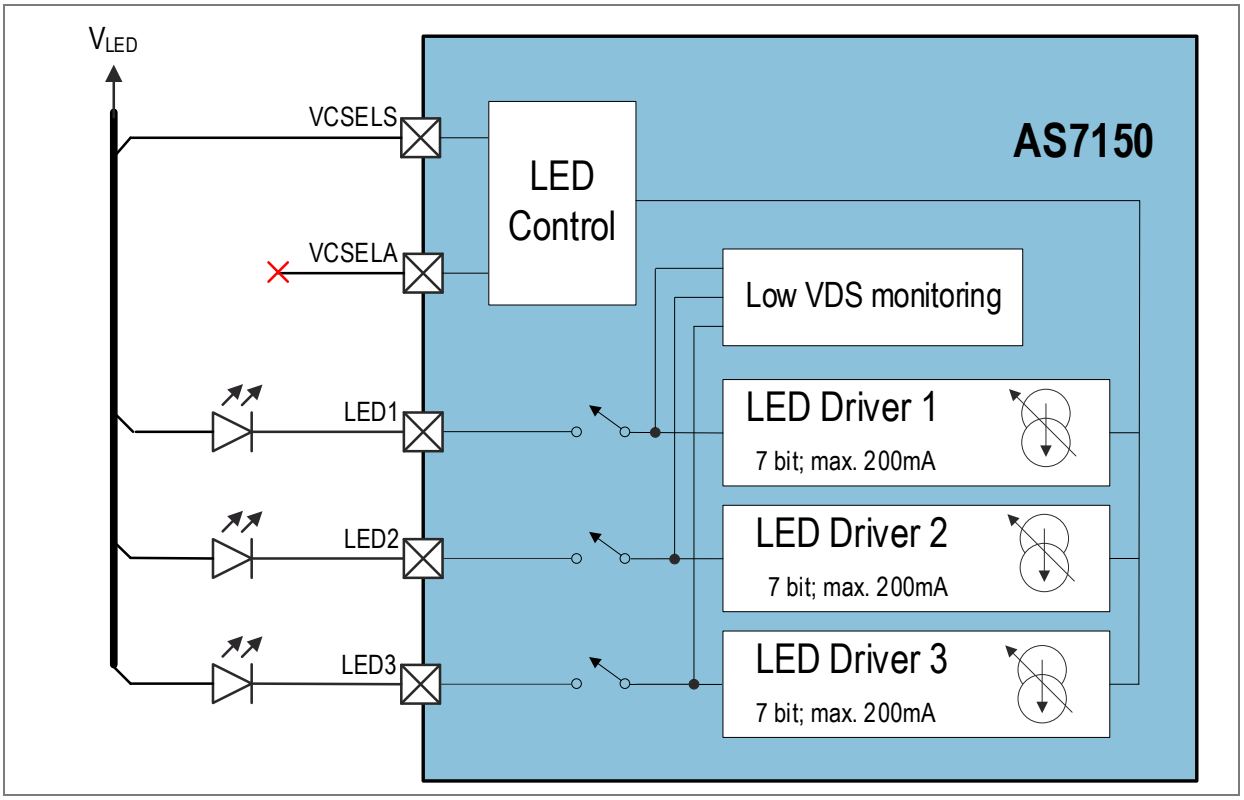
The I²C interface controls all the functions of the AS7150. All the functions can be controlled with an external MCU via the I²C interface while AS7150 is in active mode. The following chapters provide more detailed descriptions of all functional blocks of AS7150.

7.1 LED driver

AS7150 features two internal LED current sinks with internal multiplexers to connect three LED inputs. The LEDs are controlled and configured via a digital sequencer to unload the host MCU with configuration and tasks. Its configuration and assignment options are shown in chapter 7.5 PPG sequencer and can be configured via a convenient graphical user interface.

Each Led driver can support LED currents up to 200mA which can be controlled in 64 steps for the different sequencers with dedicated control registers **SEQ1_LED1_CURR**, **SEQ2_LED1_CURR, SEQ1_LED2_CURR, SEQ2_LED2_CURR, SEQ1_LED3_CURR** and **SEQ2_LED3_CURR.**

Figure 10: LED driver block diagram

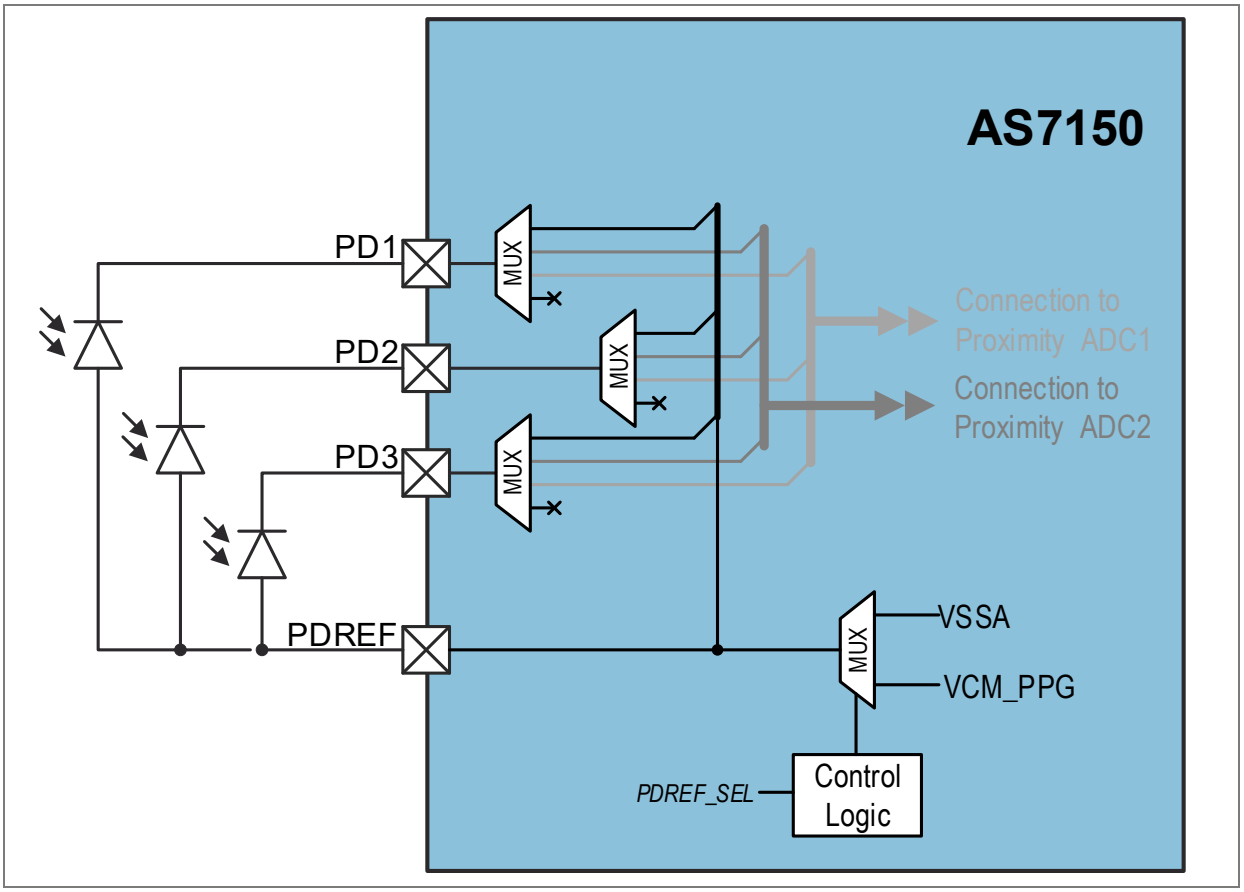


All LED input drivers are equipped with a voltage monitoring function. The Low VDS block monitors the input pad voltages. In case the voltage drops below 0.3V an interrupt is released which can be enabled via the **IRQ_EN_LED_LOWVDS** register. A voltage below 0.3V is an indication that the target LED current cannot be reached. In order to avoid false detections, the monitoring block is also linked to the device sequencer to make sure that the monitoring function is only active when the LED driver is enabled and actively driving LED current. Furthermore, it is possible to define also a debouncing time when the LED driver is switched on. The register **LOWVDS_WAIT** declares the delay time when the LED driver is switched on and the start of the voltage monitoring of the LED driver to avoid false detection due to ringing effects while the LED is switched on. Once an interrupt is released, due to an undervoltage condition, the status register **LED_LOWVDS** holds the information which LED drivers caused the undervoltage condition.

7.2 Photodiode inputs

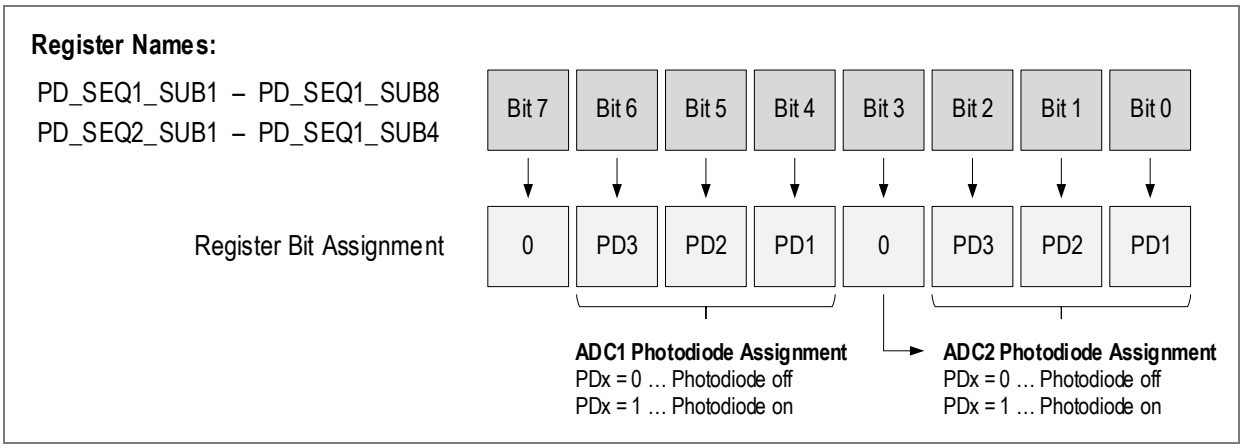
The AS7150 supports up to three photodiode inputs which can be routed to both analog to digital converters for highest design flexibility. A simplified block diagram which shows the input structures of the photodiode inputs is shown in Figure 11. Each photodiode input features a dedicated multiplexer that allows each photodiode to be connected to proximity ADC1, proximity ADC2 or to PDREF pin which is the default connection to short circuit the photodiodes when not in use. This is also the reset state after power-up and when no measurement is ongoing. The input multiplexers are controlled automatically with the built-in measurement sequencer and get connected and disconnected while a measurement is ongoing, according to the device configuration.

Figure 11: Photodiodes input selection



The registers **PD_SEQ1_SUBx** and **PD_SEQ2_SUBx** are used for the photodiode assignment where “x” represents the subsample number for sequencer 1 and sequencer 2. In default mode, bit 7 and bit 3 remain set to zero. Bits 6:4 are used to select the photodiodes for ADC1, while bits 2:0 are used to select the photodiodes for ADC2. For ADC1, bit 6 corresponds to PD3 input, bit 5 corresponds to PD2 input, and bit 4 to PD1 input. In the same way bits 2:0 are used for ADC2 and its photodiode assignment. A graphical overview of the bit assignments for **PD_SEQ1_SUBx** and **PD_SEQ2_SUBx** registers is shown in Figure 12.

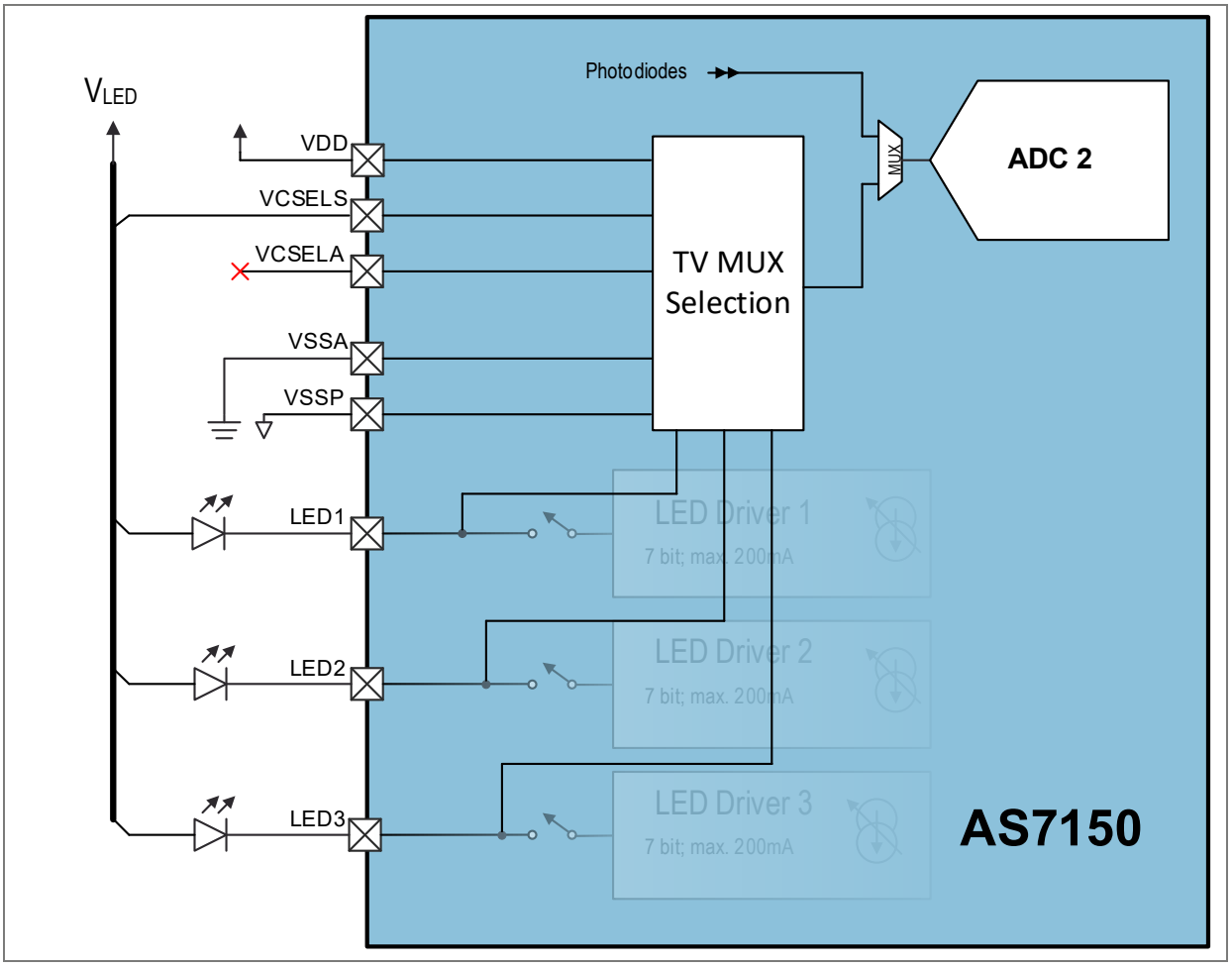
Figure 12: Photodiode selection register bit assignment



7.3 ADC2 voltage measurements

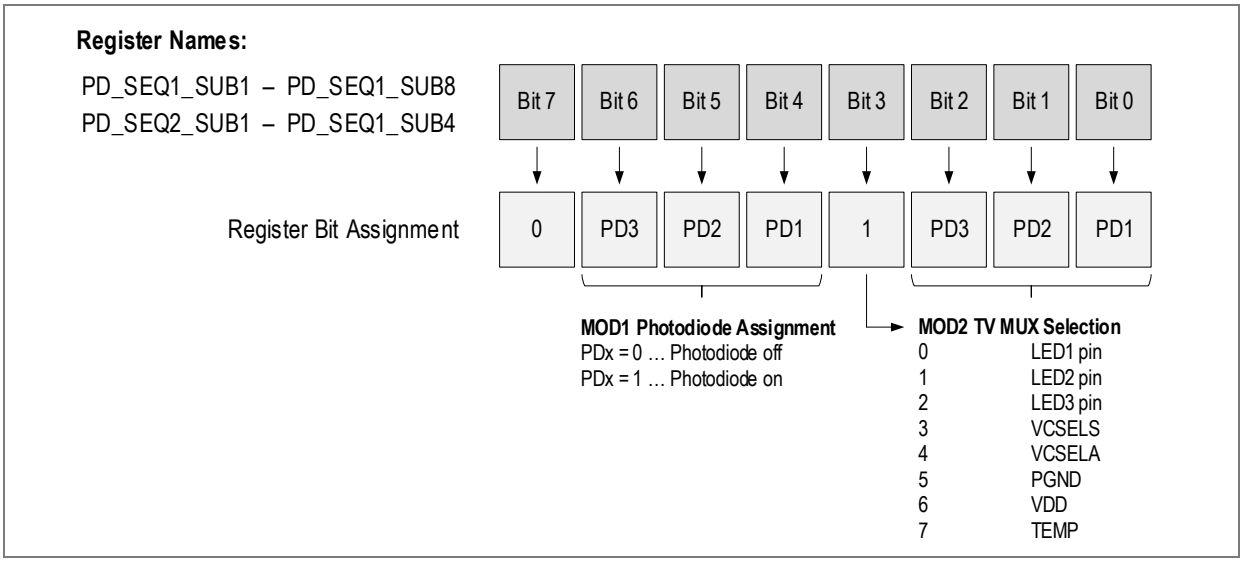
While ADC1 can only be assigned to photodiode inputs ADC2 offers the functionality to be connected to photodiode inputs or via an input multiplexer to various voltage monitoring nodes. The simplified block diagram shown in Figure 13 shows the various input voltage options which can be assigned to ADC2.

Figure 13: MOD2 voltage measurement register bit assignment



In order to connect ADC2 to an external voltage, bit 3 has to be set to one inside the PD_SEQx_SUBy register. Figure 14 below shows bit 3 of the PD_SEQx_SUBy register set to logic high. In this case, bit 2:0 decides which of the external voltages will be connected to ADC2. The photodiode current and the external voltages can be simultaneously measured via ADC1 and ADC2 respectively.

Figure 14: ADC2 voltage monitoring TV MUX selection



In order to measure the analog input voltages via ADC2 two methods (ratio-metric method and slope-based method) can be used which are described in the following chapters.

7.3.1 Ratio-metric method

This method is preferred over the slope-based method because, in this case, two measurements are taken over the same channel, thereby eliminating the effect of AGAIN values, gain error, and offset error during measurements. For the selected voltage input, using bit 2:0 (0-6), a 250kΩ resistor converts it into a current, which is applied at the input of ADC2. One end of this resistor is connected to VCM (input port of ADC2), while the other end is to one of the voltages to be measured.

1. First, measure the VCSELA/GND by setting a decimal value of 4 in the above register. The twenty-bit signed ADC output (d0 d1 d2 ... d19) for this register setting can then be converted into its analog counterpart as shown below with Equation 1 or Equation 2.

Equation 1:

$$ADC_{OUT\_GND} = \frac{d1}{2^1} + \frac{d2}{2^2} + \cdots + \frac{d19}{2^{19}}$$

Equation 2:

$$ADC_{OUT\_GND} = \frac{d1 * 2^{N-1} + d2 * 2^{N-2} + \cdots + d19 * 2^{N-N}}{2^N}$$

Note that the above formulae do not include d0 or MSB, which serves as a “sign” bit for the signed binary output. The above formulae scale the digital output into its analog counterpart part between zero and one.

2. Afterwards, set the register to a value required for measuring the voltages, such as LED1, and scale the ADC output into its analog counterpart, ADC_{OUT}, as done in step 1, and use the following formulae to estimate the input voltage:

Equation 3:

$$V_{IN} = \mathrm{VCM} * \left(1 - \frac{ADC_{OUT}}{ADC_{OUT_{GND}}}\right)$$

If V_{IN} is connected to ground, ADC_{OUT} is equal to ADC_{OUT_GND}. If V_{IN} is the same as VCM, ADC_{OUT} is equivalent to zero input current.

7.3.2 Slope-based method

This method requires us to use the slope for the given AGAIN value.

1. Once we know the reference slope, which can be measured using a DAC input, and the measured ADC_{OUT}, we can find out the corresponding ADC input current ADC_{IN}:

Equation 4:

$$ADC_{IN} = \frac{ADC_{OUT}}{SLOPE_{REF}}$$

2. Use this value of ADC_{IN} in the formulae below to calculate V_{IN}, which is one of the six external voltages applied:

Equation 5:

$$V_{IN} = \mathrm{VCM} - (ADC_{IN} * 250k)$$

This method requires you to measure the current through the resistor and depends on the gain and offset error of the ADC. Therefore, this method is not preferred.

7.4 PPG ADCs

The data acquisition signal path of AS7150 features two parallel synchronous current input analog to digital converters. Both ADC channels shown in Figure 15 and Figure 16 do provide same functionality and support true synchronous sampling of the assigned photodiode inputs. Therefore, it is possible to read out two photodiodes in a single PPG subsample measurement.

Figure 15: PPG ADC 1 signal path

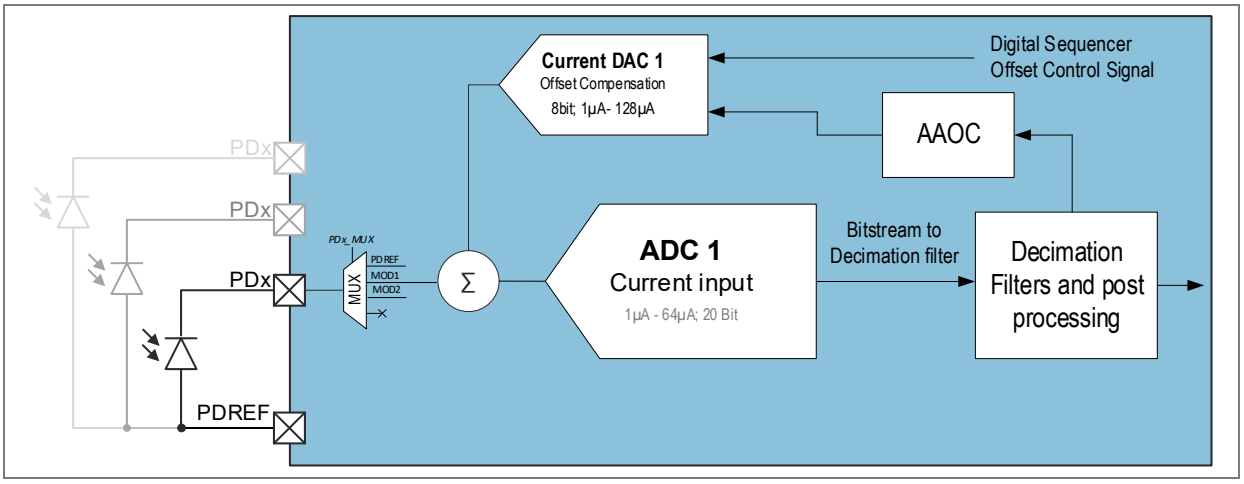
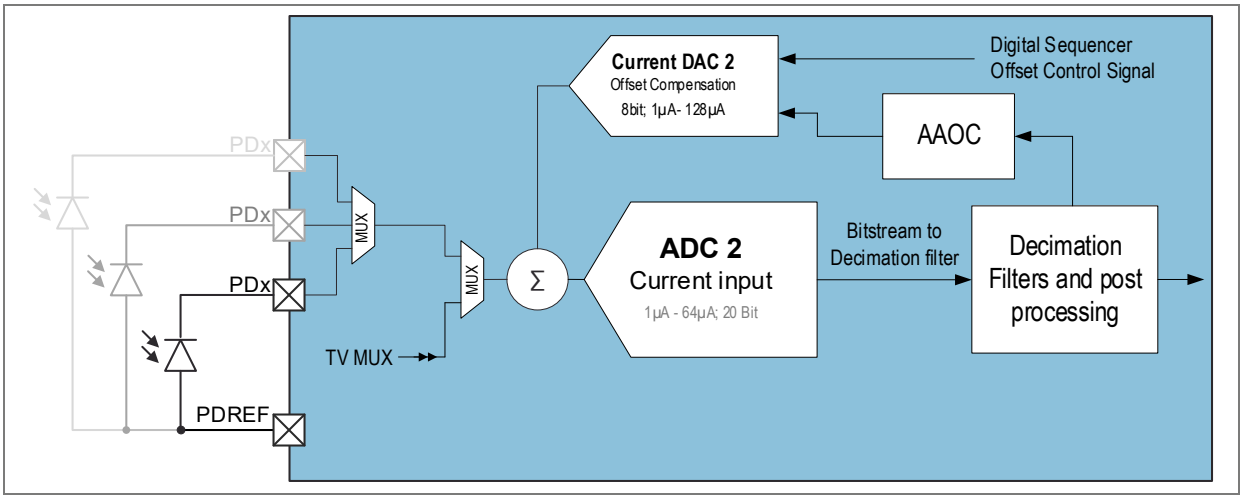


Figure 16: PPG ADC 2 signal path



For applications requiring only one signal path to be active, one of the two channels can certainly be powered down via simple register control to reduce overall system power consumption. Each ADC signal path supports seven full-scale range settings of 1 µA, 2 µA, 4 µA, 8 µA, 16 µA, 32 µA, and 64 µA which can be configured in register **MOD1_SEQ1_IREF**, **MOD1_SEQ2_IREF**, **MOD2_SEQ1_IREF**, and **MOD2_SEQ2_IREF** for each sequencer and ADC independently. In addition to the full-scale settings both ADCs have additional configuration registers **MOD1_CFGx** and **MOD2_CFGx** which allow the configuration of the decimation filters and filter order to control the desired integrations times which are the determining factor for signal integrity as well as noise behavior for the target application. Since the different configuration registers do allow for many different configuration options Table 6 provides an overview of the typically recommended configuration of the registers for all different ADC input current ranges.

Table 6: ADC1 and ADC2 FSR settings

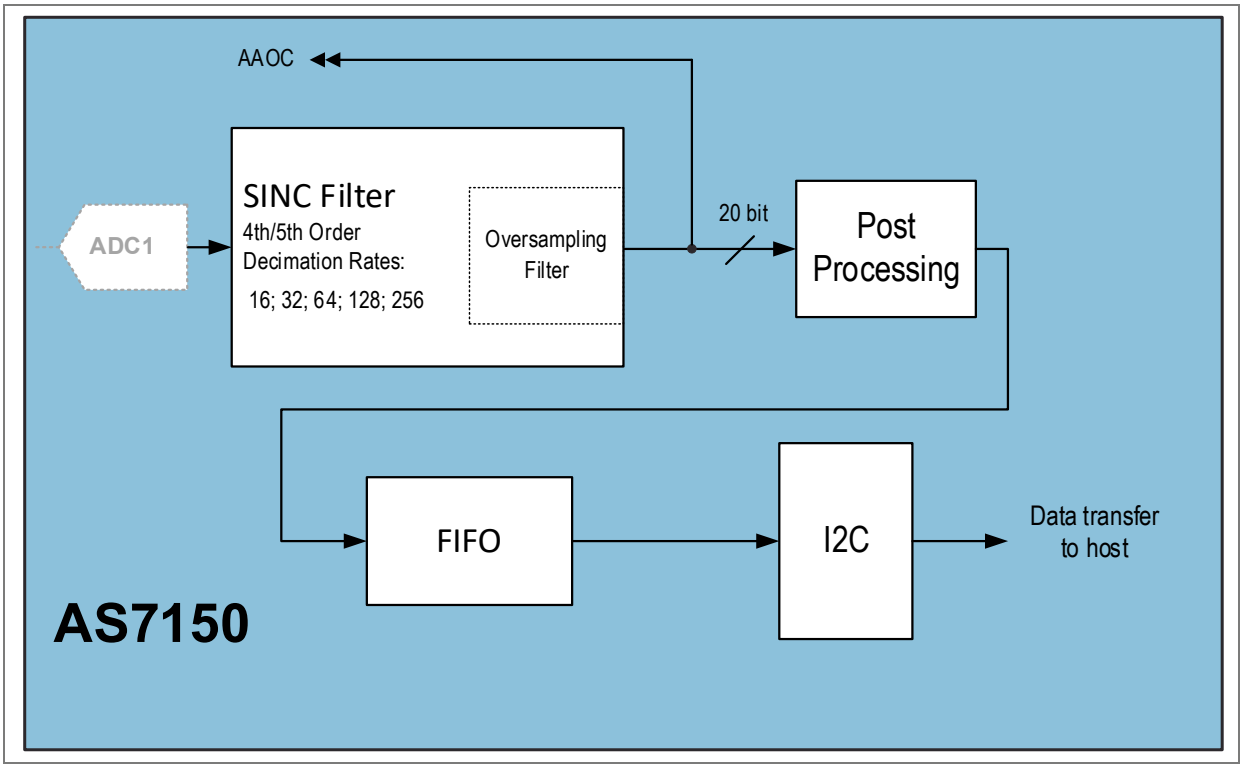
Register	Address	ADC modulator	Assigned sequencer	ADC modulator full scale input current range				
				4µA	8µA	16µA	32µA	64µA
MOD1_CFGC	0x1d	MOD1	Sequencer 1	0x27	0x27	0x2F	0x1F	0x1F
MOD1_CFGD	0x1e			0x03	0x07	0x0F	0x1F	0x3F
MOD1_CFGE	0x1f		Sequencer 2	0x27	0x27	0x2F	0x1F	0x1F
MOD1_CFGF	0x20			0x03	0x07	0x0F	0x1F	0x3F
MOD2_CFGC	0x23	MOD2	Sequencer 1	0x27	0x27	0x2F	0x1F	0x1F
MOD2_CFGD	0x24			0x03	0x07	0x0F	0x1F	0x3F
MOD2_CFGE	0x25		Sequencer 2	0x27	0x27	0x2F	0x1F	0x1F
MOD2_CFGF	0x26			0x03	0x07	0x0F	0x1F	0x3F

Each signal path also includes an 8-bit offset current DAC with up to 128µA offset current for extending the optical dynamic range by sourcing some of the exposure current via the offset DAC. This feature helps to avoid saturation of the ADC under high ambient light exposure. The full-scale current range of the offset DAC can be controlled via register **MOD1_IOS_FS** and **MOD2_IOS_FS**. The current of the offset DAC can be directly controlled via a dedicated registers **AOC_MOD1_SEQ1_SUBX**, **AOC_MOD1_SEQ2_SUBX** for modulator one and for modulator two via register **AOC_MOD2_SEQ1_SUBx**. This allows engineers to utilize their own offset compensations algorithms running on the host signal-processing unit. However, in case customers do not have an algorithm in pace, AS7058 features also an Advanced Automatic Offset Cancellation (AAOC) function which is also shown in Figure 15 and Figure 16 which automatically controls the DC offset compensation DAC eliminating the latency effect caused by I²C configuration of an external host MCU.

7.4.1 PPG signal processing overview

As indicated in the previous chapters and drawings, AS7150 supports various different post-processing options. An overview of all options and a device signal flow is shown in Figure 17. Please note that the processing options shown in Figure 17 are for ADC1 and ADC2 the same. The output of each modulator is connected to the SINC filter block which acts as down sampling filter. It is possible to select between 4th and 5th filter order via register **SEQ1_SEL_ORDER** and **SEQ2_SEL_ORDER** as well as decimation rates between 16, 32, 64, 128 and 256 via register **SEQ1_SINC_DEC** and **SEQ2_SINC_DEC**. In order to further improve SNR of the system there is an oversampling filter function, which is part of the down sampling filter, that can be enabled via registers **SEQ1_SINC_OVS** and **SEQ2_SINC_OVS** for both sequencers. The three-bit register allows for 7 different oversampling filter ratios to be enabled from factor 2 up to 128. The oversampling filter function is in default configuration disabled. Please mind that with enabled oversampling filter function the active ADC modulator time is increased resulting in higher power consumption with the benefit of better noise behavior. Once the signal passed the SINC decimation and optional oversampling filter the signal is feed into a scaling block which converts the signal into 20-bit unsigned signal. The last processing block, before that data is written to the FIFO memory, is a simple post-processing block. It enables the detection of modulator saturation and manipulation of the saturated data with fixed values. This function can be enabled via register **ASAT_ON**.

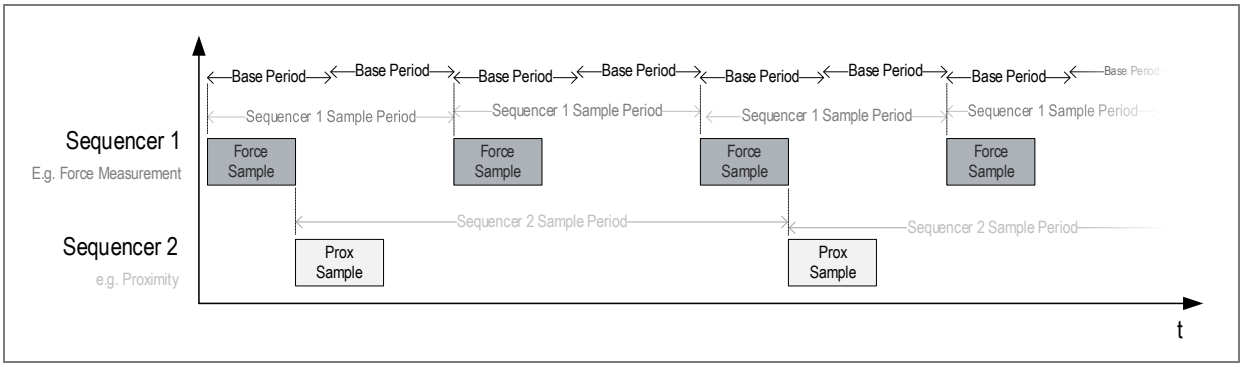
Figure 17: PPG signal processing overview



7.5 PPG sequencer

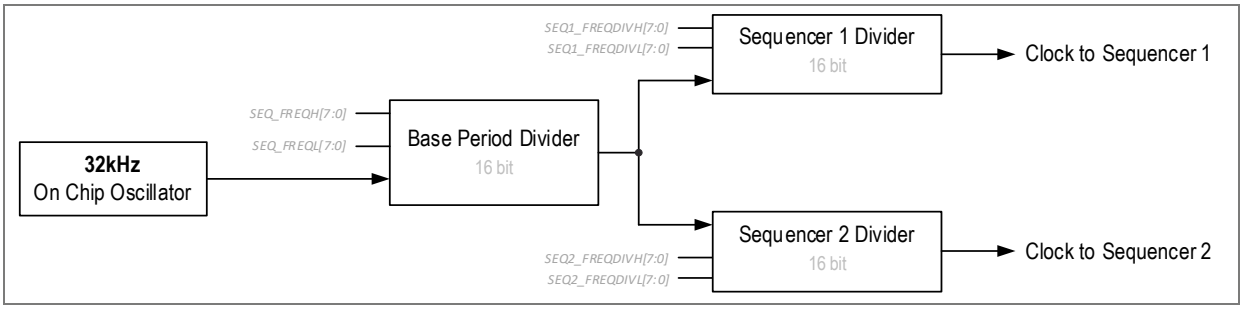
In order to unload MCU with reoccurring measurement tasks to be triggered and its related timing constraints, AS7150 has a built-in measurement sequencer which controls all relevant blocks with its corresponding timings. An overview of the sequencer timing diagram is shown in Figure 18.

Figure 18: Sequencer timing diagram



The sequencer basically supports three different sample frequencies which can be configured independently from each other. All timings for the sequencer are derived from the on-chip 32 kHz oscillator. The output of the 32kHz oscillator is fed into a first 16-bit base period divider which can be configured with two 8-bit registers **SEQ_FREQH** and **SEQ_FREQL**. The output of the base period divider acts as input clock for the sequencer 1 divider and sequencer 2 divider. The presence of two sequencer clock dividers allows for two different sample rates for Sequencer 1 and Sequencer 2 addressing the different needs depending on the selected measurement task. In a typical application sequencer 1 would run an optical force measurement at a given sample rate of typ. 25Hz and sequencer 2 could run the proximity measurement at a much lower sample rate of e.g. 10Hz. The frequency divider register for Sequencer 1 is controlled via register **SEQ1_FREQDIVH** and **SEQ1_FREQDIVL.** The corresponding control registers for Sequencer 2 are **SEQ2_FREQDIVH** and **SEQ2_FREQDIVL**.

Figure 19: Sequencer clock generation

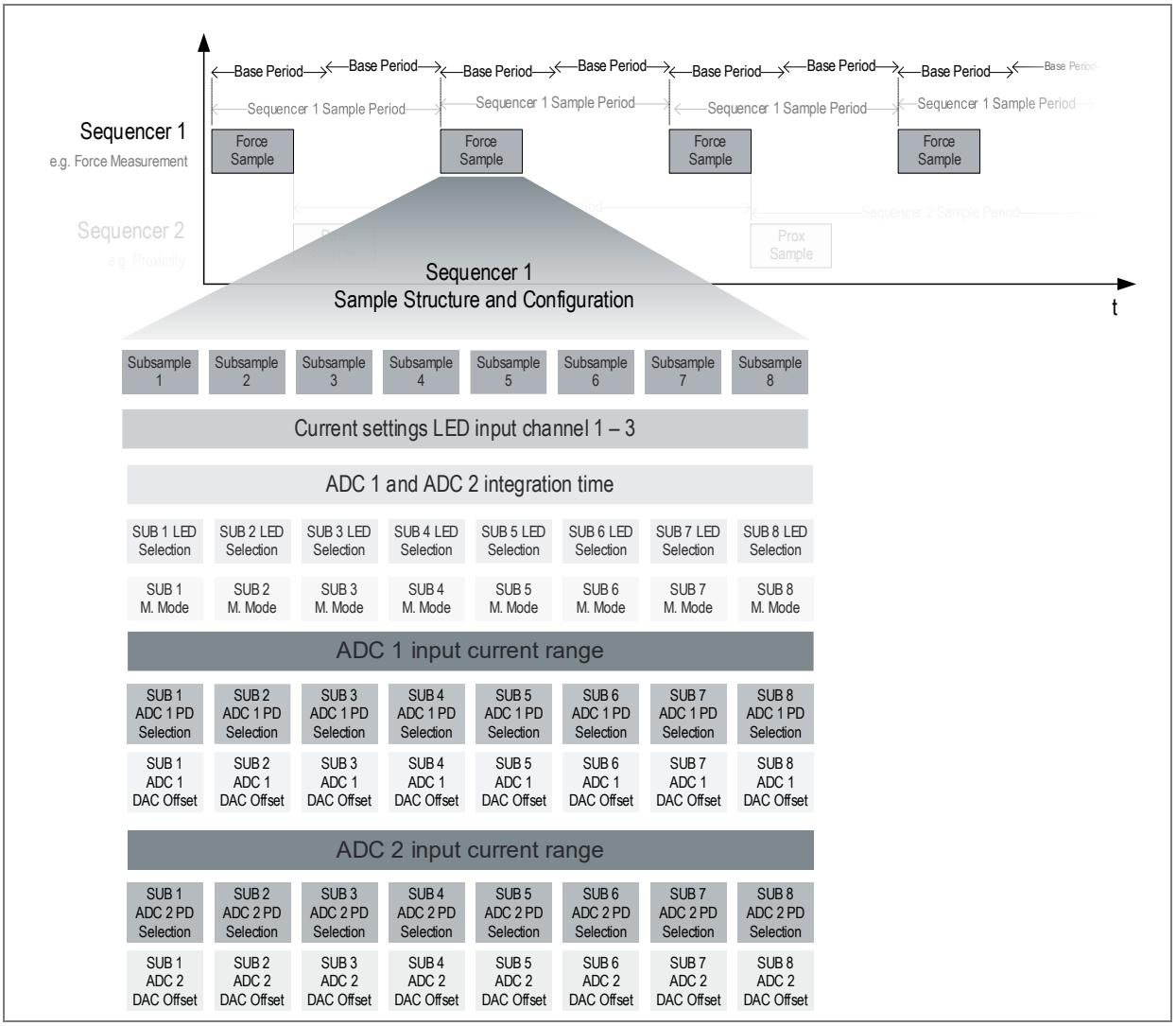


7.6 PPG sample structure

7.6.1 Sequencer 1

The AS7150 offers high flexibility in programming different measurement combinations for the photodiode and LED pins. Sequencer 1, typically used for optical force measurements, divides a measurement into samples according to the programmed Sample Period time like it is shown in Figure 18. Each sample can be divided into a maximum of eight Subsamples, which allow for individual configuration. An overview of the configuration options for a sample of Sequencer 1 is shown in Figure 20. There are general settings and like which LED is assigned to which LED input channel which are the same for each subsample. The LED input channel current settings can be configured with **SEQ1_LED1_CURR**, **SEQ1_LED2_CURR** and **SEQ1_LED3_CURR** along with the LED assignments for each subsample in **LED_SEQ1_SUBx** registers. The measurement mode itself which can be also configured for each subsample individually is defined for Sequencer 1 in register **SEQ1_MODE_A** and **SEQ1_MODE_B** register. The integration time is also for both ADCs the same and is controlled via register **SEQ1_SEL_ORDER** as well as decimation rates between 16, 32, 64, 128 and 256 via register **SEQ1_SINC_DEC**. To maintain best dynamic range and noise behavior it is also important that the current range for ADC1 and ADC2 is configured accordingly. Each ADC signal path supports seven full-scale range settings of 1µA, 2µA, 4µA, 8µA, 16µA, 32µA, and 64µA which can be configured in register **MOD1_SEQ1_IREF** and **MOD2_SEQ1_IREF** for sequencer 1. Individual configurations for each ADC are the photodiode assignments via register **PD_SEQ1_SUBx** as well as the offset DAC currents for ambient light rejection which can be configured via **AOC_MOD1_SEQ1_SUBx** and **AOC_MOD2_SEQ1_SUBx** registers.

Figure 20: Sequencer 1 sample structure and configuration options



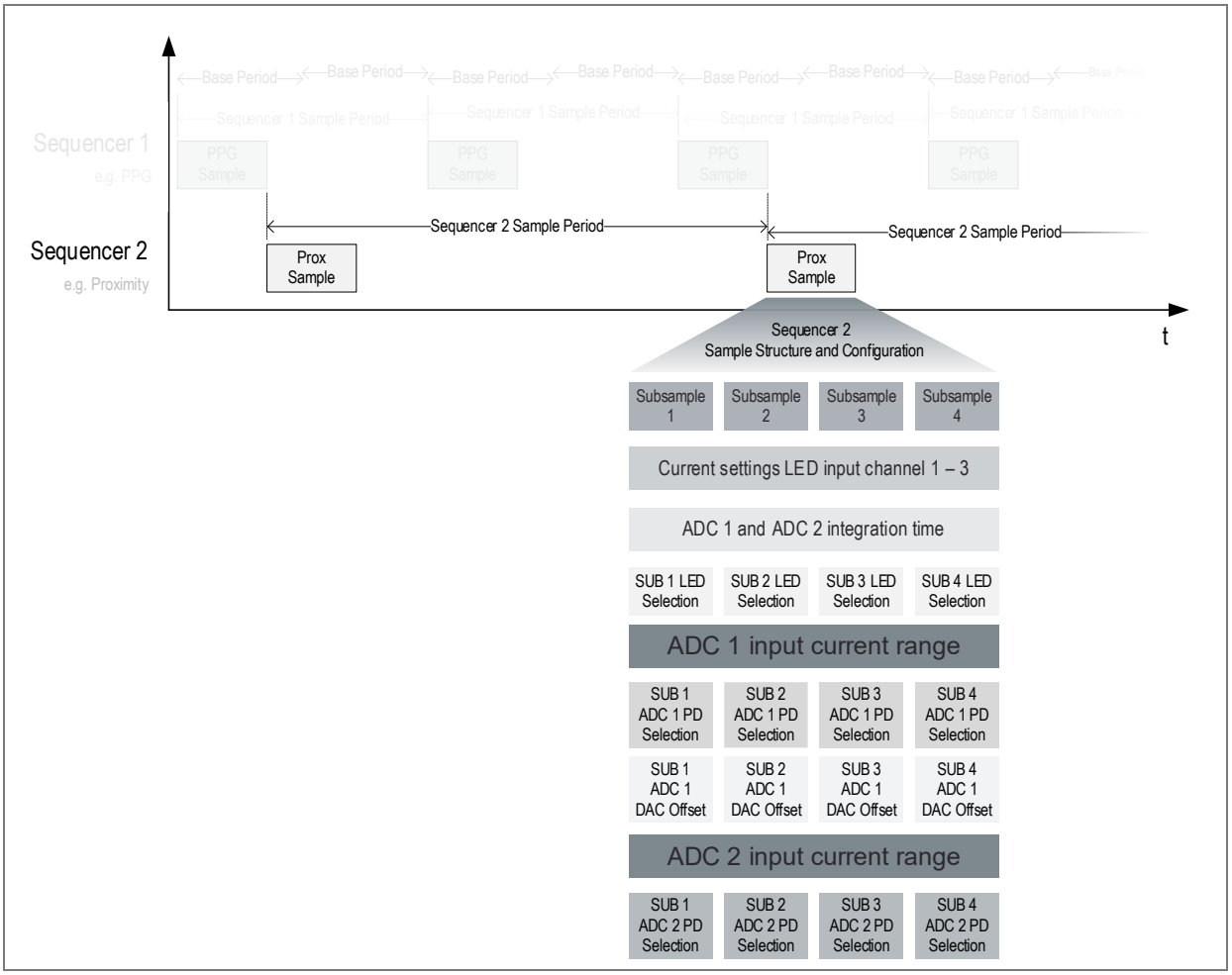
7.6.2 Sequencer 2

Sequencer 2, typically used for proximity and temperature measurements, divides measurements into samples according to the programmed Sequencer 2 Sample Period time like it is shown in Figure 18. Each sample can be divided into a maximum of four Subsamples, which allow for individual configuration. An overview of the configuration options for a sample of Sequencer 2 is shown in Figure 21. There are general settings and like which LED is assigned to which LED input channel which are the same for each subsample.

The LED input channel current settings can be configured with **SEQ2_LED1_CURR**, **SEQ2_LED2_CURR** and **SEQ2_LED3_CURR** along with the LED assignments for each subsample in **LED_SEQ2_SUBx** registers.

The integration time is also for both ADCs the same and is controlled via register **SEQ2_SEL_ORDER** as well as decimation rates between 16, 32, 64, 128 and 256 via register **SEQ2_SINC_DEC**. To maintain best dynamic range and noise behavior it is also important that the current range for ADC1 and ADC2 is configured accordingly. Each ADC signal path supports seven full-scale range settings of 1µA, 2µA, 4µA, 8µA, 16µA, 32µA, and 64µA which can be configured in register **MOD1_SEQ2_IREF** and **MOD2_SEQ2_IREF** for sequencer 2. Individual configurations for both ADCs are the photodiode assignments via register **PD_SEQ2_SUBx** as well as the offset DAC currents for ambient light rejection which can be configured via **AOC_MOD1_SEQ2_SUBx** registers.

Figure 21: Sequencer 2 sample structure and configuration options



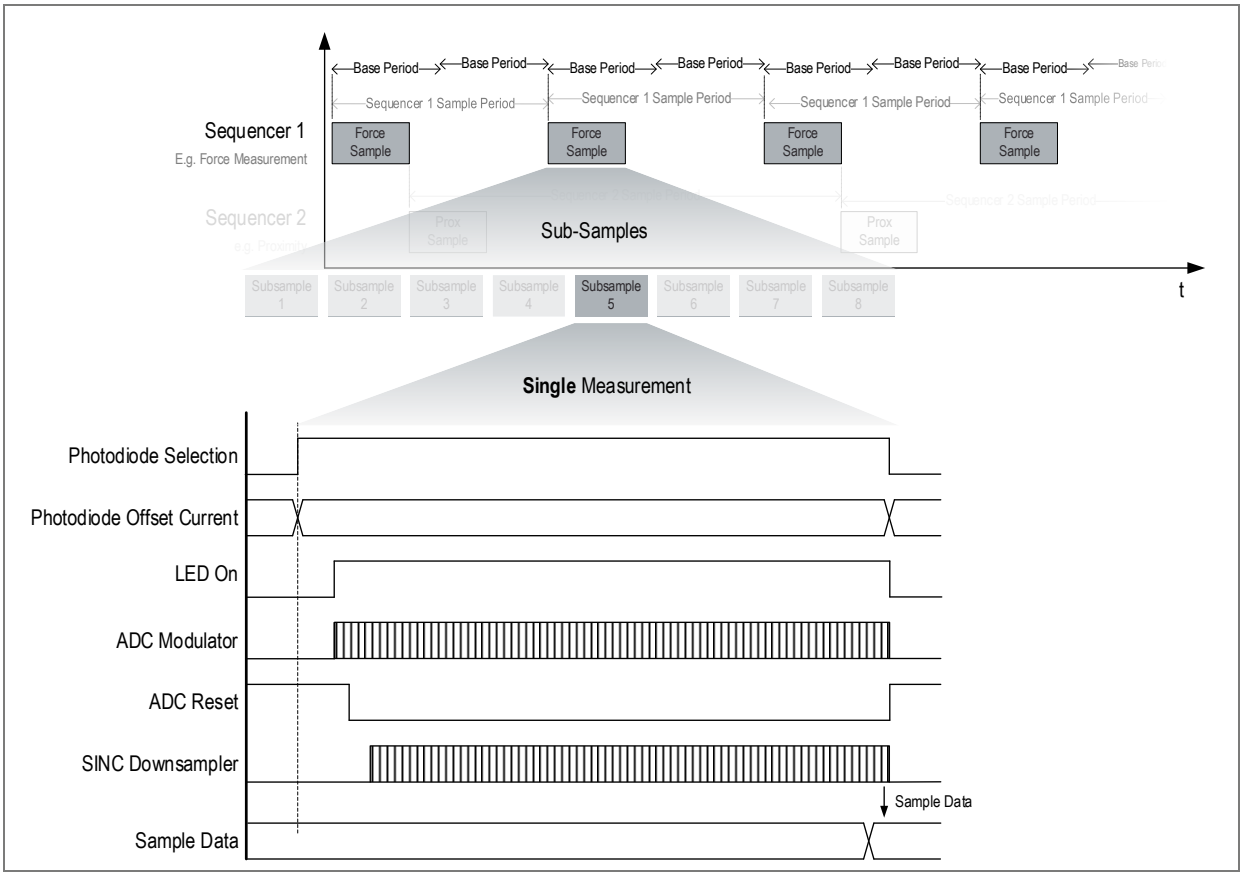
7.6.3 Measurement modes

AS7150 basic measurement mode is the Single Measurement Mode which does not support any kind of ambient light compensation. If ambient light compensation measurement modes are desired, please refer to chapter 7.6.4 Ambient light compensation. However, it's worth mentioning that all measurement modes for ambient light compensation do rely on the basic principle and timing of the Single Measurement mode which is described in this chapter and illustrated in Figure 22.

7.6.3.1 Single measurement mode

The Single Measurement mode is the simplest measurement which can be selected and assigned to a subsample. A timing diagram to explain the operation mode and working principle of the Single Measurement is shown in Figure 22. Once a Single measurement is executed, the first step in the measurement procedure is that the assigned photodiode is connected via the internal multiplexers to the selected ADC channel. At the same time a DAC offset current, which is setup in **AOC_MOD1_SEQ1_SUBx** and **AOC_MOD2_SEQ1_SUBx register**, is applied to the summing node of the selected ADC and the photodiode input. After a short delay, which can be configured as part of the chip configuration, the LEDs with the configured LED currents in registers **SEQ1_LED1_CURR**, **SEQ1_LED2_CURR** and **SEQ1_LED3_CURR** are enabled for the measurement and in parallel, the ADC is started. After a configurable modulator reset time, the SINC down-sampler filter is fed with data. The measurement time depends now very much on the configuration of the SINC filter, filter order and internal clock speed of AS7150. These parameters are typically configured with **SEQ1_MODE_A, SEQ1_MODE_B**, **SEQ1_SEL_ORDER** and **SEQ1_SINC_DEC** register for both modulators. Once the measurement time has elapsed the sample data is written to the FIFO memory and ready for readout by a host MCU. Please refer to chapter 7.6.5 Parameters for more detailed timing diagrams and timing characteristics.

Figure 22: Single measurement mode – simplified timing diagram



7.6.4 Ambient light compensation

AS7150 offers up to three different options to compensate for ambient light influences while a measurement is ongoing. This chapter provides a detailed description of Double Measurement, Tripple Measurement and the Advanced Automatic Offset Compensation (AAOC).

7.6.4.1 Double sampling

The double sampling function measures two values within a subsample. The first measurement is the same like a single measurement with the LED enabled and the configured offset current is applied to the ADC input channel. The sample data is stored temporarily in the memory. The second part of the measurement is done with the LED disabled which represents an ambient light measurement. The difference between the first measurement and the ambient light measurement is stored in the FIFO memory.

Equation 6:

$$C_{DOUBLE} = C_{LED_{ON}} - C_{LED_{OFF}}$$

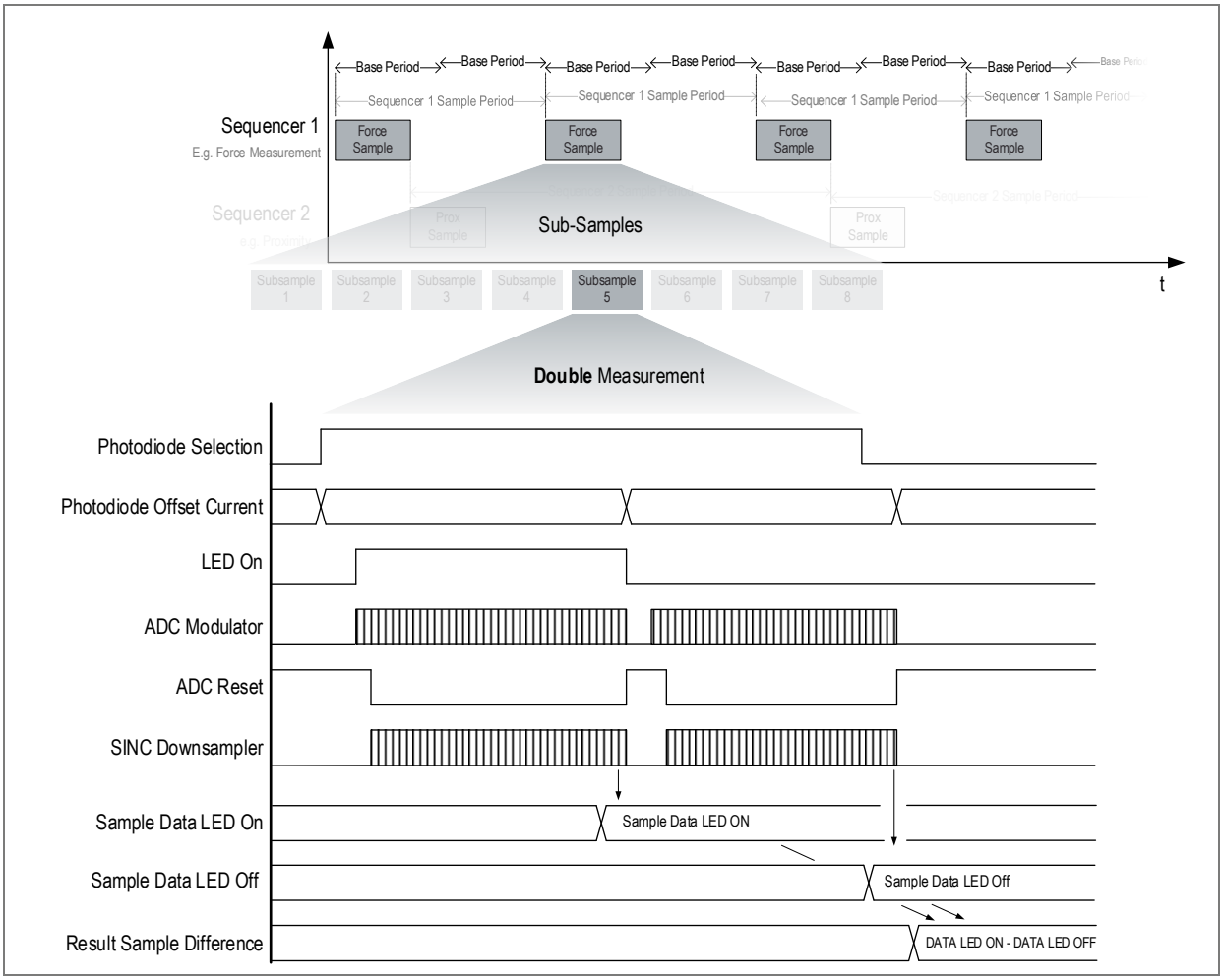
C_{DOUBLE} ... $Tripple\ Measurement\ result\ stored\ to\ FIFO$

$C_{LED_{ON}}$ ... $ADC\ count\ value\ during\ LED\ on\ phase$

$C_{LED_{OFF}}$ ... $ADC\ count\ values\ during\ LED\ off\ phase$

The assignment of the photodiodes is for both measurements the same. The programmed DAC offset current is used for the first measurement and can also be used for the second measurement (**DIS_LEDOFF** = 1). Alternatively, it is possible to use also a different value, which is stored to **AOS_LEDOFF** register, for all subsamples if register **DIS_LEDOFF** bit is cleared.

Figure 23: Double measurement mode – simplified timing diagram



7.6.4.2 Tripple sampling

The Tripple Measurement function measures three different values within a subsample. The first measurement is an ambient light measurement with the LED disabled. The result of this sampling is stored temporarily to the device. The ambient light measurement is followed then by a measurement where the LED is enabled with the predefined LED current. Its measurement result is again stored temporarily to the device memory. The last part of a Tripple Measurement is again an ambient light measurement where the LEDs are disabled. Its result is also stored temporarily to the device memory and used for the calculation for the final measurement value which is stored to the FIFO memory. The calculation of the value stored to the FIFO memory is shown in Equation 7.

Equation 7:

$$C_{TRIPPLE} = C_{LED_{ON}} - \frac{C_{LED_{OFF_1}}}{2} - \frac{C_{LED_{OFF_2}}}{2}$$

$C_{TRIPPLE}$ ... $FIFO\ Tripple\ Measurement\ result$

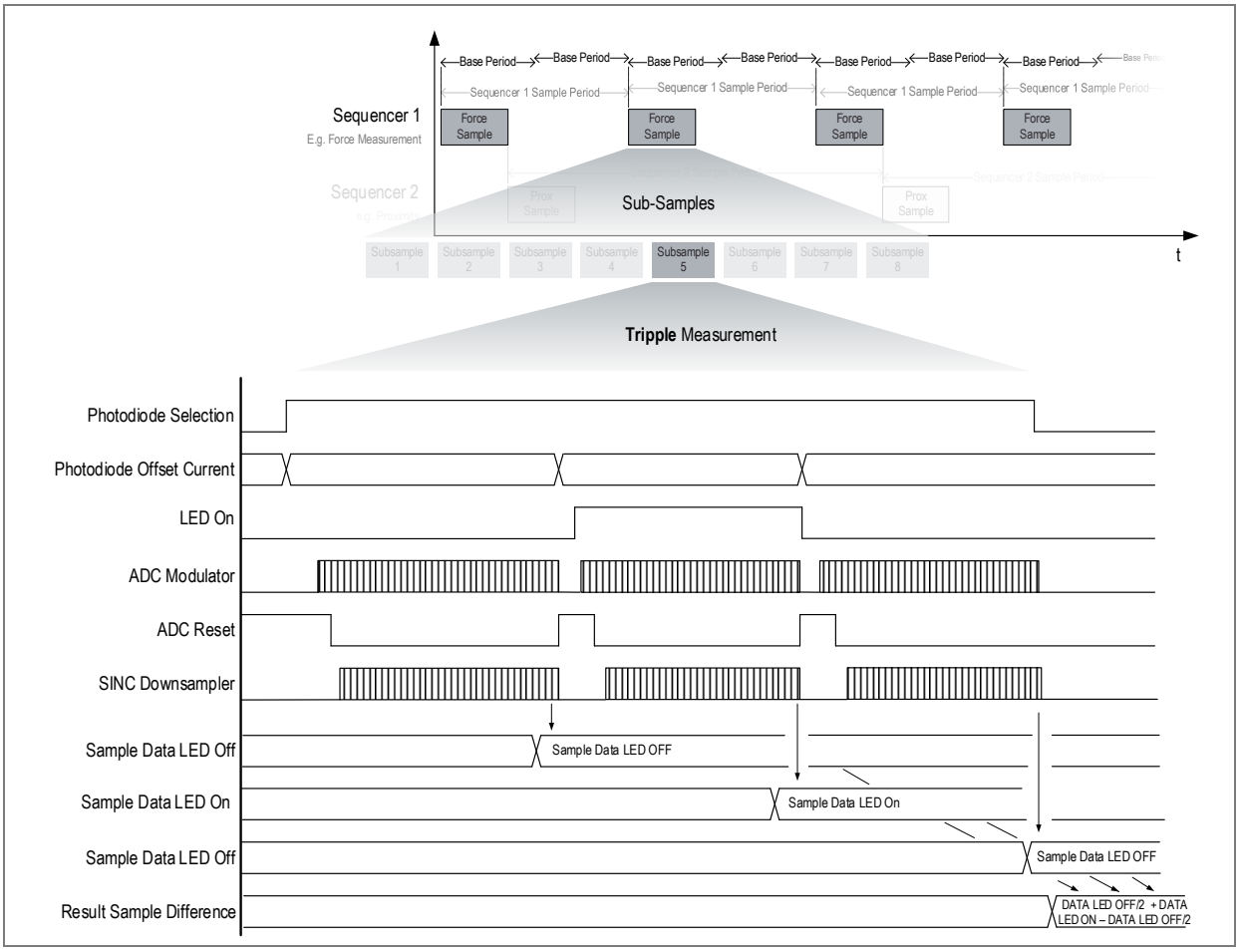
$C_{LED_{ON}}$ ... $ADC\ count\ value\ during\ LED\ on\ phase$

$C_{LED_{OFF1}}$ ... $ADC\ count\ values\ during\ first\ LED\ off\ phase$

$C_{LED_{OFF2}}$ ... $ADC\ count\ values\ during\ second\ LED\ off\ phase$

The assignment of the photodiodes is for all three measurements the same. The programmed DAC offset current is used for the second measurement but can also be used for the first and third measurement (**DIS_LEDOFF** = 1). Alternatively, it is possible to use also a different value during the LED off measurement phases which is stored to **AOS_LEDOFF** register if register **DIS_LEDOFF** bit is cleared

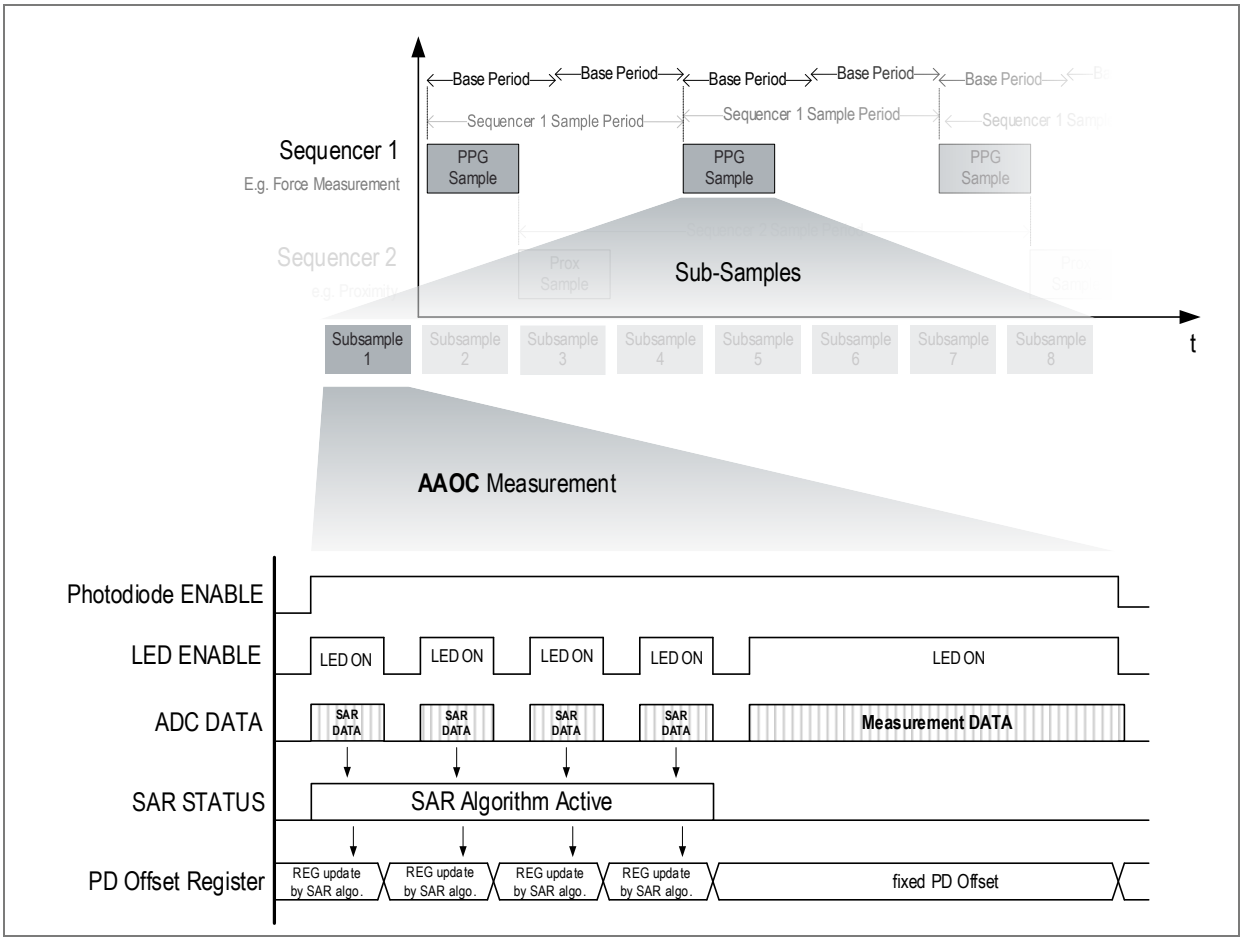
Figure 24: Tripple measurement mode – simplified timing diagram



7.6.4.3 Automatic offset compensation (AOC)

The built in AOC is an advanced ambient light compensation solution which does not require an external host to adjust the DAC offset current. In conventional approach with Double Measurement and Tripple Measurement the DAC offset current registers need to be controlled and adjusted by a host MCU via I²C interface. This approach might require several measurement iterations until an appropriate offset value is found. The AOC function eliminates the need for MCU interaction to find the correct photodiode offset current. It is based on a successive approximation approach to determine the upper 4 bits of the photodiode offset register. In order to achieve this and adjust the 4 bits accordingly AS7150 does four short measurements prior to the actual force measurement like it is shown in Figure 25. During each pre-measurement cycle the LED is also switched on and the ADC data read is feed into the SAR algorithm which adjusts the photodiode current. Once all four pre-measurements are done the offset current is adjusted correctly to avoid saturation of the ADC due to ambient light. The upper 4 bits of **AOC_MODx_SEQx_SUBx** registers are determined automatically with the first four samplings, the lower 4 bits correspond to the programmable bits. The FIFO stores the AOC data and the ADC results to simplify signal reconstruction for algorithm developers. The programmed current values for the LEDs are used for all five measurements. The assignment of the photodiodes is also fixed for all 5 measurements.

Figure 25: AAOC – simplified timing diagram



The AOC is only available in Sequencer 1 and can be activated for subsamples 1 to 8 for ADC1 and subsamples 1 and 2 in Sequencer 1 for PPG MOD2. Subsamples 1 to 4 in Sequence2 for PPG MOD1 and subsamples 3 to 8 in Sequence1 for PPG MOD2 only work with the manual programmable PD offset value. Subsamples 1 to 4 in sequence 2 for PPG MOD2 are intended for the Analog Frontend and do not have a programmable PD offset value. The PD offset registers can be overwritten if the AOC is active and take effect immediately. There are no shadow registers. The control of the AOC continues as usual.

7.6.5 Parameters

This chapter contains the detailed timing diagrams and parameters for the PPG samples.

Figure 26: Single measurement timing diagram

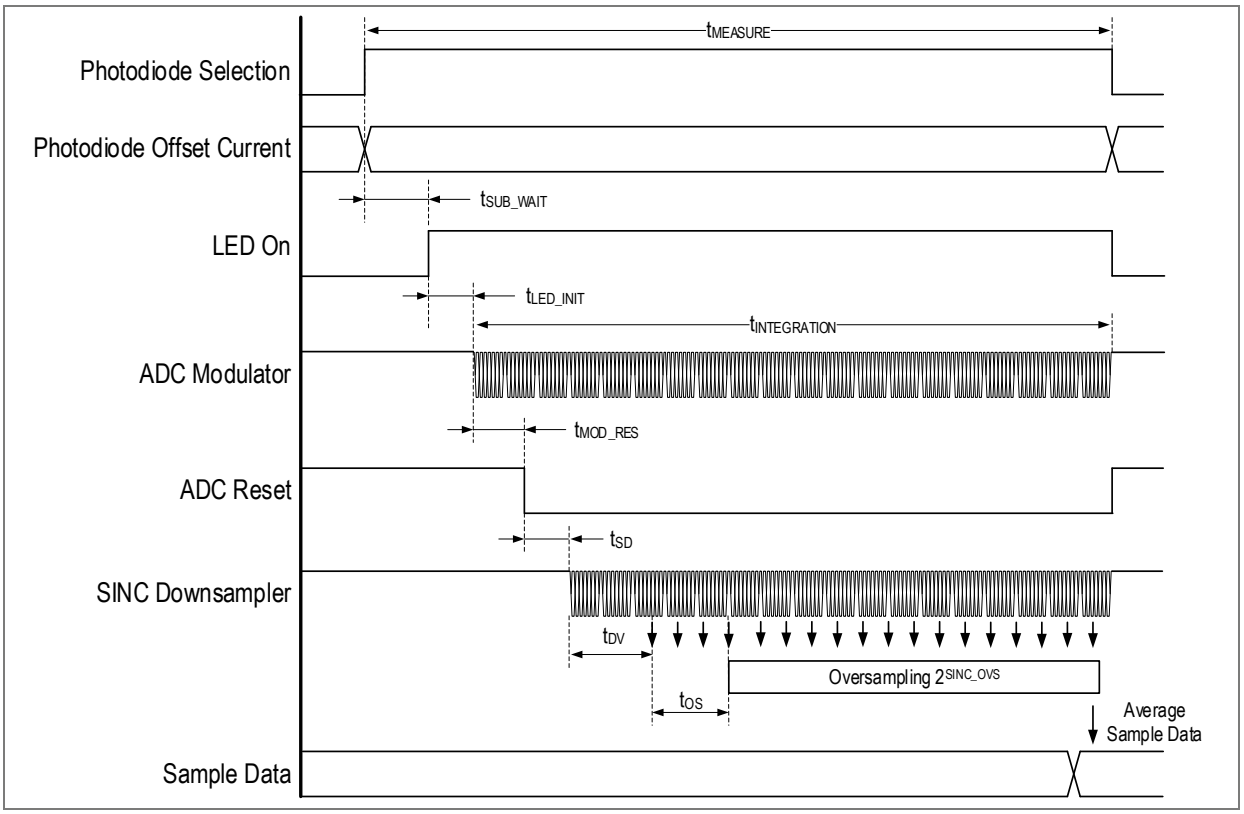


Figure 27: Double measurement timing diagram

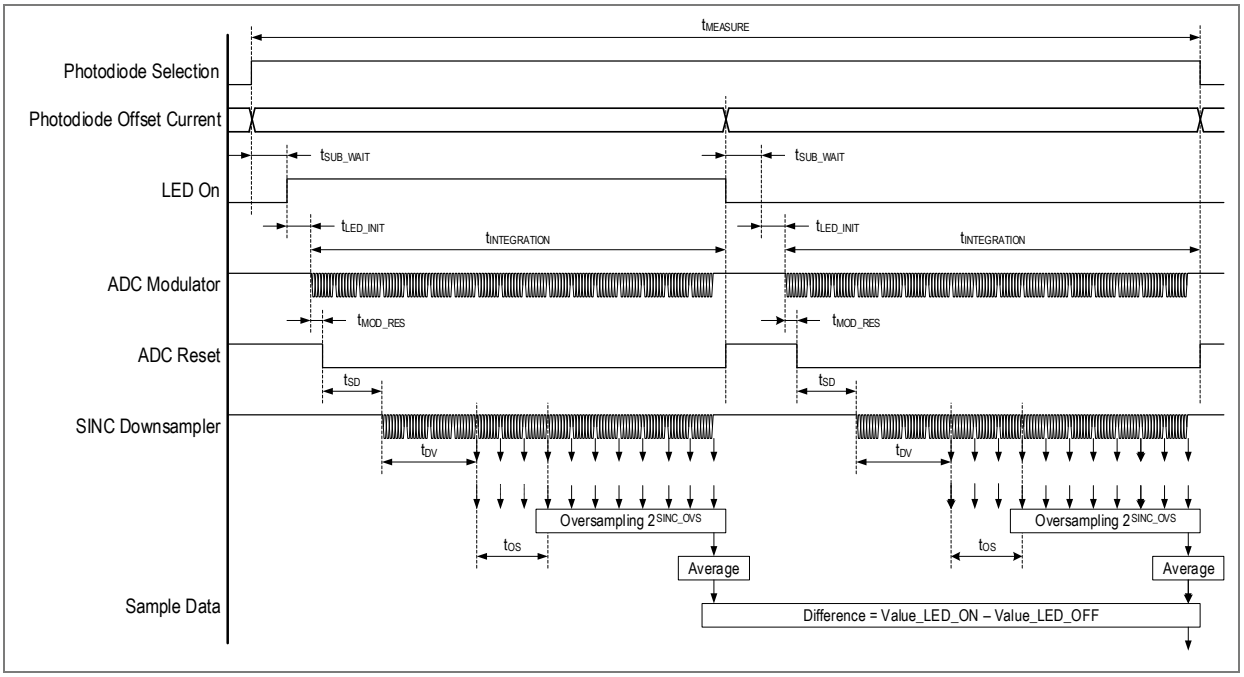


Figure 28: Tripple measurement timing diagram

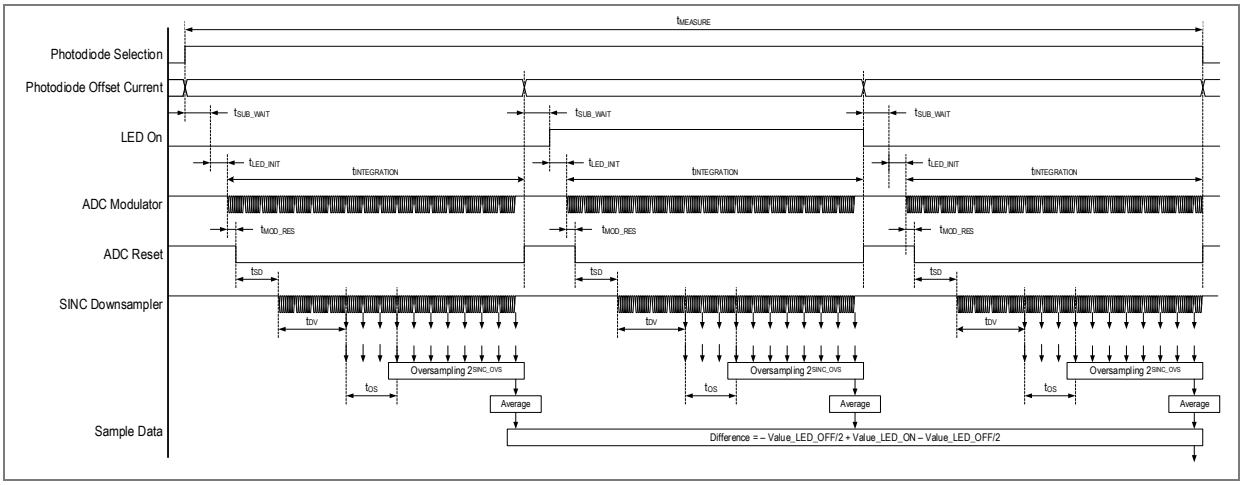


Figure 29: AAOC timing diagram

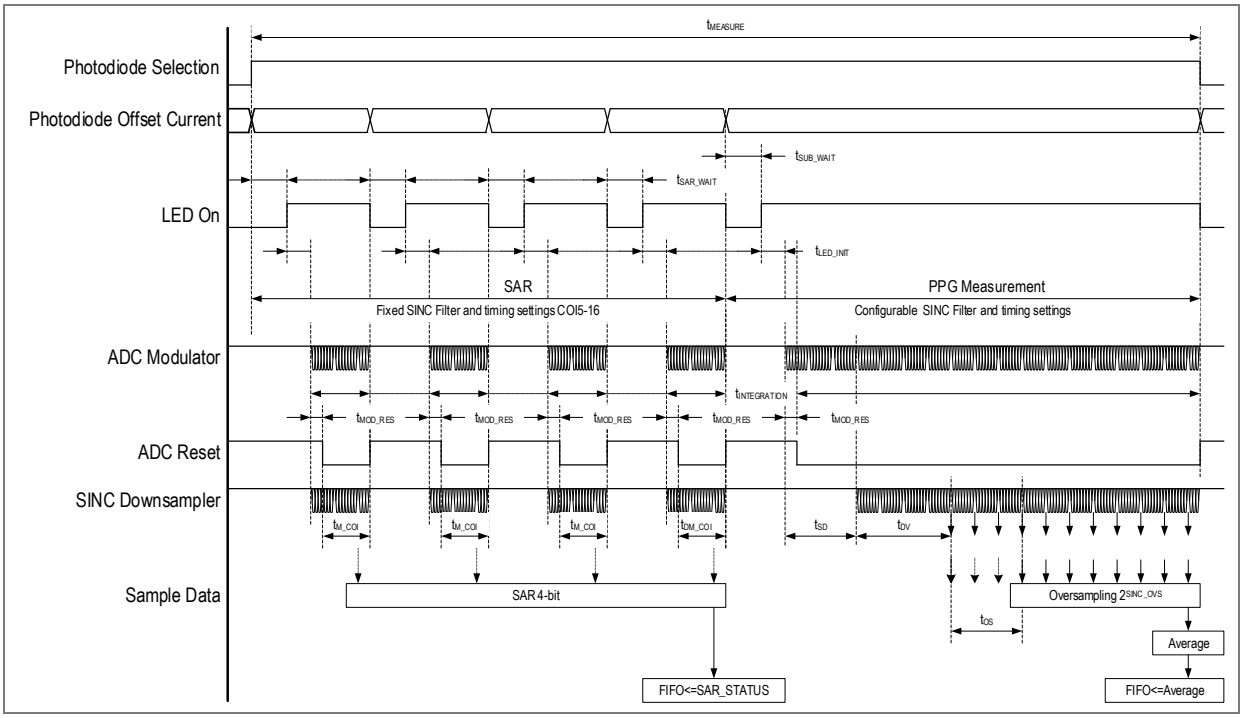


Table 7: Timing parameter measurement modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SUB_WAIT}	Subsample Wait time	Parameter controlled via *sub_wait* register	0		255	µs
t_{LED_INIT}	LED Initialization time	Parameter controlled via *led_init* register	0		255	µs
t_{MOD_RES}	ADC modulator reset time	Parameter controlled via *mod_reset_delay* register; *mod_clk* = 0;	0.4		25.5	µs
t_{SD}	SINC downsampler Start delay	Parameter controlled via *seq1_start_delay* and *seq2_start_delay* register; *mod_clk*=0;	0		240	µs
t_{SAR_WAIT}	AAOC SAR wait time	Parameter controlled via *sar_wait* register	0		255	µs
t_{M_COI}	SAR modulator on time	*ppgmod_clk=0*		2.7		µs
		ppgmod_clk=1		5.4		µs
		ppgmod_clk=2		10.8		µs
		ppgmod_clk=3		21.6		µs

The integration time $t_{INTEGRATION}$ is influenced by many parameters like modulator clock, filter order and decimation filter setting. Table 8, Table 9 and Table 10 provides example register configurations with the resulting integration times depending on decimation rates, oversampling and filter order. In case additional information about different register settings are required please do consult your local ams OSRAM support team for assistance.

Table 8: Integration times $t_{INTEGRATION}$ CIC filter operation mode filter order 5(1)

	Decimation filter order 5 (*seqX_sel_order* = 1)				
	Decimation filter oversampling factor				
Decimation rate	**0** *seqX_sinc_ovs* = 0	**2** *seqX_sinc_ovs* = 1	**4** *seqX_sinc_ovs* = 2	**8** *seqX_sinc_ovs* = 3	**16** *seqX_sinc_ovs* = 4
16 *seqX_sinc_dec* = 0	8.3 µs	11.5 µs	14.7 µs	21.1 µs	33.9 µs
32 *seqX_sinc_dec* = 1	16.3 µs	22.7 µs	29.1 µs	41.9 µs	67.5 µs
64 *seqX_sinc_dec* = 2	32.3 µs	45.1 µs	57.9 µs	83.5 µs	134.7 µs
128 *seqX_sinc_dec* = 3	64.3 µs	89.9 µs	115.5 µs	166.7 µs	269.1 µs
256 *seqX_sinc_dec* = 4	128.3 µs	179.5 µs	230.7 µs	333.1 µs	537.9 µs

(1) Conditions: **SEQx_FILTER_MODE** = 1; **MODCLK** = 0; **MOD_RESET_DELAY** = 0; **SEQx_START_DELAY** = 0; **SEQx_OS_DELAY** = 0

Table 9: Integration times $t_{INTEGRATION}$ CIC filter operation mode filter order 4(1)

	Decimation filter order 4 (*seqX_sel_order* = 0)				
	Decimation filter oversampling factor				
Decimation rate	**0** *seqX_sinc_ovs* = 0	**2** *seqX_sinc_ovs* = 1	**4** *seqX_sinc_ovs* = 2	**8** *seqX_sinc_ovs* = 3	**16** *seqX_sinc_ovs* = 4
16 *seqX_sinc_dec* = 0	6.7 µs	9.9 µs	13.1 µs	19.5 µs	32.3 µs
32 *seqX_sinc_dec* = 1	13.1 µs	19.5 µs	25.9 µs	38.7 µs	64.3 µs
64 *seqX_sinc_dec* = 2	25.9 µs	38.7 µs	51.5 µs	77.1 µs	128.3 µs
128 *seqX_sinc_dec* = 3	51.5 µs	77.1 µs	102.7 µs	153.9 µs	256.3 µs
256 *seqX_sinc_dec* = 4	102.7 µs	153.9 µs	205.1 µs	307.5 µs	512.3 µs

(1) Conditions: **SEQx_FILTER_MODE** = 1; **MODCLK** = 0; MOD_**RESET_DELAY** = 0; **SEQx_START_DELAY** = 0; **SEQx_OS_DELAY** = 0

Table 10: Integration times $t_{INTEGRATION}$ with integrator filter operation mode(1)

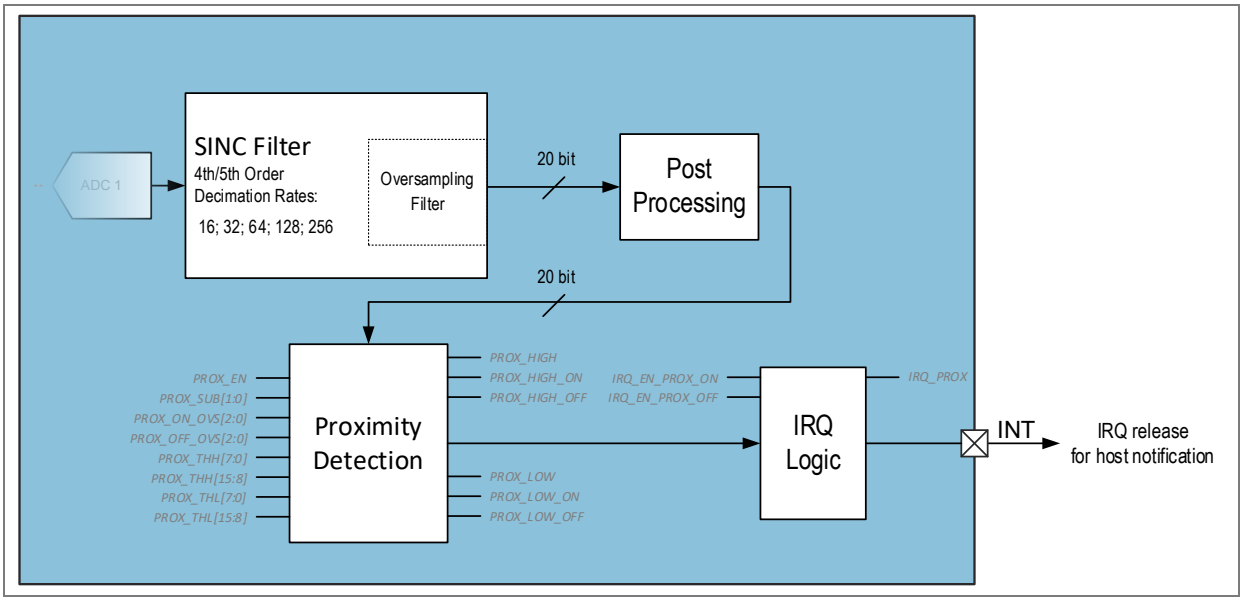
Decimation rate	**Decimation filter order 4** (*seqX_sel_order* = 0)	**Decimation filter order 5** (*seqX_sel_order* = 1)
16 *seqX_sinc_dec* = 0	2.3 µs	2.4 µs
32 *seqX_sinc_dec* = 1	3.9 µs	4 µs
64 *seqX_sinc_dec* = 2	7.1 µs	7.2 µs
128 *seqX_sinc_dec* = 3	13.5 µs	13.6 µs
256 *seqX_sinc_dec* = 4	26.3 µs	26.4 µs

(1) Conditions: **SEQx_FILTER_MODE** = 0; **MODCLK** = 0; **MOD_RESET_DELAY** = 0; **SEQx_START_DELAY** = 0

7.7 Proximity detection

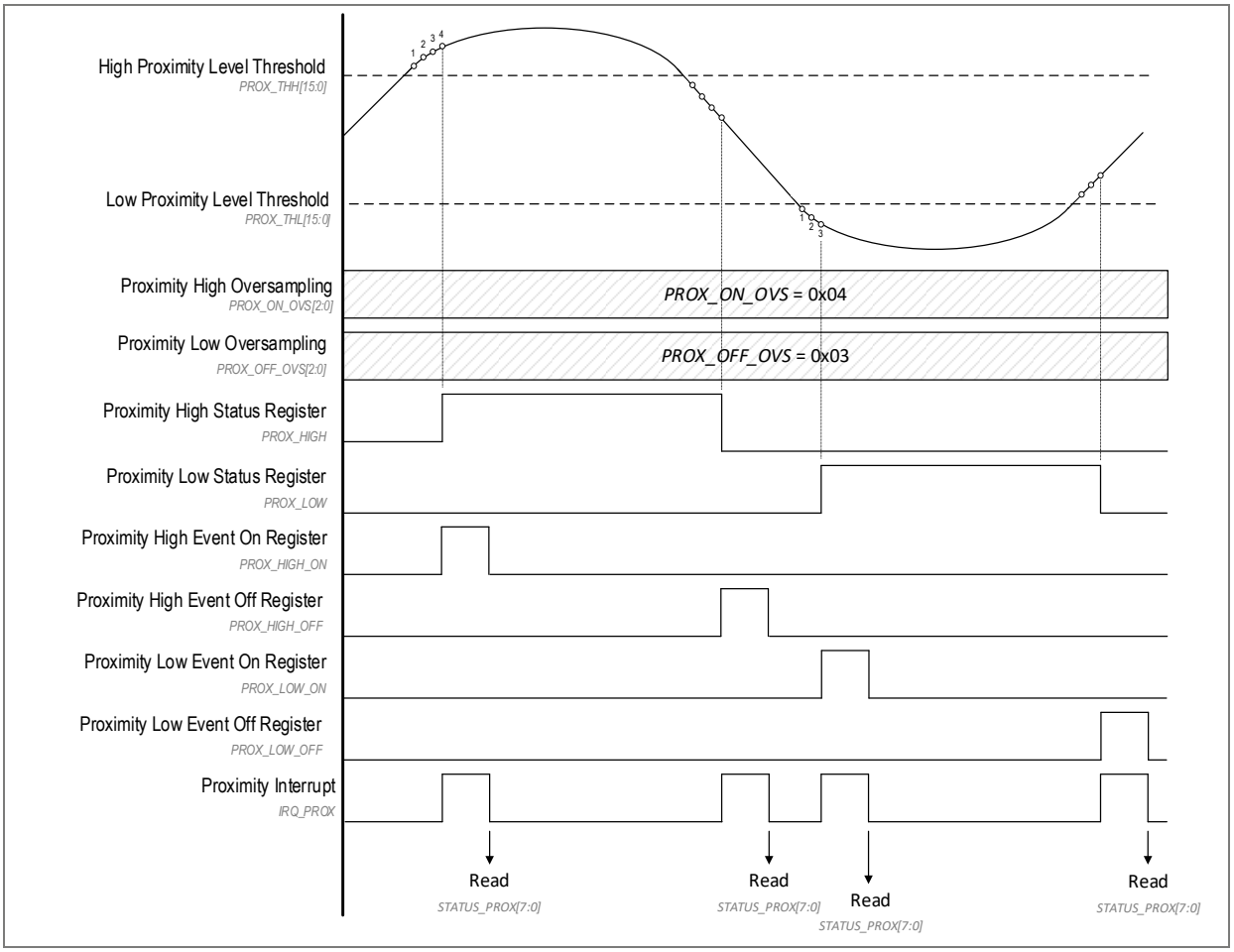
The AS7150 features an integrated proximity detection function. The feature can be enabled via register **PROX_EN** bit. The function is typically assigned to sequencer two to run independently of an ongoing force measurement like it is shown in the example timing diagram in Figure 18. The function is linked exclusively to ADC1 with the freedom to assign it to any of the four subsamples of sequencer two via register **PROX_SUB**. In order to avoid false detections and oversampling function which can be configured via register **PROX_ON_OVS** and **PROX_OFF_OVS** is also part of the system. The decision if a proximity event is triggered is configured with dedicated high and low threshold registers **PROX_THH_L**, **PROX_THH_H**, **PROX_THL_L**, **PROX_THL_H**. In order to avoid MCU polling of the registers AS7150 supports also an interrupt function in case a proximity events occurs which can be enabled for the detection and release event via registers **IRQ_EN_PROX_ON** and **IRQ_EN_PROX_OFF**. Once an interrupt event occurs the **IRQ_PROX** bit is set. Once the bit is set the host MCU can read the related proximity status register **STATUS_PROX** to find out what kind of event happened.

Figure 30: Proximity detection processing block diagram



A timing diagram which shows all relevant control signals and register names is shown in Figure 31. The timing diagram shows also to oversampling function which is enabled via **PROX_ON_OVS** and **PROX_OFF_OVS** register. In the example the ADC reading for the high proximity level needs to be 4 times above the high proximity threshold level before and interrupt is released and the related proximity bits are set tin the **STATUS_PROX** register.

Figure 31: Proximity detection timing diagram

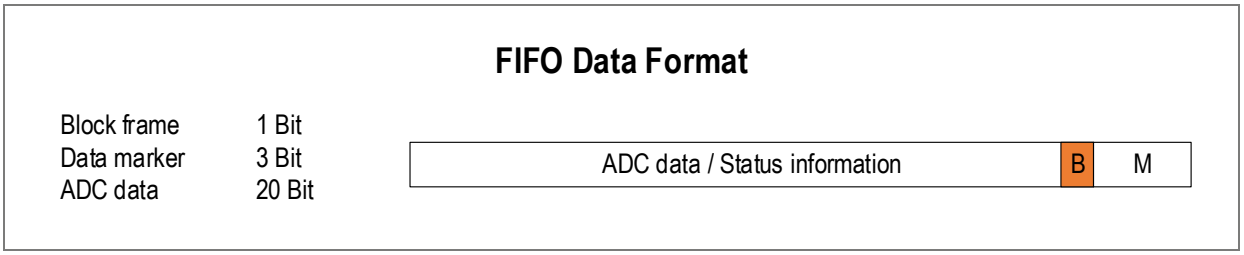


7.8 FIFO register

The AS7150 provides a 1.5 kB FIFO register for buffering the measurement data output to an external microcontroller via the I²C interface. The FIFO buffering allows the external MCU to stay in idle mode during energy-saving measurements.

The measurement data of the two channels after oversampling and possible status information from the AOC will be collected in a common data stream and written to the FIFO.

Figure 32: FIFO data format



Data marker (3 bits)

- 000 – First ADC data Sequencer 1 Modulator1
- 001 – First ADC data Sequencer 2 Modulator1
- 010 – Other ADC data Modulator1
- 011 – First ADC data Sequencer 1 Modulator2
- 100 – First ADC data Sequencer 2 Modulator2
- 101 – Other ADC data Modulator 2
- 110 – SAR Status
- 111 – AOC Status

Figure 33: AOC status information

AOC Status 20 Bit

MOD1 = 4'h0	SUB8	SUB7	SUB6	SUB5	SUB4	SUB3	SUB2	SUB1
MOD2 = 4'h2	00	00	00	00	00	00	SUB2	SUB1

Change AOC value per SubSample = 2 Bit
Bit 0 = 1 – Input current from PD on the moddulator is decreased
Bit 1 = 1 – Input current from PD on modulator is increased

The following ADC values will be measured with new AOC value.

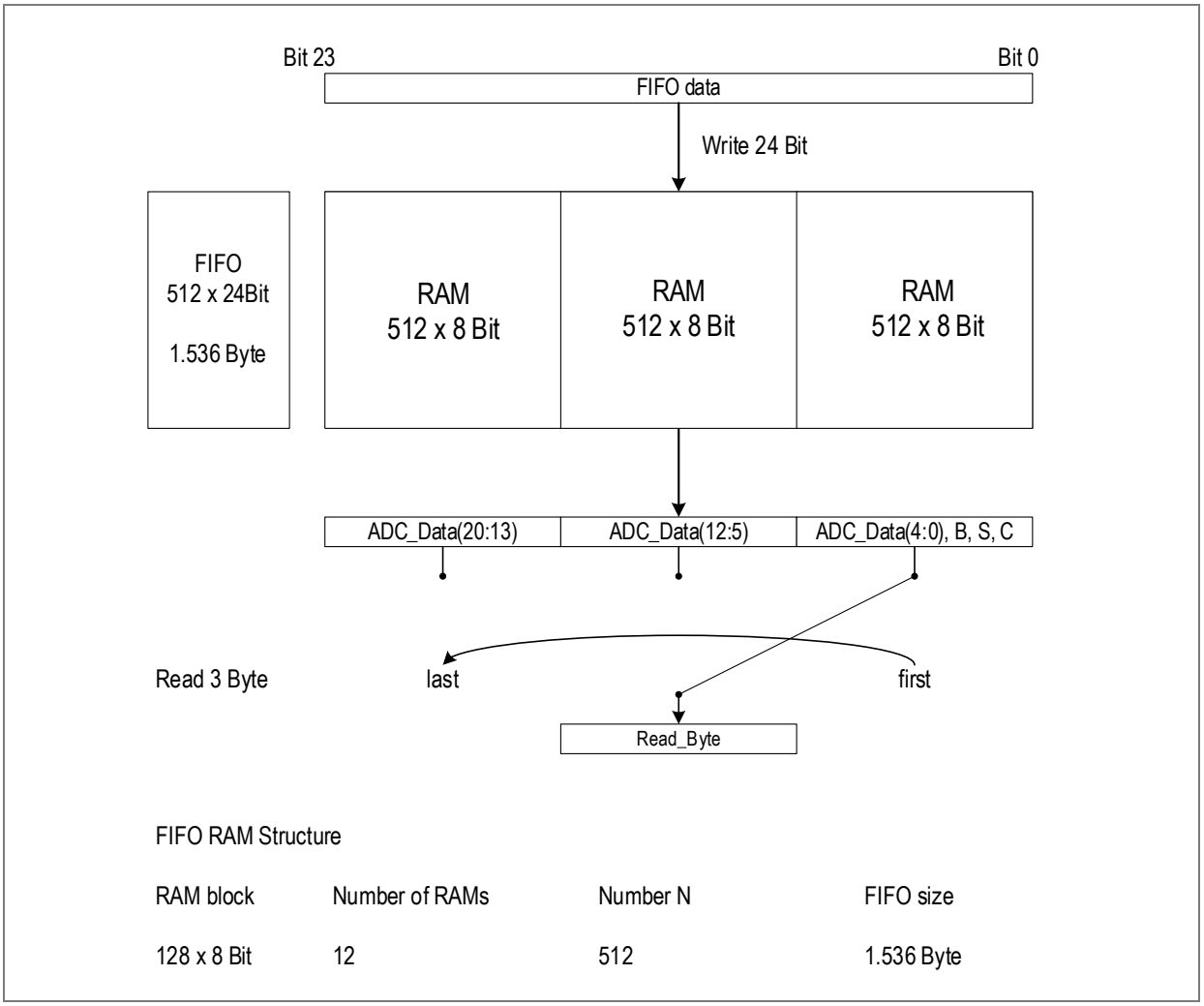
Figure 34: SAR status information

SAR Status 20 Bit

6 Bit	1 Bit	1 Bit	4 Bit	8 Bit
6'h00	MOD	SEQ	SUB	PD Offset

MOD: 0 – Modulator 1, 1 – Modulator 2
SEQ: 0 – Sequencer 1, 1– Sequencer 2
SUB: 0...7 (Seq1) – SUB Sample 1...8
0...3 (Seq2) – SUB Sample 1...4

Figure 35: FIFO data structure and organization



FIFO RAM Structure

RAM block	Number of RAMs	Number N	FIFO size
128 x 8 Bit	12	512	1.536 Byte

7.9 Communication interfaces

7.9.1 Interrupt output pin

The interrupt manager processes the interrupt events. These interrupt events must be released for processing via an interrupt enable register **IRQ_ENABLE**. The dedicated interrupt status bit is automatically reset when the corresponding sub-status register is read (auto-zero register). For the FIFO threshold reset, the FIFO must be read or cleared. In this way, no interrupt events may be lost.

7.9.2 I²C interface

The AS7150 AFE provides a digital I²C slave interface used for the external control of the measurement setup and the control of all functions for the internal features. It supports single and burst access via the I²C. Single access requires about 50% more time compared to burst access, for the transmission of the same amount of data.

The AS7150 I²C slave uses an I²C address of 0x55 (7-bit format; 1-bit R/W bit has to be added) respectively 60 h and 61 h. It expects external pull-up resistors.

I²C feature list:

- Fast mode (400 kHz) and standard mode (100 kHz) support.
- 7+1-bit addressing mode.
- Write formats: Single-Byte-Write, Burst-Write.
- Read formats: Current-Address-Read, Random-Read, Sequential-Read.
- SDA input delay and SCL spike filtering by integrated RC-components.

7.9.2.1 I²C protocol

Table 11: I²C symbol definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1-bit
Sr	Repeated start	R	1-bit
DW	Device address for write	R	0110 0000b (60 h)
DR	Device address for read	R	0110 0001b (61 h)
WA	Word address	R	8-bit
A	Acknowledge	W	1-bit
N	No Acknowledge	R	1-bit
reg_data	Register data/write	R	8-bit
data (n)	Register data/read	W	8-bit
P	Stop condition	R	1-bit
WA++	Increment word address internally	R	During acknowledge

7.9.2.2 I²C write

Byte Write and Burst Write formats are used to write data to the slave.

Figure 36: I²C byte write format

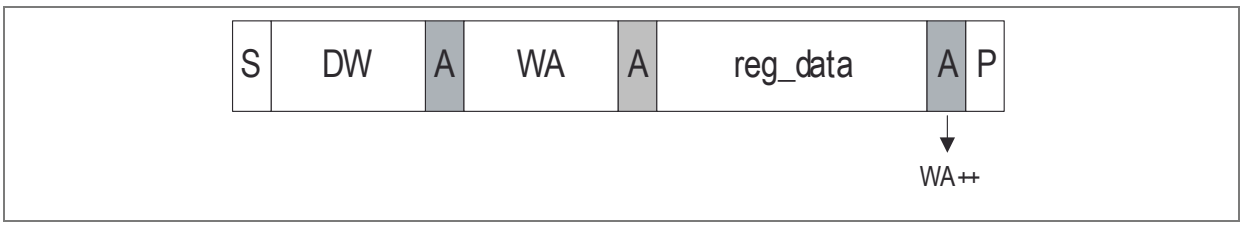
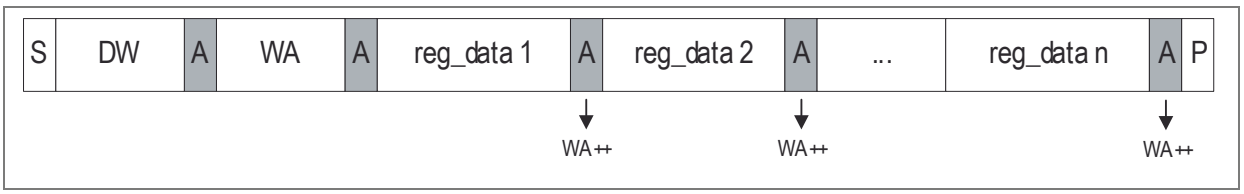


Figure 37: I²C burst write format

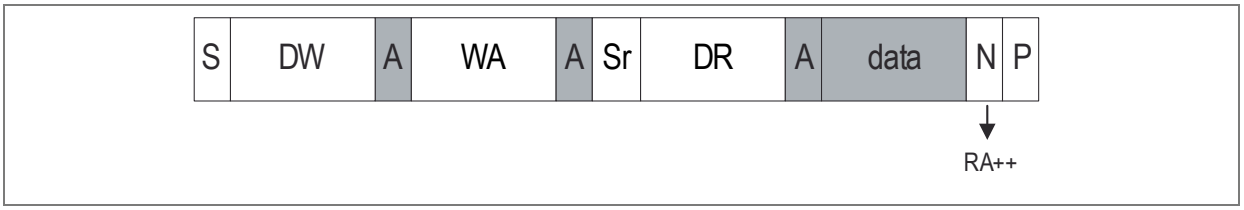


The transmission begins with the START condition, which is generated by the master when the bus is in an IDLE state (the bus is free). The device-write address is followed by the word address. After the word address, any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

7.9.2.3 I²C read

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address or, with a new transmission START followed by the device-read address - when the bus is in an IDLE state. The device-read address is always followed by the first register byte transmitted from the slave. In Read mode, any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 38: I²C random read format

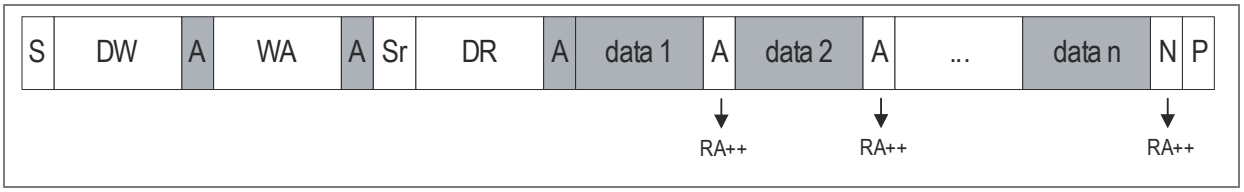


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

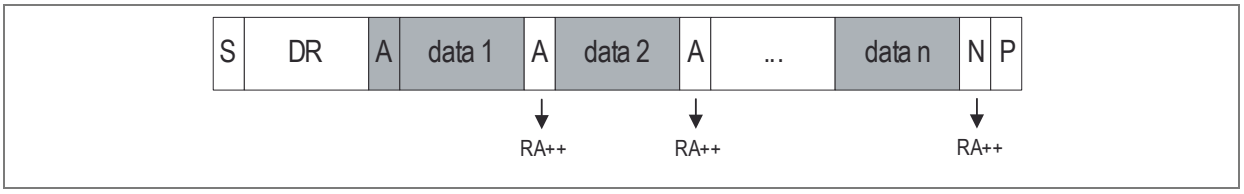
To change the data direction, a repeated START condition is issued on the first SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state, the slave transmits register data, located by the previously received word address vector. The master responds to the data byte with a “not-acknowledge” and issues a STOP condition on the bus.

Figure 39: I²C sequential read format



Sequential Read is the extended form of Random Read, as more than one register-data byte is subsequently transferred. In contrast to the Random Read, for a sequential read, the transferred register-data bytes are responded to with an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission, the master has to send a “not-acknowledge” following the last data byte and subsequently generate the STOP condition.

Figure 40: I²C current address read format



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle, and the master issues a START condition, followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a “not-acknowledge” after the first register byte. Analogous to Sequential Read, an unlimited number of data bytes can be transferred - where the data bytes have to be responded to with an acknowledge from the master. For termination of the transmission, the master sends a “not-acknowledge” following the last data byte and a subsequent STOP condition.

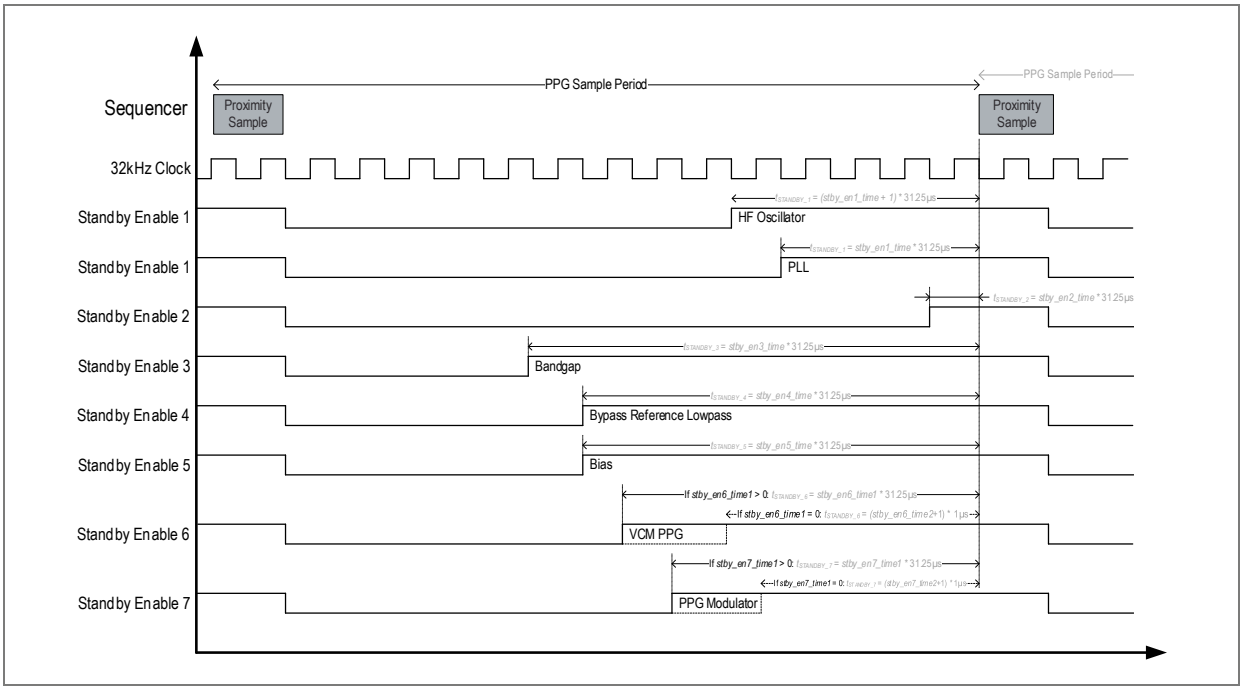
7.10 Standby operation mode

AS7150 supports standby operation mode to reduce overall power consumption during the pause times while no measurement is ongoing. Especially at very low sample rates standby mode helps to reduce system power consumption to extend the battery lifetime of a device. The standby mode function is controlled with up to 7 different standby mode enable control signals. Each of the seven standby enable signals controls a dedicated hardware block of AS7150. An overview of the 7 different control signals is shown in Table 12 below. Furthermore, it contains information about the related blocks which are necessary for a certain application. In addition to the enable registers each Standby Enable signal is also connected to a dedicated timing register to define the standby startup timing of the functional block. A simplified timing diagram of all Standby Enable signals is shown in Figure 41.

Table 12: Standby mode control signal overview

Standby control signal	Function	Timing control registers	Functionality
Standby enable 1	Controls and enables the internal PLL and high frequency oscillator.	*stby_en1_time*	Required for proximity measurement
Standby enable 2	Controls and enables the voltage reference for the LED drivers	*stby_en2_time*	Required for proximity measurement
Standby enable 3	Controls and enables on chip bandgap and bias reference current	*stby_en3_time*	Required for proximity measurement
Standby enable 4	Controls and enables the bypass functions of the low pass filter	*stby_en4_time*	Required for proximity measurement
Standby enable 5	Controls and enables the bias voltage block of the current DAC	*stby_en5_time*	Required for proximity measurement
Standby enable 6	Controls and enables the PPG common mode voltage buffer	*stby_en6_time1* *stby_en6_time2*	Required for proximity measurement
Standby enable 7	Controls and enables the PPG modulators	*stby_en7_time1* *stby_en7_time2*	Required for proximity measurement

Figure 41: Standby timing behavior



The timings which are defined in the timing registers for each control signal define the start of a block prior to the actual measurement start. The timing registers allow for exact control of the startup timing behavior of all relevant blocks and it makes sure that all system blocks are active and properly settled when a measurement is started. Right after the measurement is finished and the measurement data is written to the FIFO memory of AS7150 all Standby Enable signals are disabled again and the connected blocks are powered down. Important to mention is that Standby Enable 1 – Standby Enable 5 signals do have only one timing control register (*stby_enX_time*). Each register is linked to the 32 kHz clock domain of the device which results into a 31.25 µs multiplication factor for these registers like it is also indicated in Figure 41. The Standby Enable 6 and Standby Enable 7 control signals have two timing control registers. The *stby_enX_time* timing registers are also linked to the 32 kHz clock domain of the device which results into a 31.25 µs multiplication factor for these registers. The second timing control register *stby_enX_time2* which is also linked to Standby Enable 6 and Standby Enable 7 is connected to the 2 MHz clock domain of AS7150 which results in a 1 µs multiplication factor for these registers. Only one of the two-timing registers for a Standby Enable signal can be active at a time and the priority is controlled with the register content. In case a value greater than zero is written to *stby_enX_time* register the register content of *stby_enX_time2* register is ignored and the timing is calculated and executed based on the register content of *stby_enX_time* register. In case the *stby_enX_time* register is set to zero, the content of register *stby_enX_time2* is used for the Standby Enable signal timing based on the 1 µs clock domain.

8 Register description

The device is controlled and monitored by registers accessed through the I²C interface. These registers provide device control functions and can be read - to determine the device status and acquire device data.

The register set is summarized below in Table 13. The values of all registers and fields that are listed as reserved, or are not listed, must not be changed. Two-byte fields are always latched with the low byte, followed by the high byte. The “Name” column illustrates the purpose of each register - by highlighting the function associated with each bit. The bits are shown from MSB (D7) to LSB (D0). The gray fields are reserved, and their values must not be changed.

8.1 Register overview

Table 13: Register overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
OTP									
0x10	**CONTROL**								*i2c_fm_plus*
0x11	**CGB_CFG**	*bgcal_done_sel*	*bgcal_en*				*pll_on*	*hf_osc_on*	*lf_osc_on*
0x12	**INT_CFG**		*int_e2*	*int_e4*	*int_sr*	*int_pu*	*int_pd*		*int_inv*
0x13	**CSXN_CFG**		*csxn_e2*	*csxn_e4*	*csxn_sr*	*csxn_pu*	*csxn_pd*		
0x14	**IO_CFG**		*sda_e2*	*sda_e4*	*sda_sr*				
0x15	**REF_CFGA**	*en_bg*	*sel_ln_iled*	*en_vcm_ppg*	*sel_strtup*	*en_vr_led*	*en_bias*	*en_ptat*	*byp_ref_lp*
0x16	**REF_CFGB**			*iled_tc*			*sel_iref_ln*	*byp_progtc*	*sel_ref*
0x19	**MOD_CFGA**							*mod_opamp_ibias*	
0x1A	**MOD_CFGB**		*mod_dsm_mode*		*mod_comp_mode*		*mod_ref_mode*		
0x1B	**MOD1_CFGA**			*mod1_ios_mux*	*mod1_en*	*mod1_ios_dir*	*mod1_ios_fs*		
0x1C	**MOD1_CFGB**					*mod1_iref_scale*			
0x1D	**MOD1_CFGC**			*mod1_seq1_dsm_ampl*		*mod1_seq1_cint*			
0x1E	**MOD1_CFGD**	*mod1_seq1_iref*							
0x1F	**MOD1_CFGE**			*mod1_seq2_dsm_ampl*		*mod1_seq2_cint*			
0x20	**MOD1_CFGF**	*mod1_seq2_iref*							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x21	**MOD2_CFGA**			mod2_ios_mux	*mod2_en*	*mod2_ios_dir*	*mod2_ios_fs*		
0x22	**MOD2_CFGB**					*mod2_iref_scale*			
0x23	**MOD2_CFGC**			mod2_seq1_dsm_ampl		*mod2_seq1_cint*			
0x24	**MOD2_CFGD**	*mod2_seq1_iref*							
0x25	**MOD2_CFGE**			*mod2_seq2_dsm_ampl*	*mod2_seq2_cint*				
0x26	**MOD2_CFGF**	*mod2_seq2_iref*							
0x28	**VCSEL_CFG**	vcsel_we_disable	vcsel_safety_disable	*vcsel_vrsel*		*vcsel_short_vdd_wait*		*vcsel_short_vss_wait*	
0x29	**SEQ1_LED1_CURR**			*seq1_led1_curr*					
0x2A	**SEQ2_LED1_CURR**			*seq2_led1_curr*					
0x2B	**SEQ1_LED2_CURR**		*seq1_led2_curr*						
0x2C	**SEQ2_LED2_CURR**		*seq2_led2_curr*						
0x2D	**SEQ1_LED3_CURR**		*seq1_led3_curr*						
0x2E	**SEQ2_LED3_CURR**		*seq2_led3_curr*						
0x2F	**LED_SEQ1_SUB12**		*led_seq1_sub1*				*led_seq1_sub2*		
0x30	**LED_SEQ1_SUB34**		*led_seq1_sub3*				*led_seq1_sub4*		
0x31	**LED_SEQ1_SUB56**		*led_seq1_sub5*				*led_seq1_sub6*		
0x32	**LED_SEQ1_SUB78**		*led_seq1_sub7*				*led_seq1_sub8*		
0x33	**LED_SEQ2_SUB12**		*led_seq2_sub1*				*led_seq2_sub2*		
0x34	**LED_SEQ2_SUB34**		*led_seq2_sub3*				*led_seq2_sub4*		
0x35	**LED_LOWVDS_WAIT**	*lowvds_wait*							
0x37	**PP_CFG**	*asat_on*				*asat_fil*			
0x38	**SEQ1_SUB12_PP**	*mod1_seq1_sub1_pp*		*mod2_seq1_sub1_pp*		*mod1_seq1_sub2_pp*		*mod2_seq1_sub2_pp*	
0x39	**SEQ1_SUB34_PP**	*mod1_seq1_sub3_pp*		*mod2_seq1_sub3_pp*		*mod1_seq1_sub4_pp*		*mod2_seq1_sub4_pp*	
0x3A	**SEQ1_SUB56_PP**	*mod1_seq1_sub5_pp*		*mod2_seq1_sub5_pp*		*mod1_seq1_sub6_pp*		*mod2_seq1_sub6_pp*	
0x3B	**SEQ1_SUB78_PP**	*mod1_seq1_sub7_pp*		*mod2_seq1_sub7_pp*		*mod1_seq1_sub8_pp*		*mod2_seq1_sub8_pp*	
0x3C	**SEQ2_SUB12_PP**	*mod1_seq2_sub1_pp*		*mod2_seq2_sub1_pp*		*mod1_seq2_sub2_pp*		*mod2_seq2_sub2_pp*	
0x3D	**SEQ2_SUB34_PP**	*mod1_seq2_sub3_pp*		*mod2_seq2_sub3_pp*		*mod1_seq2_sub4_pp*		*mod2_seq2_sub4_pp*	
0x3F	**IRQ_ENABLE**	*irq_en_prox_on*	*irq_en_prox_off*	*irq_en_vcsel*	*irq_en_asat*	*irq_en_led_lowvds*	*irq_en_fifooverflow*	*irq_en_fifotreshold*	*irq_en_sequencer*
0x40	**SEQ_SAMPLE**	*seq_sample*							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x41	**SEQ_SUB_WAIT**	*sub_wait*							
0x42	**SEQ_MODCONF**				*mod_reset_delay*			*modclk*	
0x43	**SEQ_CONFIG**	*seq2_en*		*seq2_sub_sample*		*seq1_en*	*seq1_sub_sample*		
0x44	**SEQ_SAR_WAIT**	*sar_wait*							
0x45	**SEQ_LED_INIT**	*led_init*							
0x46	**SEQ_FREQL**	*seq_freq[7:0]*							
0x47	**SEQ_FREQH**	*seq_freq[15:8]*							
0x48	**SEQ1_FREQDIVL**	*seq1_freqdiv[7:0]*							
0x49	**SEQ1_FREQDIVH**	*seq1_freqdiv[15:8]*							
0x4A	**SEQ2_FREQDIVL**	*seq2_freqdiv[7:0]*							
0x4B	**SEQ2_FREQDIVH**	*seq2_freqdiv[15:8]*							
0x4C	**MOD1_SEQ1_SUB_EN**	*mod1_seq1_sub_en*							
0x4D	**MOD1_SEQ2_SUB_EN**					*mod1_seq2_sub_en*			
0x4E	**MOD2_SEQ1_SUB_EN**	*mod2_seq1_sub_en*							
0x4F	**MOD2_SEQ2_SUB_EN**					*mod2_seq2_sub_en*			
0x50	**SEQ1_MODE_A**	*seq1_sub1_mode*		*seq1_sub2_mode*		*seq1_sub3_mode*		*seq1_sub4_mode*	
0x51	**SEQ1_MODE_B**	*seq1_sub5_mode*		*seq1_sub6_mode*		*seq1_sub7_mode*		*seq1_sub8_mode*	
0x52	**SEQ2_MODE**	*seq2_sub1_mode*		*seq2_sub2_mode*		*seq2_sub3_mode*		*seq2_sub4_mode*	
0x53	**PD_SEQ1_SUB1**		*mod1_seq1_sub1_pdsel*			*mod2_seq1_sub1_pdsel*			
0x54	**PD_SEQ1_SUB2**		*mod1_seq1_sub2_pdsel*			*mod2_seq1_sub2_pdsel*			
0x55	**PD_SEQ1_SUB3**		*mod1_seq1_sub3_pdsel*			*mod2_seq1_sub3_pdsel*			
0x56	**PD_SEQ1_SUB4**		*mod1_seq1_sub4_pdsel*			*mod2_seq1_sub4_pdsel*			
0x57	**PD_SEQ1_SUB5**		*mod1_seq1_sub5_pdsel*			*mod2_seq1_sub5_pdsel*			
0x58	**PD_SEQ1_SUB6**		*mod1_seq1_sub6_pdsel*			*mod2_seq1_sub6_pdsel*			
0x59	**PD_SEQ1_SUB7**		*mod1_seq1_sub7_pdsel*			*mod2_seq1_sub7_pdsel*			
0x5A	**PD_SEQ1_SUB8**		*mod1_seq1_sub8_pdsel*			*mod2_seq1_sub8_pdsel*			
0x5B	**PD_SEQ2_SUB1**		*mod1_seq2_sub1_pdsel*			*mod2_seq2_sub1_pdsel*			
0x5C	**PD_SEQ2_SUB2**		*mod1_seq2_sub2_pdsel*			*mod2_seq2_sub2_pdsel*			
0x5D	**PD_SEQ2_SUB3**		*mod1_seq2_sub3_pdsel*			*mod2_seq2_sub3_pdsel*			
0x5E	**PD_SEQ2_SUB4**		*mod1_seq2_sub4_pdsel*			*mod2_seq2_sub4_pdsel*			
0x5F	**PDSEL_CFG**								*pdref_sel*
0x61	**SEQ1_SINC_CFGA**	*seq1_sinc_ovs*			*seq1_sinc_dec*				
0x62	**SEQ1_SINC_CFGB**		*seq1_os_delay*					*seq1_sel_order*	*seq1_filter_mode*
0x63	**SEQ1_SINC_CFGC**	*seq1_start_delay*							
0x64	**SEQ2_SINC_CFGA**	*seq2_sinc_ovs*			*seq2_sinc_dec*				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x65	**SEQ2_SINC_CFGB**		*seq2_os_delay*					*seq2_sel_order*	*seq2_filter_mode*
0x66	**SEQ2_SINC_CFGC**	*seq2_start_delay*							
0x70	**AOC_MOD1_SEQ1_SUB1**	*aoc_mod1_seq1_sub1*							
0x71	**AOC_MOD1_SEQ1_SUB2**	*aoc_mod1_seq1_sub2*							
0x72	**AOC_MOD1_SEQ1_SUB3**	*aoc_mod1_seq1_sub3*							
0x73	**AOC_MOD1_SEQ1_SUB4**	*aoc_mod1_seq1_sub4*							
0x74	**AOC_MOD1_SEQ1_SUB5**	*aoc_mod1_seq1_sub5*							
0x75	**AOC_MOD1_SEQ1_SUB6**	*aoc_mod1_seq1_sub6*							
0x76	**AOC_MOD1_SEQ1_SUB7**	*aoc_mod1_seq1_sub7*							
0x77	**AOC_MOD1_SEQ1_SUB8**	*aoc_mod1_seq1_sub8*							
0x78	**AOC_MOD1_SEQ2_SUB1**	*aoc_mod1_seq2_sub1*							
0x79	**AOC_MOD1_SEQ2_SUB2**	*aoc_mod1_seq2_sub2*							
0x7A	**AOC_MOD1_SEQ2_SUB3**	*aoc_mod1_seq2_sub3*							
0x7B	**AOC_MOD1_SEQ2_SUB4**	*aoc_mod1_seq2_sub4*							
0x7C	**AOC_MOD2_SEQ1_SUB1**	*aoc_mod2_seq1_sub1*							
0x7D	**AOC_MOD2_SEQ1_SUB2**	*aoc_mod2_seq1_sub2*							
0x7E	**AOC_MOD2_SEQ1_SUB3**	*aoc_mod2_seq1_sub3*							
0x7F	**AOC_MOD2_SEQ1_SUB4**	*aoc_mod2_seq1_sub4*							
0x80	**AOC_MOD2_SEQ1_SUB5**	*aoc_mod2_seq1_sub5*							
0x81	**AOC_MOD2_SEQ1_SUB6**	*aoc_mod2_seq1_sub6*							
0x82	**AOC_MOD2_SEQ1_SUB7**	*aoc_mod2_seq1_sub7*							
0x83	**AOC_MOD2_SEQ1_SUB8**	*aoc_mod2_seq1_sub8*							
0x84	**AOC_LEDOFF**	*aoc_ledoff*							
0x85	**AOC_CFG**				*dis_ledoff*		*aoc_ovs*		
0x86	**AOC_MOD1_THH**	*aoc_mod1_thh*							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x87	**AOC_MOD1_THL**	*aoc_mod1_thl*							
0x88	**AOC_MOD2_THH**	*aoc_mod2_thh*							
0x89	**AOC_MOD2_THL**	*aoc_mod2_thl*							
0x8A	**AOC_SAR_THRES**	*sar_thres*							
0x8B	**MOD1_SEQ1_AOC_EN**	*mod1_seq1_aoc_en*							
0x8C	**MOD2_SEQ1_AOC_EN**							*mod2_seq1_aoc_en*	
0x98	**PROX_CFG**				*prox_en*			*prox_sub*	
0x99	**PROX_OVS**		*prox_on_ovs*				*prox_off_ovs*		
0x9A	**PROX_THH_L**	*prox_thh[7:0]*							
0x9B	**PROX_THH_H**	*prox_thh[15:8]*							
0x9C	**PROX_THL_L**	*prox_thl[7:0]*							
0x9D	**PROX_THL_H**	*prox_thh[15:8]*							
0xA0	**STANDBY_ON**		*stby_en_on*						
0xA1	**STANDBY_EN1**	*stby_en1_time*							
0xA2	**STANDBY_EN2**	*stby_en2_time*							
0xA3	**STANDBY_EN3**	*stby_en3_time*							
0xA4	**STANDBY_EN4**	*stby_en4_time*							
0xA5	**STANDBY_EN5**	*stby_en5_time*							
0xA6	**STANDBY_EN6**	*stby_en6_time1*			*stby_en6_time2*				
0xA7	**STANDBY_EN7**	*stby_en7_time1*			*stby_en7_time2*				
0xD0	**FIFO_TRESHOLD**	*fifo_treshold[7:0]*							
0xD1	**FIFO_CTRL**	*fifo_clear*				*sar_data_en*			*fifo_treshold[8]*
0xEC	**PRODUCT_ID**	*otp_part_id*							
0xED	**SILICON_ID**	*silicon_id*							
0xEE	**REVISION**					*revision*			
0xEF	**CHIP_CTRL**								*chip_reset*
0xF0	**SEQ_START**								*seq_start*
0xF4	**STATUS_CGBB**					*pll_lock*	*clk_pll_ok*	*lf_bgcal_ok*	*lf_bgcal_ready*
0xF5	**STATUS_SEQ**							*seq_end*	*seq_error*
0xF6	**STATUS_LED**						*led_lowvds*		
0xF7	**STATUS_ASAT**	*mod1_asat*				*mod2_asat*			
0xF8	**STATUS_VCSEL**						*vcsel_short_vss*	*vcsel_short_vdd*	*vcsel_wd*

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0xF9	**STATUS_PROX**		*prox_high*	*prox_high_on*	*prox_high_off*		*prox_low*	*prox_low_on*	*prox_low_off*
0xFA	**STATUS**	*irq_prox*	*irq_vcsel*	*irq_asat*	*irq_led_lowvds*	*irq_fifooverflow*	*irq_fifothreshold*		*irq_sequencer*
0xFB	**FIFO_LEVEL0**	*fifo_level[7:0]*							
0xFC	**FIFO_LEVEL1**						*fifo_overflow*	*fifo_level[9:8]*	
0xFD	**FIFOL**	*fifol*							
0xFE	**FIFOM**	*fifom*							
0xFF	**FIFOH**	*fifoh*							

8.2 Control

8.2.1 CONTROL register (Address 0x10)

Table 14: CONTROL register

Addr: 0x10		CONTROL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*i2c_fm_plus*	0	R/W	This bit enables the I²C fast mode plus operation mode with up to 1MHz clock frequency. 0: Fast Mode Plus disabled 1: Fast Mode Plus enabled

8.2.2 CGB_CFG register (Address 0x11)

Table 15: CGB_CFG register

Addr: 0x11		CGB_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*bgcal_done_sel*	0	R/W	This configuration bit defines how often the 32 kHz calibration is executed. 0: Only one calibration cycle executed 1: Calibration running until low frequency oscillator is close to 32 kHz
6	*bgcal_en*	0	PUSH1	Once this bit is set to one calibration of the 32 kHz low frequency oscillator is started. 0: 32 kHz oscillator calibration disabled 1: 32 kHz oscillator calibration enabled
2	*pll_on*	0	R/W	The bit enables the internal PLL for the 20 MHz clock to operate the ADCs. 0: 20 MHz PLL disabled 1: 20 MHz PLL enabled
1	*hf_osc_on*	0	R/W	This bit enables the internal 2 MHz on chip high frequency oscillator. Please mind that there is a 100µs settling time mandatory once the 32 kHz low frequency oscillator is enabled, via *lf_osc_on*_register, before the high freqeuncy oscillator can be switch on. 0: 2 MHz high frequency oscillator disabled 1: 2 MHz high frequency oscillator enabled
0	*lf_osc_on*	0	R/W	This bit enables the internal 32kHz low frequency oscillator. 0: 32 kHz low frequency oscillator disabled 1: 32 kHz low frequency oscillator enabled

8.2.3 INT_CFG register (Address 0x12)

Table 16: INT_CFG register

Addr: 0x12		INT_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6	*int_e2*	0	R/W	This bit controls together with bit *int_e4*_the output driving strength of the INT pin. 0: Normal INT driving strength 1: Extended INT driving strength
5	*int_e4*	0	R/W	This bit controls together with bit *int_e2*_the output driving strength of the INT pin. This bit should be enabled in case driving strength of INT is still not sufficient after *int_e2* bit was set to one. 0: Normal INT driving strength 1: Extended INT driving strength
4	*int_sr*	0	R/W	This bit allows for a change of the INT pin slew rate. 0: Normal INT pin slew rate 1: Fast INT pin slew rate
3	*int_pu*	0	R/W	This bit enabled the internal pull-up resistor of the INT pin. 0: Pull-up resistor disabled 1: Pull-up resistor enabled
2	*int_pd*	0	R/W	This bit enabled the internal pull-down resistor of the INT pin. 0: Pull-down resistor disabled 1: Pull-down resistor enabled
0	*int_inv*	0	R/W	This bit can change the polarity of the IRQ output pin. 0: Normal output operation of INT pin 1: Inverted output operation of INT pin

8.2.4 IO_CFG register (Address 0x14)

Table 17: IO_CFG register

Addr: 0x14		IO_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6	*sda_e2*	*0*	R/W	This bit controls together with bit *sda_e4*_the output driving strength of the SDA pin. 0: Normal SDA driving strength 1: Extended SDA driving strength
5	*sda_e4*	0	R/W	This bit controls together with bit *sda_e2*_the output driving strength of the SDA pin. This bit should be enabled in case driving strength of SDA is still not sufficient after *sda_e2* bit was set to one. 0: Normal SDA driving strength 1: Extended SDA driving strength
4	*sda_sr*	0	R/W	This bit allows for a change of the SDA pin slew rate. 0: Normal SDA pin slew rate 1: Fast SDA pin slew rate

8.2.5 REF_CFGA register (Address 0x15)

Table 18: REF_CFGA register

Addr: 0x15		REF_CFGA		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*en_bg*	0	R/W	This bit enabled the bandgap which is the main voltage reference used to generate all internal voltages and reference currents. 0: Bandgap disabled 1: Bandgap enabled
6	*sel_ln_iled*	1	R/W	This bit enables the low noise voltage source for the LED reference current. 0: Low noise source disabled 1: Low noise source enabled
5	*en_vcm_ppg*	0	R/W	This bit enabled the VCM PPG buffer. The voltage reference for the ADCs is enabled before a measurement and disabled in standby operation mode. 0: VCM PPG buffer disabled 1: VCM PPG buffer enabled
4	*sel_strtup*	0	R/W	This bit controls the internal bandgap startup. Do not change default configuration of this register. 0: Default configuration 1: Do not use
3	*en_vr_led*	0	R/W	This bit enables the voltage reference of the LED driver as well as the LED buffer. 0: LED buffer and reference voltage disabled 1: LED buffer and reference voltage enabled
2	*en_bias*	0	R/W	This bit enables the reference current bias reference of the ambient light DC offset DAC. 0: Reference current disabled 1: Reference current enabled
1	*en_ptat*	0	R/W	This bit controls the tail current of the VCM buffers. Do not change default configuration of this register. 0: Default configuration 1: Do not use
0	*byp_ref_lp*	0	R/W	This control bit enables the low-pass filter bypass mode of the internal bandgap voltage for a faster device startup. 0: Bypass mode disabled 1: Bypass mode enabled

8.2.6 REF_CFGB register (Address 0x16)

Table 19: REF_CFGB register

Addr: 0x16		REF_CFGB		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:3	*iled_tc*	0	R/W	This five-bit register allows to configure a temperature coefficient for the LED current.
2	*sel_iref_ln*	1	R/W	This bit enables a low noise current reference for the offset compensation current DAC. 0: Regular current reference selected 1: Low noise current reference selected
1	*byp_progtc*	1	R/W	This is the bypass enable bit for the temperature compensation circuit for the LED current. 0: Bypass disabled 1: Bypass enabled
0	*sel_ref*	0	R/W	This bit controls the voltage level of the common mode buffer. 0: 0.8 V VCM voltage level 1: 0.75 V VCM voltage level

8.2.7 PDSEL_CFG register (Address 0x5F)

Table 20: PDSEL_CFG register

Addr: 0x5F		PDSEL_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*pdref_sel*	0	R/W	This register controls the internal reference voltage switch of the PDREF input pin. If this bit is set to one the PDREF input pin is connected to VSSA which is an analog ground voltage. If this bit is set to zero the pin is connected to internal PPG common mode voltage level which is typically 0.8V. Please refer to Figure 11 for a block diagram which shows the internal connection of the control switch. 0: Connected to VCM_PPG 1: Connected to VSSA

8.2.8 CHIP_CTRL register (Address 0xEF)

Table 21: CHIP_CTRL register

Addr: 0xEF		CHIP_CTRL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*chip_reset*	0	PUSHPOP	This is the chip reset register. Once the bit is written to one a device reset is triggered like it happens during power on of the device. 0: Normal device operation 1: Chip reset is triggered

8.2.9 SEQ_START register (Address 0xF0)

Table 22: SEQ_START register

Addr: 0xF0		SEQ_START		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*start_seq*	0	R_PUSH	This bit controls the start and stop of the sequencer with all enabled subsamples. Once this bit is set to one the sequencer starts the number of measurements defined in **SEQ_SAMPLE** register. If the **SEQ_SAMPLE** register is set to zero the sequencer is running in continuous mode. 0: Sequencer is stopped 1: Sequencer is running

8.3 ADC modulators and offset DAC

8.3.1 MOD_CFGA register (Address 0x19)

Table 23: MOD_CFGA register

Addr: 0x19		MOD_CFGA		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1:0	*mod_opamp_ibias*	0	R/W	This configuration bit is used for internal production testing. Please do not change default value of this register. 0: Default configuration 1: Do not use 2: Do not use 3: Do not use

8.3.2 MOD_CFGB register (Address 0x1A)

Table 24: MOD_CFGB register

Addr: 0x1A		MOD_CFGB		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:5	*mod_dsm_mode*	0	R/W	This configuration bit is used for internal production testing for the ADC modulator. Please do not change default value of this register. 0: Default configuration 1: Do not use 2: Do not use 3: Do not use
4:3	*mod_comp_mode*	0	R/W	This bit enables the modulator comparator operation mode. Please do not change register setting from its default configuration unless advised by ams OSRAM support team.
2:0	*mod_ref_mode*	0	R/W	This bit enables the reference DAC operation mode. Please do not change register setting from its default configuration unless advised by ams OSRAM support team.

8.3.3 MOD1_CFGA register (Address 0x1B)

Table 25: MOD1_CFGA register

Addr: 0x1B		MOD1_CFGA		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5	*mod1_ios_mux*	0	R/W	This bit allows to connect the offset DAC of modulator 2 to be connect to modulator 1 for calibration purpose. 0: Offset DAC 1 connected to modulator 1 1: Offset DAC 2 connected to modulator 1
4	*mod1_en*	0	R/W	This bit enables the ADC modulator 1. 0: ADC Modulator 1 disabled 1: ADC Modulator 1 enabled
3	*mod1_ios_dir*	0	R/W	This register controls the current direction of the offset DAC for modulator 1. Please do not change this register. 0: Default configuration 1: Do not use
2:0	*mod1_ios_fs*	4	R/W	This register allows for the full-scale configuration of the offset DAC for ADC modulator 1 which is used for ambient light cancellation. 0: 1µA 1: 2µA 2: 4µA 3: 8µA 4: 16µA 5: 32µA 6: 64µA 7: 128µA

8.3.4 MOD1_CFGB register (Address 0x1C)

Table 26: MOD1_CFGB register

Addr: 0x1C		MOD1_CFGB		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3:0	*mod1_iref_scale*	0	R/W	This register controls the current reference scale factor for the DAC current reference of modulator 1. Please contact ams OSRAM support team for correct configuration of this register. 0: Do not use 1: Do not use 2: Do not use 3: Do not use 4: 0.625 5: Do not use 6: Do not use 7: 1.000 8-15: Do not use

8.3.5 MOD1_CFGC register (Address 0x1D)

Table 27: MOD1_CFGC register

Addr: 0x1D		MOD1_CFGC		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5	*mod1_seq1_dsm_ampl*	0	R/W	This bit allows for a change of the DSM integrator amplitude scale. Please contact local ams OSRAM support team for correct configuration of this register.
4:0	*mod1_seq1_cint*	0	R/W	This register configures the integrator capacity of ADC modulator 1 of sequencer 1. Please contact local ams OSRAM support team for correct configuration of this register. 0: 1 pF 2: 2 pF … 15: 16 pF 16 … 31: Do not use

8.3.6 MOD1_CFGD register (Address 0x1E)

Table 28: MOD1_CFGD register

Addr: 0x1E		MOD1_CFGD		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*mod1_seq1_iref*	0	R/W	The register allows for the configuration of the current P-DAC reference current for sequencer 1. Please contact local ams OSRAM support team for correct configuration of this register. 0: 1 µA 2: 2 µA … 31: 32µA 32 … 255: Do not use

8.3.7 MOD1_CFGE register (Address 0x1F)

Table 29: MOD1_CFGE register

Addr: 0x1F		MOD1_CFGE		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5	*mod1_seq2_dsm_ampl*	0	R/W	This bit allows for a change of the DSM integrator amplitude scale. Please contact local ams OSRAM support team for correct configuration of this register.
3:0	*mod1_seq2_cint*	0	R/W	This register configures the integrator capacity of ADC modulator 1 for sequencer 2. Please contact local ams OSRAM support team for correct configuration of this register. 0: 1 pF 2: 2 pF … 15: 16 pF 16 … 31: Do not use

8.3.8 MOD1_CFGF register (Address 0x20)

Table 30: MOD1_CFGF register

Addr: 0x20		MOD1_CFGF		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*mod1_seq2_iref*	0	R/W	The register allows for the configuration of the current P-DAC reference current for sequencer 2 of ADC modulator 1. Please contact local ams OSRAM support team for correct configuration of this register. 0: 1µA 2: 2µA … 31: 32µA 32 … 255: Do not use

8.3.9 MOD2_CFGA register (Address 0x21)

Table 31: MOD2_CFGA register

Addr: 0x21		MOD2_CFGA		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5	*mod2_ios_mux*	0	R/W	This bit allows to connect the offset DAC of modulator 1 to be connected to modulator 2 for calibration purpose. 0: Offset DAC 2 connected to modulator 2 1: Offset DAC 1 connected to modulator 2
4	*mod2_en*	0	R/W	This bit enables the ADC modulator 2. 0: ADC Modulator 2 disabled 1: ADC Modulator 2 enabled
3	*mod2_ios_dir*	0	R/W	This register controls the current direction of the offset DAC for modulator 2. Please do not change this register. 0: Default configuration 1: Do not use
2:0	*mod2_ios_fs*	4	R/W	This register allows for the full-scale configuration of the offset DAC for ADC modulator 2 which is used for ambient light cancellation. 0: 1 µA 1: 2 µA 2: 4 µA 3: 8 µA 4: 16 µA 5: 32 µA 6: 64 µA 7: 128µA

8.3.10 MOD2_CFGB register (Address 0x22)

Table 32: MOD2_CFGB register

Addr: 0x22		MOD2_CFGB		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3:0	*mod2_iref_scale*	0	R/W	This register controls the current reference scale factor for the DAC current reference of modulator 2. Please contact ams OSRAM support team for correct configuration of this register. 0: Do not use 1: Do not use 2: Do not use 3: Do not use 4: 0.625 5: Do not use 6: Do not use 7: 1.000 8-15: Do not use

8.3.11 MOD2_CFGC register (Address 0x23)

Table 33: MOD2_CFGC register

Addr: 0x23		MOD2_CFGC		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5	*mod2_seq1_dsm_ampl*	0	R/W	This bit allows for a change of the DSM integrator amplitude scale. Please contact local ams OSRAM support team for correct configuration of this register.
4:0	*mod2_seq1_cint*	0	R/W	This register configures the integrator capacity of ADC modulator 2 of sequencer 1. Please contact local ams OSRAM support team for correct configuration of this register. 0: 1 pF 2: 2 pF … 15: 16 pF 16 … 31: Do not use

8.3.12 MOD2_CFGD register (Address 0x24)

Table 34: MOD2_CFGD register

Addr: 0x24		MOD2_CFGD		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*mod2_seq1_iref*	0	R/W	The register allows for the configuration of the current P-DAC reference current for sequencer 1. Please contact local ams OSRAM support team for correct configuration of this register. 0: 1 µA 2: 2 µA … 31: 32µA 32 … 255: Do not use

8.3.13 MOD2_CFGE register (Address 0x25)

Table 35: MOD2_CFGE register

Addr: 0x25		MOD2_CFGE		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5	*mod2_seq2_dsm_ampl*	0	R/W	This bit allows for a change of the DSM integrator amplitude scale. Please contact local ams OSRAM support team for correct configuration of this register.
3:0	*mod2_seq2_cint*	0	R/W	This register configures the integrator capacity of ADC modulator 2 for sequencer 2. Please contact local ams OSRAM support team for correct configuration of this register. 0: 1pF 2: 2pF … 15: 16pF 16 … 31: Do not use

8.3.14 MOD2_CFGF register (Address 0x26)

Table 36: MOD2_CFGF register

Addr: 0x26		MOD2_CFGF		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*mod2_seq2_iref*	0	R/W	The register allows for the configuration of the current P-DAC reference current for sequencer 2 of ADC modulator 2. Please contact local ams OSRAM support team for correct configuration of this register. 0: 1µA 2: 2µA … 31: 32µA 32 … 255: Do not use

8.4 VCSEL configuration

8.4.1 VCSEL_CFG register (Address 0x28)

Table 37: VCSEL_CFG register

Addr: 0x28		VCSEL_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*vcsel_wd_disable*	0	R/W	This bit disables the VCSEL/LED watchdog function of AS7150. 0: VCSEL watchdog enabled 1: VCSEL watchdog disabled
6	*vcsel_safety_disable*	0	R/W	This bit disables the safety control logic evaluation of the short circuit to VSS/VDD signals. 0: Control logic enabled 1: Control logic disabled
5:4	*vcsel_vrsel*	0	R/W	This register controls the reference voltage level for the build in comparators of the VCSEL watchdog. 0: 50mV 1: 100mV 2: 150mV 3: 200mV
3:2	*vcsel_short_vdd_wait*	0	R/W	This register defines the time between switching on short detection and the valid result for a VDD connection. All VCSEL LEDs use the same time. 0: 2µs 1: 4µs 2: 8µs 3: 1µs
1:0	*vcsel_short_vss_wait*	0	R/W	This register defines the time between switching on short detection and the valid result for a VSS connection. All VCSEL LEDs use the same time. 0: 2µs 1: 4µs 2: 8µs 3: 12µs

8.5 LED currents

8.5.1 SEQ1_LED1_CURR register (Address 0x29)

Table 38: SEQ1_LED1_CURR register

Addr: 0x29		SEQ1_LED1_CURR		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5:0	*seq1_led1_curr*	0	R/W	This 6-bit register controls the VCSEL current for LED1 input for sequencer 1. 0: 0.313mA 1: 0.625mA 2: 0.938mA … 62: 19.7mA 63: 20mA

8.5.2 SEQ2_LED1_CURR register (Address 0x2A)

Table 39: SEQ2_LED1_CURR register

Addr: 0x2A		SEQ2_LED1_CURR		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5:0	*seq2_led1_curr*	0	R/W	This 6-bit register controls the VCSEL current for LED1 input for sequencer 2. 0: 0.313mA 1: 0.625mA 2: 0.938mA … 62: 19.7mA 63: 20mA

8.5.3 SEQ1_LED2_CURR register (Address 0x2B)

Table 40: SEQ1_LED2_CURR register

Addr: 0x2B		SEQ1_LED2_CURR		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:0	*seq1_led2_curr*	0	R/W	This 7-bit register controls the LED current for LED2 input for sequencer 1. 0: 1.563mA 1: 3.125mA 2: 4.688mA … 62: 198.4mA 63: 200mA

8.5.4 SEQ2_LED2_CURR register (Address 0x2C)

Table 41: SEQ2_LED2_CURR register

Addr: 0x2C		SEQ2_LED2_CURR		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:0	*seq2_led2_curr*	0	R/W	This 7-bit register controls the LED current for LED2 input for sequencer 2. 0: 1.563mA 1: 3.125mA 2: 4.688 mA … 62: 198.4mA 63: 200mA

8.5.5 SEQ1_LED3_CURR register (Address 0x2D)

Table 42: SEQ1_LED3_CURR register

Addr: 0x2D		SEQ1_LED3_CURR		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:0	*seq1_led3_curr*	0	R/W	This 7-bit register controls the LED current for LED3 input for sequencer 1. 0: 1.563mA 1: 3.125mA 2: 4.688mA … 62: 198.4mA 63: 200mA

8.5.6 SEQ2_LED3_CURR register (Address 0x2E)

Table 43: SEQ2_LED3_CURR register

Addr: 0x2E		SEQ2_LED3_CURR		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:0	*seq2_led3_curr*	0	R/W	This 7-bit register controls the LED current for LED3 input for sequencer 2. 0: 1.563mA 1: 3.125mA 2: 4.688mA … 62: 198.4mA 63: 200mA

8.6 LED sequencer / subsample assignment

8.6.1 LED_SEQ1_SUB12 register (Address 0x2F)

Table 44: LED_SEQ1_SUB12 register

Addr: 0x2F		LED_SEQ1_SUB12		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*led_seq1_sub1*	0	R/W	This register assigns for sequencer 1, in subsample 1, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned
2:0	*led_seq1_sub2*	0	R/W	This register assigns for sequencer 1, in subsample 2, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned

8.6.2 LED_SEQ1_SUB34 register (Address 0x30)

Table 45: LED_SEQ1_SUB34 register

Addr: 0x30		LED_SEQ1_SUB34		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*led_seq1_sub3*	0	R/W	This register assigns for sequencer 1, in subsample 3, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned
2:0	*led_seq1_sub4*	0	R/W	This register assigns for sequencer 1, in subsample 4, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned

8.6.3 LED_SEQ1_SUB56 register (Address 0x31)

Table 46: LED_SEQ1_SUB56 register

Addr: 0x31		LED_SEQ1_SUB56		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*led_seq1_sub5*	0	R/W	This register assigns for sequencer 1, in subsample 5, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned
2:0	*led_seq1_sub6*	0	R/W	This register assigns for sequencer 1, in subsample 6, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned

8.6.4 LED_SEQ1_SUB78 register (Address 0x32)

Table 47: LED_SEQ1_SUB78 register

Addr: 0x32		LED_SEQ1_SUB78		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*led_seq1_sub7*	0	R/W	This register assigns for sequencer 1, in subsample 7, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned
2:0	*led_seq1_sub8*	0	R/W	This register assigns for sequencer 1, in subsample 8, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned

8.6.5 LED_SEQ2_SUB12 register (Address 0x33)

Table 48: LED_SEQ2_SUB12 register

Addr: 0x33		LED_SEQ2_SUB12		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*led_seq2_sub1*	0	R/W	This register assigns for sequencer 2, in subsample 1, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned
2:0	*led_seq2_sub2*	0	R/W	This register assigns for sequencer 2, in subsample 2, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned

8.6.6 LED_SEQ2_SUB34 register (Address 0x34)

Table 49: LED_SEQ2_SUB34 register

Addr: 0x34		LED_SEQ2_SUB34		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*led_seq2_sub3*	0	R/W	This register assigns for sequencer 2, in subsample 3, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned
2:0	*led_seq2_sub4*	0	R/W	This register assigns for sequencer 2, in subsample 4, the LED inputs. Each bit of the register represents one LED input whereas the LSB is assigned to LED1 and the MSB is assigned to LED3. 000: No LED assigned to subsample 1 001: LED1 assigned 010: LED2 assigned 011: LED1 and LED2 assigned 100: LED3 assigned 101: LED1 and LED3 assigned 110: LED2 and LED 3 assigned 111: LED1, LED2 and LED3 assigned

8.6.7 LED_LOWVDS_WAIT register (Address 0x35)

Table 50: LED_LOWVDS_WAIT register

Addr: 0x35		LED_LOWVDS_WAIT		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*lowvds_wait*	0	R/W	This register defines the time between switching on a LED and the start of voltage monitoring in 1 µs steps. 0: 0µs 1: 1µs 2: 2µs 3: 3µs … 255: 255µs

8.7 Post processing

8.7.1 PP_CFG register (Address 0x37)

Table 51: PP_CFG register

Addr: 0x37		PP_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*asat_on*	0	R/W	This register enables the analog saturation post processing function of AS7150. 0: Analog sat. post processing disabled 1: Analog sat. post processing enabled
3:0	*asat_fil*	0	R/W	This is the configuration register of the digital filter for analog saturation. The register configures the minimum length of the input pulse to be detected as analog saturation. The minimum detection length is configured with the *asat_fil* register value multiplied with the oscillation period of the digital modulator clock (*modclk*).

8.7.2 SEQ1_SUB12_PP register (Address 0x38)

Table 52: SEQ1_SUB12_PP register

Addr: 0x38		SEQ1_SUB12_PP		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*mod1_seq1_sub1_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 1 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
5:4	*mod2_seq1_sub1_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 1 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
3:2	*mod1_seq1_sub2_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 2 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
1:0	*mod2_seq1_sub2_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 2 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register

8.7.3 SEQ1_SUB34_PP register (Address 0x39)

Table 53: SEQ1_SUB34_PP register

Addr: 0x39		SEQ1_SUB34_PP		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*mod1_seq1_sub3_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 3 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
5:4	*mod2_seq1_sub3_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 3 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
3:2	*mod1_seq1_sub4_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 4 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
1:0	*mod2_seq1_sub4_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 4 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register

8.7.4 SEQ1_SUB56_PP register (Address 0x3A)

Table 54: SEQ1_SUB56_PP register

Addr: 0x3A		SEQ1_SUB56_PP		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*mod1_seq1_sub5_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 5 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
5:4	*mod2_seq1_sub5_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 5 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
3:2	*mod1_seq1_sub6_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 6 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
1:0	*mod2_seq1_sub6_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 6 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register

8.7.5 SEQ1_SUB78_PP register (Address 0x3B)

Table 55: SEQ1_SUB78_PP register

Addr: 0x3B		SEQ1_SUB78_PP		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*mod1_seq1_sub7_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 7 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
5:4	*mod2_seq1_sub7_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 7 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
3:2	*mod1_seq1_sub8_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 8 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
1:0	*mod2_seq1_sub8_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 8 in sequencer 1. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register

8.7.6 SEQ2_SUB12_PP register (Address 0x3C)

Table 56: SEQ2_SUB12_PP register

Addr: 0x3C		SEQ2_SUB12_PP		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*mod1_seq2_sub1_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 1 in sequencer 2. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
5:4	*mod2_seq2_sub1_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 1 in sequencer 2. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
3:2	*mod1_seq2_sub2_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 2 in sequencer 2. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
1:0	*mod2_seq2_sub2_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 2 in sequencer 2. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register

8.7.7 SEQ2_SUB34_PP register (Address 0x3D)

Table 57: SEQ2_SUB34_PP register

Addr: 0x3D		SEQ2_SUB34_PP		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*mod1_seq2_sub3_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 3 in sequencer 2. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
5:4	*mod2_seq2_sub3_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 3 in sequencer 2. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
3:2	*mod1_seq2_sub4_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 1 for subsample 4 in sequencer 2. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register
1:0	*mod2_seq2_sub4_pp*	0	R/W	This register configures the post processing function for ADC modulator channel 2 for subsample 4 in sequencer 2. 0: Normal value 1: Inverted value 2: Value – *pp_offset* register value 3: Write value to *pp_offset* register

8.8 Interrupt

8.8.1 IRQ_ENABLE register (Address 0x3F)

Table 58: IRQ_ENABLE register

Addr: 0x3F		IRQ_ENABLE		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*irq_en_prox_on*	0	R/W	This is interrupt enable register for the integrated proximity function. Once this register is enabled an interrupt is released on a rising edge of the proximity high (**PROX_THH_L** and **PROX_THH_H**) and proximity low threshold (**PROX_THL_L** and **PROX_THL_H**) levels. Please refer to Figure 31 for a timing diagram of the proximity function and its related registers. 0: Proximity interrupt rising edge disabled 1: Proximity interrupt rising edge enabled
6	*irq_en_prox_off*	0	R/W	This is interrupt enable register for the integrated proximity function. Once this register is enabled an interrupt is released on a falling edge of the proximity high (**PROX_THH_L** and **PROX_THH_H**) and proximity low threshold (**PROX_THL_L** and **PROX_THL_H**) levels. Please refer to Figure 31 for a timing diagram of the proximity function and its related registers. 0: Proximity interrupt falling edge disabled 1: Proximity interrupt falling edge enabled
5	*irq_en_vcsel*	0	R/W	This is the interrupt enable register for the VCSEL control safety logic. 0: VCSEL safety interrupt disabled 1: VCSEL safety interrupt enabled
4	*irq_en_asat*	0	R/W	This is the analog saturation interrupt enable register. An interrupt is released once an analog saturation of ADC modulator 1 or ADC modulator 2 is detected. 0: Analog saturation interrupt disabled 1: Analog saturation interrupt enabled
3	*irq_en_led_lowvds*	0	R/W	This is the interrupt enable register which detects a low voltage condition on the LED1, LED2 and LED3 current sinks which means that the configured LED current cannot be guaranteed any more. 0: LED driver low V_{DS} interrupt disabled 1: LED driver low V_{DS} interrupt enabled

Addr: 0x3F		IRQ_ENABLE		
2	*irq_en_fifooverflow*	0	R/W	This is the FIFO overflow interrupt enable register. Please mind that once this interrupt is released for host notification data samples got lost. 0: FIFO overflow interrupt disabled 1: FIFO overflow interrupt enabled
1	*irq_en_fifothreshold*	0	R/W	Interrupt enable register for the FIFO threshold. In case the FIFO level is bigger than the FIFO threshold level, defined in register **FIFO_THRESHOLD**, an interrupt is released. 0: FIFO threshold interrupt disabled 1: FIFO threshold interrupt enabled
0	*irq_en_sequencer*	0	R/W	Interrupt enable register for sequencer. 0: Sequencer interrupt disabled 1: Sequencer interrupt enabled

8.9 Sequencer general

8.9.1 SEQ_SAMPLE register (Address 0x40)

Table 59: SEQ_SAMPLE register

Addr: 0x40		SEQ_SAMPLE		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*seq_sample*	0	R/W	This register defined the number of measurement samples for the activated channel. If the register *seq_sample_* = 0 the sequencer runs continuously.

8.9.2 SEQ_SUB_WAIT register (Address 0x41)

Table 60: SEQ_SUB_WAIT register

Addr: 0x41		SEQ_SUB_WAIT		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*sub_wait*	0	R/W	This register controls the subsample wait time t_{SUB_WAIT} which can be added to have breaks in between each subsample. A detailed timing diagram which shows t_{SUB_WAIT} can be found in chapter 7.6.5. The waiting time is a multiple of 1 µs of the register value which gives a range of 0 – 255µs as subsample waiting time.

8.9.3 SEQ_MODCONF register (Address 0x42)

Table 61: SEQ_MODCONF register

Addr: 0x42		SEQ_MODCONF		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*mod_reset_delay*	0	R/W	This register configures the ADC modulator settling time t_{MOD_RES} after startup or standby mode start of the modulators. A detailed timing diagram which shows t_{MOD_RES} can be found in chapter 7.6.5. The reset times for the different register settings which are shown below are calculated for f_{MOD_CLK} of 10 MHz which is configured via register *modclk*. 0: 4 * (1/ f_{MOD_CLK}) = 0.4 µs 1: 8 * (1/ f_{MOD_CLK}) = 0.8 µs 2: 16 * (1/ f_{MOD_CLK}) = 1.6 µs 3: 32 * (1/ f_{MOD_CLK}) = 3.2 µs 4: 64 * (1/ f_{MOD_CLK}) = 6.4 µs 5: 128 * (1/ f_{MOD_CLK}) = 12.8 µs 6: 256 * (1/ f_{MOD_CLK}) = 25.6 µs 7: 256 * (1/ f_{MOD_CLK}) = 25.6 µs
1:0	*modclk*	0	R/W	This register controls the ADC modulator clock frequency f_{MOD_CLK} which is used for both sequencers and ADC modulators. 0: 10MHz 1: 5MHz 2: 2.5MHz 3: 1.25MHz

With a reduction of the Modulator clock frequency, the converting time will increase, and the signal-to-noise ratio will improve. Please keep in mind that longer converting times lead to and increased power consumption.

8.9.4 SEQ_CONFIG register (Address 0x43)

Table 62: SEQ_CONFIG register

Addr: 0x43		SEQ_CONFIG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*seq2_en*	0	R/W	This bit enables sequencer 2 for continuous measurements. Please refer to chapter 7.6.2 for more details about sequencer 2. 0: Sequencer 2 disabled 1: Sequencer 2 enabled
5:4	*seq2_sub_sample*	0	R/W	In this register the desired number of subsamples for sequencer 2 can be activated. 0: 1 subsample enabled 1: 2 subsamples enabled 2: 3 subsamples enabled 3: 4 subsamples enabled
3	*seq1_en*	0	R/W	This bit enables sequencer 1 for continuous measurements. Please refer to chapter 7.6.1 for more details about sequencer 1. 0: Sequencer 2 disabled 1: Sequencer 2 enabled
2:0	*seq1_sub_sample*	0	R/W	In this register the desired number of subsamples for sequencer 1 can be activated. 0: 1 subsample enabled 1: 2 subsamples enabled 2: 3 subsamples enabled 3: 4 subsamples enabled 4: 5 subsamples enabled 5: 6 subsamples enabled 6: 7 subsamples enabled 7: 8 subsamples enabled

8.9.5 SEQ_SAR_WAIT register (Address 0x44)

Table 63: SEQ_SAR_WAIT register

Addr: 0x44		SEQ_SAR_WAIT		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*sar_wait*	0	R/W	This register configures the SAR wait time for an activated SAR measurement function which is used for ambient light cancellation. The time is configured with the register value multiplied by 1µs. A detailed timing diagram which shows the t_{SAR_WAIT} is shown in Figure 25. 0: 0µs 1: 1µs 2: 2µs … 255: 255µs

8.9.6 SEQ_LED_INIT register (Address 0x45)

Table 64: SEQ_LED_INIT register

Addr: 0x45		SEQ_LED_INIT		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led_init*	0	R/W	This register configures the waiting time after the LEDs are turned on until the ADC modulators are switched on. A detailed timing diagram which shows t_{LED_INIT} is shown in Figure 26. The time is configured with the register value multiplied by 1µs. 0: 0µs 1: 1µs 2: 2µs … 255: 255µs

8.9.7 SEQ_FREQL register (Address 0x46)

Table 65: SEQ_FREQL register

Addr: 0x46		SEQ_FREQL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*seq_freq[7:0]*	0	R/W	This is the lower 8-bit configuration register for the sequencer sample period. Please find the calculation formulas for sequencer sample rate and period time below where n represents the full 16-bit *seq_freq[15:0]* register value which is split into two 8-bit registers **SEQ_FREQL** and **SEQ_FREQH**. $T_{SEQ} = (n+1) * 31.25\ \mu s$ $f_{SEQ} = \frac{1}{n+1} * 31.25\ \mu s; n > 0$

8.9.8 SEQ_FREQH register (Address 0x47)

Table 66: SEQ_FREQH register

Addr: 0x47		SEQ_FREQH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*seq_freq[15:8]*	0	R/W	This is the higher 8-bit configuration register for the sequencer sample period. Please find the calculation formulas for sequencer sample rate and period time below where n represents the full 16-bit *seq_freq[15:0]* register value which is split into two 8-bit registers **SEQ_FREQL** and **SEQ_FREQH**. $T_{SEQ} = (n+1) * 31.25\ \mu s$ $f_{SEQ} = \frac{1}{n+1} * 31.25\ \mu s; n > 0$

8.9.9 SEQ1_FREQDIVL register (Address 0x48)

Table 67: SEQ1_FREQDIVL register

Addr: 0x48		SEQ1_FREQDIVL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*seq1_freqdiv[7:0]*	0	R/W	This is the lower 8-bit frequency divider registers for sequencer 1 sample period. Please find the calculation formulas for sequencer 1 sample rate and period time below where n represents the full 16-bit *seq1_freqdiv[15:0]* register value which is split into two 8-bit registers **SEQ1_FREQDIVL** and **SEQ1_FREQDIVH**. In order to get a better understanding of the clock generation unit Figure 19 provides and overview of the clock tree. $T_{SEQ1} = (n+1) * T_{SEQ}$ $f_{SEQ1} = \frac{f_{SEQ}}{n+1}$

8.9.10 SEQ1_FREQDIVH register (Address 0x49)

Table 68: SEQ1_FREQDIVH register

Addr: 0x49		SEQ1_FREQDIVH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*seq1_freqdiv[15:8]*	0	R/W	This is the higher 8-bit frequency divider registers for sequencer 1 sample period. Please find the calculation formulas for sequencer 1 sample rate and period time below where n represents the full 16-bit *seq1_freqdiv[15:0]* register value which is split into two 8-bit registers **SEQ1_FREQDIVL** and **SEQ1_FREQDIVH**. In order to get a better understanding of the clock generation unit Figure 19 provides and overview of the clock tree. $T_{SEQ1} = (n+1) * T_{SEQ}$ $f_{SEQ1} = \frac{f_{SEQ}}{n+1}$

8.9.11 SEQ2_FREQDIVL register (Address 0x4A)

Table 69: SEQ2_FREQDIVL register

Addr: 0x4A		SEQ2_FREQDIVL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*seq2_freqdiv[7:0]*	0	R/W	This is the lower 8-bit frequency divider registers for sequencer 2 sample period. Please find the calculation formulas for sequencer 2 sample rate and period time below where n represents the full 16-bit *seq2_freqdiv[15:0]* register value which is split into two 8 bit registers **SEQ2_FREQDIVL** and **SEQ2_FREQDIVH**. In order to get a better understanding of the clock generation unit Figure 19 provides and overview of the clock tree. $T_{SEQ2} = (n+1) * T_{SEQ}$ $f_{SEQ2} = \frac{f_{SEQ}}{n+1}$

8.9.12 SEQ2_FREQDIVH register (Address 0x4B)

Table 70: SEQ2_FREQDIVH register

Addr: 0x4B		SEQ2_FREQDIVH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*seq2_freqdiv[15:8]*	0	R/W	This is the higher 8-bit frequency divider registers for sequencer 2 sample period. Please find the calculation formulas for sequencer 2 sample rate and period time below where n represents the full 16-bit *seq2_freqdiv[15:0]* register value which is split into two 8-bit registers **SEQ2_FREQDIVL** and **SEQ2_FREQDIVH**. In order to get a better understanding of the clock generation unit Figure 19 provides and overview of the clock tree. $T_{SEQ2} = (n+1) * T_{SEQ}$ $f_{SEQ2} = \frac{f_{SEQ}}{n+1}$

8.9.13 MOD1_SEQ1_SUB_EN register (Address 0x4C)

Table 71: MOD1_SEQ1_SUB_EN register

Addr: 0x4C		MOD1_SEQ1_SUB_EN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*mod1_seq1_sub_en*	0	R/W	This 8-bit register enables ADC modulator 1 subsamples for Sequencer 1. Each bit represents one subsample whereas the LSB represents subsample 1. The MSB of this register represents subsample number eight. Please refer also to Figure 20 for a graphical overview of sequencer 1 subsample structure. 0000 0001: Subsample 1 enabled 0000 0011: Subsample 1 and 2 enabled 0000 0111: Subsample 1, 2 and 3 enabled … 1111 1111: All eight subsamples enabled

8.9.14 MOD1_SEQ2_SUB_EN register (Address 0x4D)

Table 72: MOD1_SEQ2_SUB_EN register

Addr: 0x4D		MOD1_SEQ2_SUB_EN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3:0	*mod1_seq2_sub_en*	0	R/W	This 4-bit register enables ADC modulator 1 subsamples for Sequencer 2. Each bit represents one subsample whereas the LSB represents subsample 1. The MSB of this register represents subsample number four. Please refer also to Figure 21 for a graphical overview of sequencer 2 subsample structure. 0001: Subsample 1 enabled 0011: Subsample 1 and 2 enabled 0111: Subsample 1, 2 and 3 enabled 1111: All four subsamples enabled

8.9.15 MOD2_SEQ1_SUB_EN register (Address 0x4E)

Table 73: MOD2_SEQ1_SUB_EN register

Addr: 0x4E		MOD2_SEQ1_SUB_EN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*mod2_seq1_sub_en*	0	R/W	This 8-bit register enables ADC modulator 2 subsamples for Sequencer 1. Each bit represents one subsample whereas the LSB represents subsample 1. The MSB of this register represents subsample number eight. Please refer also to Figure 20 for a graphical overview of sequencer 1 subsample structure. 0000 0001: Subsample 1 enabled 0000 0011: Subsample 1 and 2 enabled 0000 0111: Subsample 1, 2 and 3 enabled … 1111 1111: All eight subsamples enabled

8.9.16 MOD2_SEQ2_SUB_EN register (Address 0x4F)

Table 74: MOD2_SEQ2_SUB_EN register

Addr: 0x4F		MOD2_SEQ2_SUB_EN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3:0	*mod2_seq2_sub_en*	0	R/W	This 4-bit register enables ADC modulator 2 subsamples for Sequencer 2. Each bit represents one subsample whereas the LSB represents subsample 1. The MSB of this register represents subsample number four. Please refer also to Figure 21 for a graphical overview of sequencer 2 subsample structure. 0001: Subsample 1 enabled 0011: Subsample 1 and 2 enabled 0111: Subsample 1, 2 and 3 enabled 1111: All four subsamples enabled

8.9.17 SEQ1_MODE_A register (Address 0x50)

Table 75: SEQ1_MODE_A register

Addr: 0x50		SEQ1_MODE_A		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*seq1_sub1_mode*	0	R/W	This register configures for sequencer 1 the measurement mode for subsample 1. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement
5:4	*seq1_sub2_mode*	0	R/W	This register configures for sequencer 1 the measurement mode for subsample 2. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement
3:2	*seq1_sub3_mode*	0	R/W	This register configures for sequencer 1 the measurement mode for subsample 3. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement
1:0	*seq1_sub4_mode*	0	R/W	This register configures for sequencer 1 the measurement mode for subsample 4. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement

8.9.18 SEQ1_MODE_B register (Address 0x51)

Table 76: SEQ1_MODE_B register

Addr: 0x51		SEQ1_MODE_B		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*seq1_sub5_mode*	0	R/W	This register configures for sequencer 1 the measurement mode for subsample 5. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement
5:4	*seq1_sub6_mode*	0	R/W	This register configures for sequencer 1 the measurement mode for subsample 6. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement
3:2	*seq1_sub7_mode*	0	R/W	This register configures for sequencer 1 the measurement mode for subsample 7. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement
1:0	*seq1_sub8_mode*	0	R/W	This register configures for sequencer 1 the measurement mode for subsample 8. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement

8.9.19 SEQ2_MODE register (Address 0x52)

Table 77: SEQ2_MODE register

Addr: 0x52		SEQ2_MODE		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*seq2_sub1_mode*	0	R/W	This register configures for sequencer 2 the measurement mode for subsample 1. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement
5:4	*seq2_sub2_mode*	0	R/W	This register configures for sequencer 2 the measurement mode for subsample 2. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement
3:2	*seq2_sub3_mode*	0	R/W	This register configures for sequencer 2 the measurement mode for subsample 3. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement
1:0	*seq2_sub4_mode*	0	R/W	This register configures for sequencer 2 the measurement mode for subsample 4. Please refer to chapter 7.6.3 and 7.6.4 for a detailed description of each measurement mode. 00: Single Measurement 01: Double Measurement 10: Tripple Measurement 11: SAR Single Measurement

8.10 Sequencer subsample configuration

8.10.1 PD_SEQ1_SUB1 register (Address 0x53)

Table 78: PD_SEQ1_SUB1 register

Addr: 0x53		PD_SEQ1_SUB1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq1_sub1_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 1 for subsample 1. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3	*mod2_seq1_sub1_pdsel*	0	R/W	This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 1 for subsample 1. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 1 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2

Addr: 0x53	PD_SEQ1_SUB1	
2:0		Depending on register bit *mod2_seq1_sub1_pdsel[3]* the register bits *mod2_seq1_sub1_pdsel[2:0]* support a different function. If *mod2_seq1_sub1_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 1 for subsample 1: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq1_sub1_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 1 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.2 PD_SEQ1_SUB2 register (Address 0x54)

Table 79: PD_SEQ1_SUB2 register

Addr: 0x54		PD_SEQ1_SUB2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq1_sub2_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 1 for subsample 2. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 1 for subsample 2. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 2 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq1_sub2_pdsel*	0	R/W	Depending on register bit *mod2_seq1_sub2_pdsel[3]* the register bits *mod2_seq1_sub2_pdsel[2:0]* support a different function. If *mod2_seq1_sub2_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 1 for subsample 2: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq1_sub2_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 2 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.3 PD_SEQ1_SUB3 register (Address 0x55)

Table 80: PD_SEQ1_SUB3 register

Addr: 0x55		PD_SEQ1_SUB3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq1_sub3_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 1 for subsample 3. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 1 for subsample 3. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 3 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq1_sub3_pdsel*	0	R/W	Depending on register bit *mod2_seq1_sub3_pdsel[3]* the register bits *mod2_seq1_sub3_pdsel[2:0]* support a different function. If *mod2_seq1_sub3_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 1 for subsample 3: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq1_sub3_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 3 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.4 PD_SEQ1_SUB4 register (Address 0x56)

Table 81: PD_SEQ1_SUB4 register

Addr: 0x56		PD_SEQ1_SUB4		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq1_sub4_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 1 for subsample 4. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 1 for subsample 4. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 4 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq1_sub4_pdsel*	0	R/W	Depending on register bit *mod2_seq1_sub4_pdsel[3]* the register bits *mod2_seq1_sub4_pdsel[2:0]* support a different function. If *mod2_seq1_sub4_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 1 for subsample 4: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq1_sub4_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 4 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.5 PD_SEQ1_SUB5 register (Address 0x57)

Table 82: PD_SEQ1_SUB5 register

Addr: 0x57		PD_SEQ1_SUB5		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq1_sub5_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 1 for subsample 5. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 1 for subsample 5. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 5 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq1_sub5_pdsel*	0	R/W	Depending on register bit *mod2_seq1_sub5_pdsel[3]* the register bits *mod2_seq1_sub5_pdsel[2:0]* support a different function. If *mod2_seq1_sub5_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 1 for subsample 5: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq1_sub5_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 5 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.6 PD_SEQ1_SUB6 register (Address 0x58)

Table 83: PD_SEQ1_SUB6 register

Addr: 0x58		PD_SEQ1_SUB6		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq1_sub6_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 1 for subsample 6. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 1 for subsample 6. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 6 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq1_sub6_pdsel*	0	R/W	Depending on register bit *mod2_seq1_sub6_pdsel[3]* the register bits *mod2_seq1_sub6_pdsel[2:0]* support a different function. If *mod2_seq1_sub6_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 1 for subsample 6: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq1_sub6_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 6 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.7 PD_SEQ1_SUB7 register (Address 0x59)

Table 84: PD_SEQ1_SUB7 register

Addr: 0x59		PD_SEQ1_SUB7		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq1_sub7_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 1 for subsample 7. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 1 for subsample 7. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 7 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq1_sub7_pdsel*	0	R/W	Depending on register bit *mod2_seq1_sub7_pdsel[3]* the register bits *mod2_seq1_sub7_pdsel[2:0]* support a different function. If *mod2_seq1_sub7_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 1 for subsample 7: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq1_sub7_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 7 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.8 PD_SEQ1_SUB8 register (Address 0x5A)

Table 85: PD_SEQ1_SUB8 register

Addr: 0x5A		PD_SEQ1_SUB8		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq1_sub8_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 1 for subsample 8. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 1 for subsample 8. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 8 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq1_sub8_pdsel*	0	R/W	Depending on register bit *mod2_seq1_sub8_pdsel[3]* the register bits *mod2_seq1_sub8_pdsel[2:0]* support a different function. If *mod2_seq1_sub8_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 1 for subsample 8: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq1_sub8_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 1 for subsample 8 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.9 PD_SEQ2_SUB1 register (Address 0x5B)

Table 86: PD_SEQ2_SUB1 register

Addr: 0x5B		PD_SEQ2_SUB1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq2_sub1_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 2 for subsample 1. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 2 for subsample 1. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 2 for subsample 1 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq2_sub1_pdsel*	0	R/W	Depending on register bit *mod2_seq2_sub1_pdsel[3]* the register bits *mod2_seq2_sub1_pdsel[2:0]* support a different function. If *mod2_seq2_sub1_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 2 for subsample 1: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq2_sub1_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 2 for subsample 1 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.10 PD_SEQ2_SUB2 register (Address 0x5C)

Table 87: PD_SEQ2_SUB2 register

Addr: 0x5C		PD_SEQ2_SUB2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq2_sub2_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 2 for subsample 2. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 2 for subsample 2. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 2 for subsample 2 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq2_sub2_pdsel*	0	R/W	Depending on register bit *mod2_seq2_sub2_pdsel[3]* the register bits *mod2_seq2_sub2_pdsel[2:0]* support a different function. If *mod2_seq2_sub2_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 2 for subsample 2: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq2_sub2_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 2 for subsample 2 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.11 PD_SEQ2_SUB3 register (Address 0x5D)

Table 88: PD_SEQ2_SUB3 register

Addr: 0x5D		PD_SEQ2_SUB3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq2_sub3_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 2 for subsample 3. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 2 for subsample 3. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 2 for subsample 3 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq2_sub3_pdsel*	0	R/W	Depending on register bit *mod2_seq2_sub3_pdsel[3]* the register bits *mod2_seq2_sub3_pdsel[2:0]* support a different function. If *mod2_seq2_sub3_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 2 for subsample 3: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq2_sub3_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 2 for subsample 3 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.10.12 PD_SEQ2_SUB4 register (Address 0x5E)

Table 89: PD_SEQ2_SUB4 register

Addr: 0x5E		PD_SEQ2_SUB4		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*mod1_seq2_sub4_pdsel*	0	R/W	This bit assigns the photodiode input for ADC modulator 1 in sequencer 2 for subsample 4. Each bit represents one photodiode input whereas the LSB represents PD1 and the MSB represents PD3 input. 001: PD1 assigned to ADC modulator 010: PD2 assigned to ADC modulator 100: PD3 assigned to ADC modulator
3				This is the input source selection bit for ADC modulator 2. If this bit is set to zero, the photodiode inputs can be assigned to modulator 2 in sequencer 2 for subsample 4. If this bit is set to one the AFE function block is connected to ADC modulator 2 in sequencer 2 for subsample 4 to measure various input sources. 0: Photodiode inputs assigned to ADC 1: AFE inputs assigned to ADC modulator 2
2:0	*mod2_seq2_sub4_pdsel*	0	R/W	Depending on register bit *mod2_seq2_sub4_pdsel[3]* the register bits *mod2_seq2_sub4_pdsel[2:0]* support a different function. If *mod2_seq2_sub4_pdsel[3]* is set to 0 the register assigns the photodiode inputs to ADC modulator 2 in sequencer 2 for subsample 4: 001: PD1 connected to ADC modulator 2 010: PD2 connected to ADC modulator 2 100: PD3 connected to ADC modulator 2 If *mod2_seq2_sub4_pdsel[3]* is set to 1 the AFE function block is connected to ADC modulator 2 in sequencer 2 for subsample 4 and allows for the following input configuration: 000: LED 1 001: LED 2 010: LED 3 011: VCSELS 100: VCSELA 101: PGND 110: VDD 111: ITEMP

8.11 Sequencer down sampler configuration

8.11.1 SEQ1_SINC_CFGA register (Address 0x61)

Table 90: SEQ1_SINC_CFGA register

Addr: 0x61		SEQ1_SINC_CFGA		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*seq1_sinc_ovs*	0	R/W	This register controls the ADC oversampling filter of sequencer 1 whose input signal is the decimation filter output of the ADC modulator. Please refer to Figure 17 which provides an overview of the signal processing flow including the oversampling filter. The oversampling ratio is calculated with the numerical register value of *seq1_sinc_ovs* register to the power of two. Please find the calculation formula below: $OVS_{RATIO} = 2^{seq1\_sinc\_ovs}$
4:2	*seq1_sinc_dec*	0	R/W	This register controls the ADC decimation ratio of sequencer 1 which is applicable for both ADC modulators. Please refer to Figure 17 which provides an overview of the signal processing flow including the decimation filters. 0: Decimation factor 16 1: Decimation factor 32 2: Decimation factor 64 3: Decimation factor 128 4: Decimation factor 256

8.11.2 SEQ1_SINC_CFGB register (Address 0x62)

Table 91: SEQ1_SINC_CFGB register

Addr: 0x62		SEQ1_SINC_CFGB		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:3	*seq1_os_delay*	0	R/W	In case embedded oversampling filter function is enabled this register allows to configure a delay before data from the SINC down sampler is used for the oversampling calculation for sequencer 1. Please refer also to Figure 26 which shows the t_{OS} timing related to this register. 000: No oversampling delay 001: 1µs delay 010: 2µs delay … 111: 7µs delay
1	*seq1_sel_order*	0	R/W	This register controls the filter order of sequencer one down sampling SINC filter. Please refer to Figure 17 which provides an overview of the signal processing flow including the filter order selection block. 0: 4^{th} order down sampling filter enabled 1: 5^{th} order down sampling filter enabled
0	*seq1_filter_mode*	1	R/W	This register bit controls the filter operation mode of sequencer one down sampling filter. Default filter operation mode is a CIC filter which can be reconfigured to integrator filter mode by setting *seq1_filter_mode* bit. 0: Integrator filter operation mode 1: CIC filter operation mode

8.11.3 SEQ1_SINC_CFGC register (Address 0x63)

Table 92: SEQ1_SINC_CFGC register

Addr: 0x63		SEQ1_SINC_CFGC		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*seq1_start_delay*	0	R/W	This register controls the start delay after the ADC modulator reset is released and modulator data is supplied to the SINC down sampling filter block. Please refer to Figure 26 which shows the t_{SD} timing related to this register for sequencer 1. 0: No oversampling delay 1: 1µs start delay 2: 2µs start delay … 255: 255µs start delay

8.11.4 SEQ2_SINC_CFGA register (Address 0x64)

Table 93: SEQ2_SINC_CFGA register

Addr: 0x64		SEQ2_SINC_CFGA		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*seq2_sinc_ovs*	0	R/W	This register controls the ADC oversampling filter of sequencer 2 whose input signal is the decimation filter output of the ADC modulator. Please refer to Figure 17 which provides an overview of the signal processing flow including the oversampling filter. The oversampling ratio is calculated with the numerical register value of *seq2_sinc_ovs* register to the power of two. Please find the calculation formula below: $OVS_{RATIO} = 2^{seq2\_sinc\_ovs}$
4:2	*seq2_sinc_dec*	0	R/W	This register controls the ADC decimation ratio of sequencer 2 which is applicable for both ADC modulators. Please refer to Figure 17 which provides an overview of the signal processing flow including the decimation filters. 0: Decimation factor 16 1: Decimation factor 32 2: Decimation factor 64 3: Decimation factor 128 4: Decimation factor 256

8.11.5 SEQ2_SINC_CFGB register (Address 0x65)

Table 94: SEQ2_SINC_CFGB register

Addr: 0x65		SEQ2_SINC_CFGB		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:3	*seq2_os_delay*	0	R/W	In case embedded oversampling filter function is enabled this register allows to configure a delay before data from the SINC down sampler is used for the oversampling calculation for sequencer 2. Please refer also to Figure 26 which shows the t_{OS} timing related to this register. 000: No oversampling delay 001: 1µs delay 010: 2µs delay … 111: 7µs delay
1	*seq2_sel_order*	0	R/W	This register controls the filter order of sequencer 2 down sampling SINC filter. Please refer to Figure 17 which provides an overview of the signal processing flow including the filter order selection block. 0: 4^{th} order down sampling filter enabled 1: 5^{th} order down sampling filter enabled
0	*seq2_filter_mode*	1	R/W	This register bit controls the filter operation mode of sequencer 2 down sampling filter. Default filter operation mode is a CIC filter which can be reconfigured to integrator filter mode by setting *seq1_filter_mode* bit. 0: Integrator filter operation mode 1: CIC filter operation mode

8.11.6 SEQ2_SINC_CFGC register (Address 0x66)

Table 95: SEQ2_SINC_CFGC register

Addr: 0x66		SEQ2_SINC_CFGC		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*seq2_start_delay*	0	R/W	This register controls the start delay after the ADC modulator reset is released and modulator data is supplied to the SINC down sampling filter block. Please refer to Figure 26 which shows the t_{SD} timing related to this register for sequencer 2. 0: No oversampling delay 1: 1µs start delay 2: 2µs start delay … 255: 255µs start delay

8.12 AOC

All registers in this chapter are ambient light compensation current control registers for both sequencers, modulators and subsamples. The LSB current value for each register is calculated by the defined offset DAC full scale range divided by 255. Both DACs support a wide full-scale range starting with 1µA full scale range going up to 128µA full scale range which is controlled via 3-bit registers *mod1_ios_fs* and *mod2_ios_fs* for both ADC modulator inputs.

8.12.1 AOC_MOD1_SEQ1_SUB1 register (Address 0x70)

Table 96: AOC_MOD1_SEQ1_SUB1 register

Addr: 0x70		AOC_MOD1_SEQ1_SUB1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq1_sub1*	0	R/W	This is the ambient light compensation offset current control register for subsample 1 in sequencer 1 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.2 AOC_MOD1_SEQ1_SUB2 register (Address 0x71)

Table 97: AOC_MOD1_SEQ1_SUB2 register

Addr: 0x71		AOC_MOD1_SEQ1_SUB2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq1_sub2*	0	R/W	This is the ambient light compensation offset current control register for subsample 2 in sequencer 1 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.3 AOC_MOD1_SEQ1_SUB3 register (Address 0x72)

Table 98: AOC_MOD1_SEQ1_SUB3 register

Addr: 0x72		AOC_MOD1_SEQ1_SUB3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq1_sub3*	0	R/W	This is the ambient light compensation offset current control register for subsample 3 in sequencer 1 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.4 AOC_MOD1_SEQ1_SUB4 register (Address 0x73)

Table 99: AOC_MOD1_SEQ1_SUB4 register

Addr: 0x73		AOC_MOD1_SEQ1_SUB4		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq1_sub4*	0	R/W	This is the ambient light compensation offset current control register for subsample 4 in sequencer 1 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.5 AOC_MOD1_SEQ1_SUB5 register (Address 0x74)

Table 100: AOC_MOD1_SEQ1_SUB5 register

Addr: 0x74		AOC_MOD1_SEQ1_SUB5		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq1_sub5*	0	R/W	This is the ambient light compensation offset current control register for subsample 5 in sequencer 1 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.6 AOC_MOD1_SEQ1_SUB6 register (Address 0x75)

Table 101: AOC_MOD1_SEQ1_SUB6 register

Addr: 0x75		AOC_MOD1_SEQ1_SUB6		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq1_sub6*	0	R/W	This is the ambient light compensation offset current control register for subsample 6 in sequencer 1 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.7 AOC_MOD1_SEQ1_SUB7 register (Address 0x76)

Table 102: AOC_MOD1_SEQ1_SUB7 register

Addr: 0x76		AOC_MOD1_SEQ1_SUB7		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq1_sub7*	0	R/W	This is the ambient light compensation offset current control register for subsample 7 in sequencer 1 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.8 AOC_MOD1_SEQ1_SUB8 register (Address 0x77)

Table 103: AOC_MOD1_SEQ1_SUB8 register

Addr: 0x77		AOC_MOD1_SEQ1_SUB8		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq1_sub8*	0	R/W	This is the ambient light compensation offset current control register for subsample 8 in sequencer 1 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.9 AOC_MOD1_SEQ2_SUB1 register (Address 0x78)

Table 104: AOC_MOD1_SEQ2_SUB1 register

Addr: 0x78		AOC_MOD1_SEQ2_SUB1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq2_sub1*	0	R/W	This is the ambient light compensation offset current control register for subsample 1 in sequencer 2 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.10 AOC_MOD1_SEQ2_SUB2 register (Address 0x79)

Table 105: AOC_MOD1_SEQ2_SUB2 register

Addr: 0x79		AOC_MOD1_SEQ2_SUB2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq2_sub2*	0	R/W	This is the ambient light compensation offset current control register for subsample 2 in sequencer 2 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.11 AOC_MOD1_SEQ2_SUB3 register (Address 0x7A)

Table 106: AOC_MOD1_SEQ2_SUB3 register

Addr: 0x7A		AOC_MOD1_SEQ2_SUB3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq2_sub3*	0	R/W	This is the ambient light compensation offset current control register for subsample 3 in sequencer 2 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.12 AOC_MOD1_SEQ2_SUB4 register (Address 0x7B)

Table 107: AOC_MOD1_SEQ2_SUB4 register

Addr: 0x7B		AOC_MOD1_SEQ2_SUB4		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_seq2_sub4*	0	R/W	This is the ambient light compensation offset current control register for subsample 4 in sequencer 2 for ADC modulator 1. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.13 AOC_MOD2_SEQ1_SUB1 register (Address 0x7C)

Table 108: AOC_MOD2_SEQ1_SUB1 register

Addr: 0x7C		AOC_MOD2_SEQ1_SUB1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_seq1_sub1*	0	R/W	This is the ambient light compensation offset current control register for subsample 1 in sequencer 1 for ADC modulator 2. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.14 AOC_MOD2_SEQ1_SUB2 register (Address 0x7D)

Table 109: AOC_MOD2_SEQ1_SUB2 register

Addr: 0x7D		AOC_MOD2_SEQ1_SUB2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_seq1_sub2*	0	R/W	This is the ambient light compensation offset current control register for subsample 2 in sequencer 1 for ADC modulator 2. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.15 AOC_MOD2_SEQ1_SUB3 register (Address 0x7E)

Table 110: AOC_MOD2_SEQ1_SUB3 register

Addr: 0x7E		AOC_MOD2_SEQ1_SUB3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_seq1_sub3*	0	R/W	This is the ambient light compensation offset current control register for subsample 3 in sequencer 1 for ADC modulator 2. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.16 AOC_MOD2_SEQ1_SUB4 register (Address 0x7F)

Table 111: AOC_MOD2_SEQ1_SUB4 register

Addr: 0x7F		AOC_MOD2_SEQ1_SUB4		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_seq1_sub4*	0	R/W	This is the ambient light compensation offset current control register for subsample 4 in sequencer 1 for ADC modulator 2. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.17 AOC_MOD2_SEQ1_SUB5 register (Address 0x80)

Table 112: AOC_MOD2_SEQ1_SUB5 register

Addr: 0x80		AOC_MOD2_SEQ1_SUB5		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_seq1_sub5*	0	R/W	This is the ambient light compensation offset current control register for subsample 5 in sequencer 1 for ADC modulator 2. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.18 AOC_MOD2_SEQ1_SUB6 register (Address 0x81)

Table 113: AOC_MOD2_SEQ1_SUB6 register

Addr: 0x81		AOC_MOD2_SEQ1_SUB6		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_seq1_sub6*	0	R/W	This is the ambient light compensation offset current control register for subsample 6 in sequencer 1 for ADC modulator 2. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.19 AOC_MOD2_SEQ1_SUB7 register (Address 0x82)

Table 42: AOC_MOD2_SEQ1_SUB7 register

Addr: 0x82		AOC_MOD2_SEQ1_SUB7		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_seq1_sub7*	0	R/W	This is the ambient light compensation offset current control register for subsample 7 in sequencer 1 for ADC modulator 2. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.20 AOC_MOD2_SEQ1_SUB8 register (Address 0x83)

Table 114: AOC_MOD2_SEQ1_SUB8 register

Addr: 0x83		AOC_MOD2_SEQ1_SUB8		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_seq1_sub8*	0	R/W	This is the ambient light compensation offset current control register for subsample 8 in sequencer 1 for ADC modulator 2. If any of these registers is set to 0 no offset current is applied to is appendant ADC modulator.

8.12.21 AOC_LEDOFF register (Address 0x84)

Table 115: AOC_LEDOFF register

Addr: 0x84		AOC_LEDOFF		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_ledoff*	0	R/W	This is the ambient light compensation offset current control register for double and triple sampling during LED off phase.

8.12.22 AOC_CFG register (Address 0x85)

Table 116: AOC_CFG register

Addr: 0x85		AOC_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*dis_ledoff*	0	R/W	This register disables the utilization of the *aos_ledoff* ambient light compensation offset current register value to be used during the LED off measurement phase for double and triple sampling measurement mode. Instead, the photodiode offset value of the subsample is used during LED off phase for double and triple measurement. 0: Register *aoc_ledoff* value used during LED off phase for double and triple sampling 1: Register *aoc_ledoff* not used during LED off phase for double and triple sampling
2:0	*aoc_ovs*	0	R/W	This register controls the AOC ADC oversampling filter function whose input signal is the decimation filter output of the ADC modulator. The oversampling ratio is calculated with the numerical register value of *aoc_ovs* register to the power of two. Please find the calculation formula below: $OVS_{RATIO} = 2^{\text{aoc\_ovs}}$

8.12.23 AOC_MOD1_THH register (Address 0x86)

Table 117: AOC_MOD1_THH register

Addr: 0x86		AOC_MOD1_THH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_thh*	255	R/W	This is the AOC high threshold register for decreasing the ambient light offset current for all subsamples for ADC modulator 1.

8.12.24 AOC_MOD1_THL register (Address 0x87)

Table 118: AOC_MOD1_THL register

Addr: 0x87		AOC_MOD1_THL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod1_thl*	255	R/W	This is the AOC low threshold register for increasing the ambient light offset current for all subsamples for ADC modulator 1.

8.12.25 AOC_MOD2_THH register (Address 0x88)

Table 119: AOC_MOD2_THH register

Addr: 0x88		AOC_MOD2_THH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_thh*	255	R/W	This is the AOC high threshold register for decreasing the ambient light offset current for all subsamples for ADC modulator 2.

8.12.26 AOC_MOD2_THL register (Address 0x89)

Table 120: AOC_MOD2_THL register

Addr: 0x89		AOC_MOD2_THL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*aoc_mod2_thl*	255	R/W	This is the AOC low threshold register for increasing the ambient light offset current for all subsamples for ADC modulator 2.

8.12.27 AOC_SAR_TRES register (Address 0x8A)

Table 121: AOC_SAR_TRES register

Addr: 0x8A		AOC_SAR_TRES		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*sar_thres*	128	R/W	This is the AOC SAR threshold register which is used for all subsamples. This 8-bit register represents the threshold of the most significant bits of a 20-bit ADC reading for the SAR algorithms to find the correct DAC offset current setting to channel ambient light via the integrated current DAC. Please refer to chapter 7.6.4.3 for more information about regarding the SAR AOC function.

8.12.28 MOD1_SEQ1_AOC_EN register (Address 0x8B)

Table 122: MOD1_SEQ1_AOC_EN register

Addr: 0x8B		MOD1_SEQ1_AOC_EN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*mod1_seq1_aoc_en*	0	R/W	This register enables the AOC function for sequencer 1 and ADC modulator 1. Each bit of the register represents one subsample whereas the LSB is assigned to subsample 1 and the MSB is assigned to subsample 8. 0000 0001: AOC subsample 1 enabled 0000 0010: AOC subsample 2 enabled 0000 0011: AOC subsample 1 and 2 enabled … 1111 1111: AOC for all 8 subsamples enabled

8.12.29 MOD2_SEQ1_AOC_EN register (Address 0x8C)

Table 123: MOD2_SEQ1_AOC_EN register

Addr: 0x8C		MOD2_SEQ1_AOC_EN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1:0	*mod2_seq1_aoc_en*	0	R/W	This register enables the AOC function for sequencer 1 and ADC modulator 2. Each bit of the register represents one subsample whereas the LSB is assigned to subsample 1 and the MSB is assigned to subsample 8. 01: AOC subsample 1 enabled 10: AOC subsample 2 enabled 11: AOC for subsample 1 and 2 enabled

8.13 Proximity

8.13.1 PROX_CFG register (Address 0x98)

Table 124: PROX_CFG register

Addr: 0x98		PROX_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*prox_en*	0	R/W	This bit enables the build in proximity function of AS7150. 0: Proximity function disabled 1: Proximity function enabled
1:0	*prox_sub*	0	R/W	This register assigns the subsample which is used for the proximity detection function. The proximity function is always assigned to ADC modulator 1 in combination with sequencer 2. 00: Proximity function assigned to subsample 1 01: Proximity function assigned to subsample 2 10: Proximity function assigned to subsample 3 11: Proximity function assigned to subsample 4

8.13.2 PROX_OVS register (Address 0x99)

Table 125: PROX_OVS register

Addr: 0x99		PROX_OVS		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*prox_on_ovs*	0	R/W	This register controls the proximity oversampling function of the higher proximity threshold. In its default configuration the oversampling is disabled. If the register value is greater than zero the numeric value of the register defines the number of proximity measurements the ADC reading must be above/below the **PROX_THH** register threshold in order to trigger a proximity interrupt. Please refer to chapter 7.7 and Figure 31 which illustrates the proximity oversampling function with its related control registers and a dedicated timing diagram. 0: Oversampling disabled 1: Single oversampling 2: Double oversampling 3: Tripple oversampling … 7: 7 times oversampling
2:0	*prox_off_ovs*	0	R/W	This register controls the proximity oversampling function of the lower proximity threshold. In its default configuration the oversampling is disabled. If the register value is greater than zero the numeric value of the register defines the number of proximity measurements the ADC reading must be below/above the **PROX_THL** register threshold in order to trigger a proximity interrupt. Please refer to chapter 7.7 and Figure 31 which illustrates the proximity oversampling function with its related control registers and a dedicated timing diagram. 0: Oversampling disabled 1: Single oversampling 2: Double oversampling 3: Tripple oversampling … 7: 7 times oversampling

8.13.3 PROX_THH_L register (Address 0x9A)

Table 126: PROX_THH_L register

Addr: 0x99		PROX_THH_L		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*prox_thh[7:0]*	0	R/W	This is the lower 8-bit proximity threshold register for the proximity high threshold. Please refer to chapter 7.7 and Figure 31 which shows the control registers and a dedicated timing diagram.

8.13.4 PROX_THH_H register (Address 0x9B)

Table 127: PROX_THH_H register

Addr: 0x9B		PROX_THH_H		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*prox_thh[15:8]*	0	R/W	This is the higher 8-bit proximity threshold register for the proximity high threshold. Please refer to chapter 7.7 and Figure 31 which shows the control registers and a dedicated timing diagram.

8.13.5 PROX_THL_L register (Address 0x9C)

Table 128: PROX_THL_L register

Addr: 0x9C		PROX_THL_L		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*prox_thl[7:0]*	0	R/W	This is the lower 8-bit proximity threshold register for the proximity low threshold. Please refer to chapter 7.7 and Figure 31 which shows the control registers and a dedicated timing diagram.

8.13.6 PROX_THL_H register (Address 0x9D)

Table 129: PROX_THL_H register

Addr: 0x9D		PROX_THL_H		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*prox_thl[15:8]*	0	R/W	This is the higher 8-bit proximity threshold register for the proximity low threshold. Please refer to chapter 7.7 and Figure 31 which shows the control registers and a dedicated timing diagram.

8.14 Standby

8.14.1 STANDBY_ON register (Address 0xA0)

Table 130: STANDBY_ON register

Addr: 0xA0		STANDBY_ON		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:0	*stby_en_on*	0	R/W	This is the standby enable register. Each bit of this 7-bit register controls a dedicated power block of AS7150 whereas the LSB controls Standby Enable 1 signal and bit 6 Standby Enable 7 signal. Please refer to chapter 7.10 and Figure 41 for more detailed information about the standby mode. 000 0001: Standby Enable 1 control enabled 000 0010: Standby Enable 2 control enabled … 111 1111: All 7 standby enable control signals enabled

8.14.2 STANDBY_EN1 register (Address 0xA1)

Table 131: STANDBY_EN1 register

Addr: 0xA1		STANDBY_EN1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en1_time*	4	R/W	This register controls the standby timing for Standby Enable 1 block. Please refer to Figure 41 for a detailed timing diagram of $t_{STANDBY\_1}$. The standby wait time $t_{STANDBY\_1}$ is calculated with the following formula: $t_{STANDBY\_1\_OSC} = stby\_en1\_time * 31.25\ \mu s$ The timing diagram shown in Figure 41 shows that the Standby Enable 1 block controls also the PLL block which has one clock cycle delay to the oscillator block resulting in the following formula for the PLL start block: $t_{STANDBY\_1\_OSC} = (stby\_en1\_time + 1) * 31.25\ \mu s$

8.14.3 STANDBY_EN2 register (Address 0xA2)

Table 132: STANDBY_EN2 register

Addr: 0xA2		STANDBY_EN2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en2_time*	2	R/W	This register controls the standby timing for Standby Enable 2 block. Please refer to Figure 41 for a detailed timing diagram of $t_{STANDBY\_2}$. The standby wait time $t_{STANDBY\_2}$ is calculated with the following formula: $t_{STANDBY\_2} = stby\_en2\_time * 31.25\ \mu s$

8.14.4 STANDBY_EN3 register (Address 0xA3)

Table 133: STANDBY_EN3 register

Addr: 0xA3		STANDBY_EN3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en3_time*	4	R/W	This register controls the standby timing for Standby Enable 3 block. Please refer to Figure 41 for a detailed timing diagram of $t_{STANDBY\_3}$. The standby wait time $t_{STANDBY\_3}$ is calculated with the following formula: $t_{STANDBY\_3} = stby\_en3\_time * 31.25\ \mu s$

8.14.5 STANDBY_EN4 register (Address 0xA4)

Table 134: STANDBY_EN4 register

Addr: 0xA4		STANDBY_EN4		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en4_time*	4	R/W	This register controls the standby timing for Standby Enable 4 block. Please refer to Figure 41 for a detailed timing diagram of $t_{STANDBY\_4}$. The standby wait time $t_{STANDBY\_4}$ is calculated with the following formula: $t_{STANDBY\_4} = stby\_en4\_time * 31.25\ \mu s$

8.14.6 STANDBY_EN5 register (Address 0xA5)

Table 135: STANDBY_EN5 register

Addr: 0xA5		STANDBY_EN5		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en5_time*	4	R/W	This register controls the standby timing for Standby Enable 5 block. Please refer to Figure 41 for a detailed timing diagram of $t_{STANDBY\_5}$. The standby wait time $t_{STANDBY\_5}$ is calculated with the following formula: $t_{STANDBY\_5} = stby\_en5\_time * 31.25\ \mu s$

8.14.7 STANDBY_EN6 register (Address 0xA6)

Table 136: STANDBY_EN6 register

Addr: 0xA6		STANDBY_EN6		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en6_time1*	0	R/W	This register controls the standby timing for Standby Enable 6 block. Once this register is configured to a value great than zero $t_{STANDBY\_6}$ is calculated with the following formula: $t_{STANDBY\_6} = (stby\_en6\_time1 + 1) * 31.25\ \mu s$ The register value of *stby_en6_time2* register is ignored in case *stby_en6_time1 is greater zero* and does not contribute to the timing calculation of $t_{STANDBY\_6}$. However, if register *stby_en6_time1* is set to zero the timing for Standby Enable 6 block is controlled via register *stby_en6_time2* register.
4:0	*stby_en6_time2*	16	R/W	In case *stby_en6_time1* register is set to zero this register takes over timing control of Standby Enable block 6. The timing for $t_{STANDBY\_6}$ is then calculated with the following formula: $t_{STANDBY\_6} = stby\_en6\_time2 * 1\ \mu s$

8.14.8 STANDBY_EN7 register (Address 0xA7)

Table 137: STANDBY_EN7 register

Addr: 0xA7		STANDBY_EN7		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en7_time1*	0	R/W	This register controls the standby timing for Standby Enable 7 block. Once this register is configured to a value great than zero $t_{STANDBY\_7}$ is calculated with the following formula: $t_{STANDBY\_7} = (stby\_en7\_time1 + 1) * 31.25\ \mu s$ The register value of *stby_en7_time2* register is ignored in case *stby_en7_time1 is greater zero* and does not contribute to the timing calculation of $t_{STANDBY\_7}$. However, if register *stby_en7_time1* is set to zero the timing for Standby Enable 7 block is controlled via register *stby_en7_time2* register.
4:0	*stby_en7_time2*	16	R/W	In case *stby_en7_time1* register is set to zero this register takes over timing control of Standby Enable block 7. The timing for $t_{STANDBY\_7}$ is then calculated with the following formula: $t_{STANDBY\_7} = stby\_en7\_time2 * 1\ \mu s$

8.15 FIFO

8.15.1 FIFO_THRESHOLD register (Address 0xD0)

Table 138: FIFO_THRESHOLD register

Addr: 0xD0		FIFO_THRESHOLD		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*fifo_threshold[7:0]*	0	R/W	This is the lower 8-bit FIFO threshold register.

8.15.2 FIFO_CTRL register (Address 0xD1)

Table 139: FIFO_CTRL register

Addr: 0xD1		FIFO_CTRL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*fifo_clear*	0	PUSH	This self-clearing bit deletes the FIFO on chip memory.
3	*sar_data_en*	0	R/W	In order to reduce I²C traffic, especially when high sample rates are used in the system, this bit allows to copy the 4-bit SAR data to the least significant bits of the ADC data stream. This means from the 20 transferred ADC data bits the bits 0 to 3 are overwritten with SAR data. With this feature you avoid reading an additional data word to get the SAR information. 0: SAR copy function to ADC data stream disabled. 1: SAR copy function to ADC data stream enabled
0	*fifo_threshold[8]*	0	R/W	This is MSB of the 9-bit FIFO threshold register.

8.15.3 FIFO_LEVEL0 register (Address 0xFB)

Table 140: FIFO_LEVEL0 register

Addr: 0xFB		FIFO_LEVEL0		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*fifo_level[7:0]*	0	RO	This is the lower 8-bit FIFO level register.

8.15.4 FIFO_LEVEL1 register (Address 0xFC)

Table 141: FIFO_LEVEL1 register

Addr: 0xFC		FIFO_LEVEL1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2	*fifo_overflow*	0	RO	This is the FIFO overflow status bit. 0: No FIFO overflow 1: FIFO overflow
1:0	*fifo_level[9:8]*	0	RO	This is the upper 2- bit FIFO level register.

8.15.5 FIFOL register (Address 0xFD)

The FIFO can be read with individual read accesses (three consecutive I²C addresses for a FIFO entry) or with burst read accesses (n * 3 bytes for n FIFO entry). By reading FIFOL, a FIFO entry is read from the FIFO and the FIFO level is reduced. If you read beyond the end of the FIFO, the last FIFO entry will be repeated. There is no underflow flag; this is not an error condition. The FIFO level is 512 entries.

Table 142: FIFOL register

Addr: 0xFD		FIFOL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:4		0	PUSHPOP	These are the lower 4 bits of the ADC data reading.
3	*fifol*	0	PUSHPOP	This bit contains the block frame information.
2:0		0	PUSHPOP	This bit contains the data marker information. Please refer to Figure 32 for more information regarding the data marker.

8.15.6 FIFOM register (Address 0xFE)

Table 143: FIFOM register

Addr: 0xFE		FIFOM		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*fifom*	0	PUSHPOP	This is the middle data byte of the 20-bit ADC reading. On burst read the address jumps back to **FIFOL**.

8.15.7 FIFOH register (Address 0xFF)

Table 144: FIFOH register

Addr: 0xFF		FIFOH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*fifoh*	0	PUSHPOP	This is the high data byte of the 20-bit ADC reading.

8.16 Device revision

8.16.1 PRODUCT_ID (Address 0xEC)

Table 145: PRODUCT_ID register

Addr: 0xEC		PRODUCT_ID		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:3	*otp_part_id*	0	RO	This is the 5-bit part identification register of AS7150.

8.16.2 SILICON_ID (Address 0xED)

Table 146: SILICON_ID register

Addr: 0xED		SILICON_ID		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*silicon_id*	0	RO	This is the silicon identification register of AS7150.

8.16.3 REVISION (Address 0xEE)

Table 147: REVISION register

Addr: 0xEE		REVISION		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*revision*	0	RO	This is the device revision identification register of AS7150.

8.17 Status register

8.17.1 STATUS_CGBB (Address 0xF4)

Table 148: STATUS_CGBB register

Addr: 0xF4		STATUS_CGBB		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3	*pll_lock*	0	RO	This is the PLL status bit. Once the bit is one the PLL is in locked state. 0: PLL not locked 1: PLL locked
2	*clk_pll_ok*	0	RO	This is the 20 MHz PLL clock output status bit. Once the bit is one the internal 20 MHz clock is running. 0: 20 MHz clock not running 1: 20 MHz clock running
1	*lf_bgcal_ok*	0	RO	This is the status bit for the low frequency oscillator calibration cycles. 0: Low frequency calibration on going 1: Low frequency done and frequency is ok
0	*lf_bgcal_ready*	0	RO	This is the status information bit which indicates that the last low frequency calibration cycle is done. 0: Low frequency calibration on going 1: Low frequency calibration cycle done

8.17.2 STATUS_SEQ (Address 0xF5)

Table 149: STATUS_SEQ register

Addr: 0xF5		STATUS_SEQ		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1	*seq_end*	0	RO	This is the status information bit that the sequencer was stopped.
0	*seq_error*	0	RO	This is the sequencer error bit which is set if a measurement was not started because the sample frequency is too high.

8.17.3 STATUS_LED (Address 0xF6)

Table 150: STATUS_LED register

Addr: 0xF6		STATUS_LED		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2:0	*led_lowvds*	0	RO	This is the low voltage LED driver current sink status bit. Each of the three bits represents one LED input. A bit is set to one in case the configured LED current cannot be reached resulting in a low drain to source voltage at the internal LED driver current sink. 000: No low voltage condition at LED inputs 001: Low voltage condition VCSEL driver 1 010: Low voltage condition LED2 input 100: Low voltage condition LED3 input

8.17.4 STATUS_ASAT (Address 0xF7)

Table 151: STATUS_ASAT register

Addr: 0xF7		STATUS_ASAT		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:4	*mod1_asat*	0	RO	This is the analog saturation status register for ADC modulator one. As long as the modulator is working in its operating input range and there is no saturation detected all bits of this register are zero. If any of the four status bits is one the ADC modulator one has run into saturation.
3:0	*mod2_asat*	0	R0	This is the analog saturation status register for ADC modulator two. As long as the modulator is working in its operating input range and there is no saturation detected all bits of this register are zero. If any of the four status bits is one the ADC modulator one has run into saturation.

8.17.5 STATUS_VCSEL (Address 0xF8)

Table 152: STATUS_VCSEL register

Addr: 0xF8		STATUS_VCSEL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2	*vcsel_short_vss*	0	RO	This is the VCSEL safety status register for detecting a short circuit to ground. 0: No short circuit to GND detected 1: VCSEL short circuit to ground detected
1	*vcsel_short_vdd*	0	RO	This is the VCSEL safety status register for detecting a short circuit to VDD. 0: No short circuit to VDD detected 1: VCSEL short circuit to VDD detected
0	*vcsel_wd*	0	RO	This is the VCSEL safety status register for the watchdog. This bit is set to one once the VCSEL on time which is longer than the defined maximum on time is detected. 0: No VCSEL on time violation 1: VCSEL on time violation detected

8.17.6 STATUS_PROX (Address 0xF9)

Table 153: STATUS_PROX register

Addr: 0xF9		STATUS_PROX		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6	*prox_high*	0	RO	This is the proximity high status register. This bit is set to one once the ADC proximity reading exceeds the threshold of the configured **PROX_THH** register value. The bit is automatically set to zero once the reading falls below **PROX_THH** register value. Please refer to Figure 31 for a detailed timing diagram of the proximity function.
5	*prox_high_on*	0	RO	This is a proximity event bit which is set to one once the ADC proximity reading exceeds the **PROX_THH** register threshold. It is cleared automatically once the **STATUS_PROX** register is read by the host MCU. Please refer to Figure 31 for a detailed timing diagram of the proximity function.
4	*prox_high_off*	0	RO	This is a proximity event bit which is set to one once the ADC proximity reading falls below the **PROX_THH** register threshold. It is cleared automatically once the **STATUS_PROX** register is read by the host MCU. Please refer to Figure 31 for a detailed timing diagram of the proximity function.
2	*prox_low*	0	RO	This is a proximity low status register. This bit is set to one once the ADC proximity reading falls below the threshold of the configured **PROX_THL** register value. The bit is cleared again once the reading exceeds the **PROX_THL** register value. Please refer to Figure 31 for a detailed timing diagram of the proximity function.
1	*prox_low_on*	0	RO	This is a proximity event bit which is set to one once the ADC proximity reading falls below the **PROX_THL** register threshold. It is cleared automatically once the **STATUS_PROX** register is read by the host MCU. Please refer to Figure 31 for a detailed timing diagram of the proximity function.
0	*prox_low_off*	0	RO	This is a proximity event bit which is set to one once the ADC proximity reading goes above the **PROX_THL** register threshold. It is cleared automatically once the **STATUS_PROX** register is read by the host MCU. Please refer to Figure 31 for a detailed timing diagram of the proximity function.

8.17.7 STATUS (Address 0xFA)

The **STATUS** register shows the current status of the interface. When released via **IRQ_ENABLE**, all bits can trigger an interrupt. Reading the **STATUS** registers only deletes *irq_iir_overflow*, *irq_fifooverflow_*and *irq_sequencer*.

To delete *irq_prox*, the **STATUS_PROX** register must be read.
To delete *irq_vcsel*, the **STATUS_VCSEL** register must be read.
To delete *irq_asat*, the **STATUS_ASAT** register must be read.
To delete *irq_lowvds*, the **STATUS_LED** register must be read.
To delete *irq_sequencer*, the **STATUS_SEQ** register must be read.
The interrupt for the fill level of the FIFO *irq_fifothreshold* cannot be deleted directly, but only by lowering the FIFO level.

Table 154: STATUS register

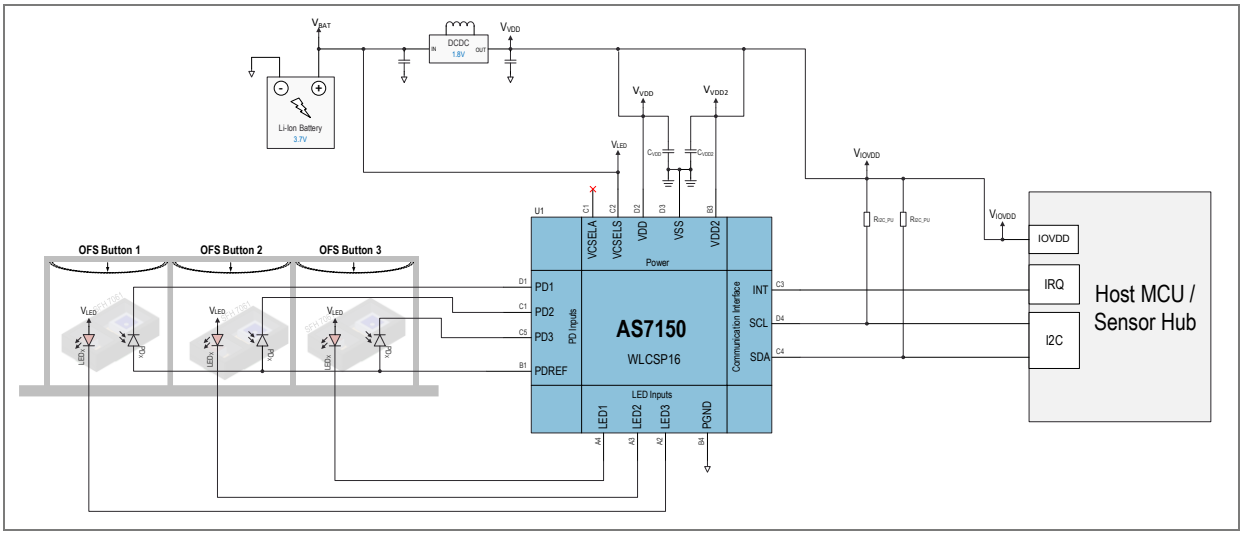
Addr: 0xFA		STATUS		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*irq_prox*	0	RO	This is the proximity interrupt status register. Please read the **STATUS_PROX** register for detailed information about the proximity state.
6	*irq_vcsel*	0	RO	This is the VCSEL interrupt status register. Please read the **STATUS_VCSEL** register to get information about the root cause of the interrupt which can be a short circuit on one of the LED inputs or an on time violation.
5	*irq_asat*	0	RO	This is the ADC modulator analog saturation interrupt register. Please check the **STATUS_ASAT** register to find out which of the modulators ran into saturation.
4	*irq_led_lowvds*	0	RO	This is the LED driver input low voltage detection interrupt register. Please read STATUS_LED register in order to find out which LED input has run into an undervoltage condition.
3	*irq_fifooverflow*	0	RO	This is the FIFO overflow interrupt register. Once this bit is set a FIFO overflow event occurred and ADC sampling data got lost.
2	*irq_fifothreshold*	0	RO	This is the FIFO threshold interrupt register. This interrupt is released one the FIFO level is above the FIFO level defined in **FIFO_THRESHOLD** register.
0	*irq_sequencer*	0	RO	This is the sequencer interrupt register. Please read out the **STATUS_SEQ** register to find out the root cause of the interrupt.

9 Application information

This chapter contains application related information.

9.1 Schematic

Figure 43: AS7150 application schematic 3 force buttons



9.2 External components

This chapter provides recommended external components for the example schematics shown in chapter 9.1.

Table 155: External components - capacitors

Symbol	Parameter	Temp. characteristic	Min. rated voltage	Max. tolerance	Recommended typ. value
C_{VDD}	Input capacitor for VDD pin	Y5R; X5R	4 V	±10%	1 µF
C_{VDD2}	Input capacitor for VDD2 pin	Y5R; X5R	4 V	±10%	1 µF

Table 156: External components - resistors

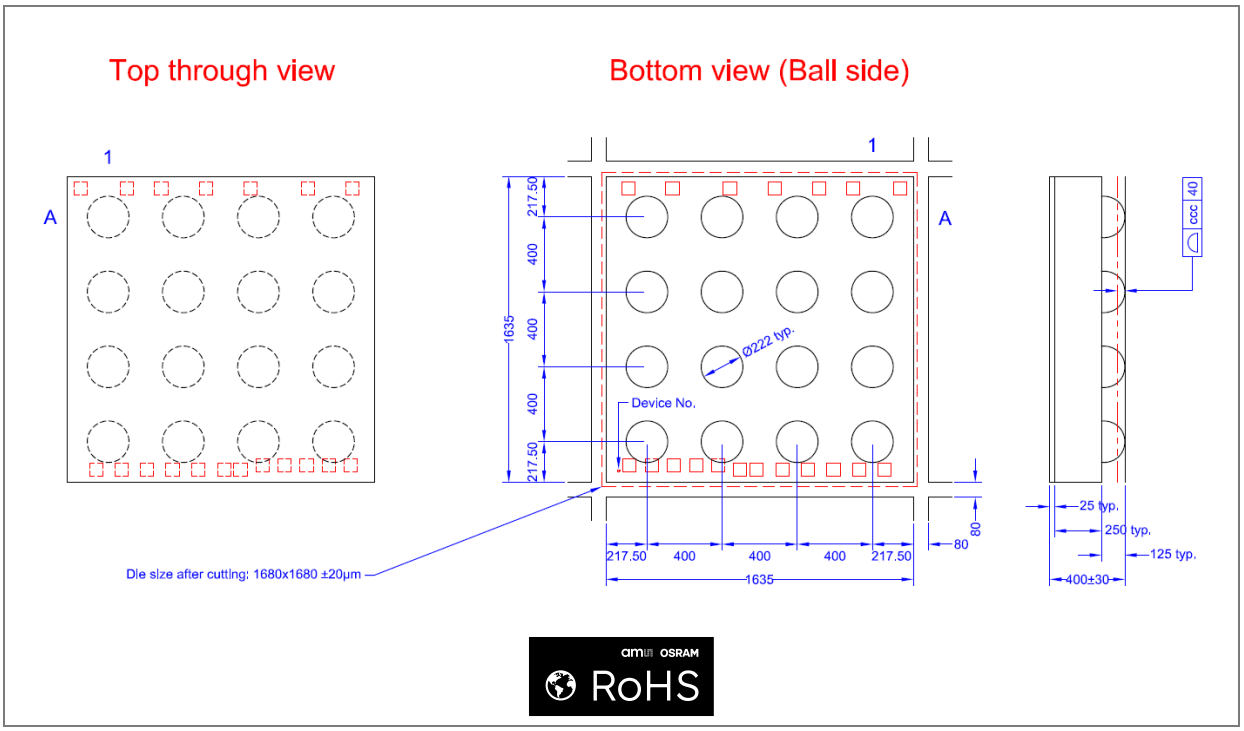
Symbol	Parameter	Min. power dissipation	Max. tolerance	Min. / Max. nominal resistance	Recommended typ. value
R_{I2C_PU}	I²C bus pull up resistors	0.03 W	±10%	1 kΩ / 47 kΩ	10 kΩ

Table 157: Optical front ends

Symbol	Parameter	Vendor	Part number	LED wavelength	Typ. forward voltage IR
MODx	Top looker optical front end with one photodiode and one IR LED	ams OSRAM	SFH 7061	940 nm	1.3 V @ 20 mA
MODx	Top looker optical front end with two photodiodes and one IR LED	ams OSRAM	SFH 7062	940 nm	1.3 V @ 20 mA
MODx	Side looker optical front end with one photodiode and one IR LED	ams OSRAM	SFH 7065	940 nm	1.3 V @ 20 mA
MODx	Side looker optical front end with two photodiodes and one IR LED	ams OSRAM	SFH 7066	940 nm	1.3 V @ 20 mA

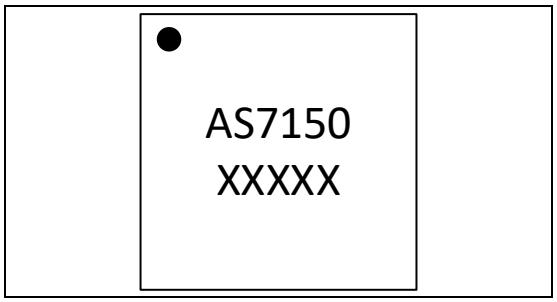
10 Package drawings & markings

Figure 44: WLCSP package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

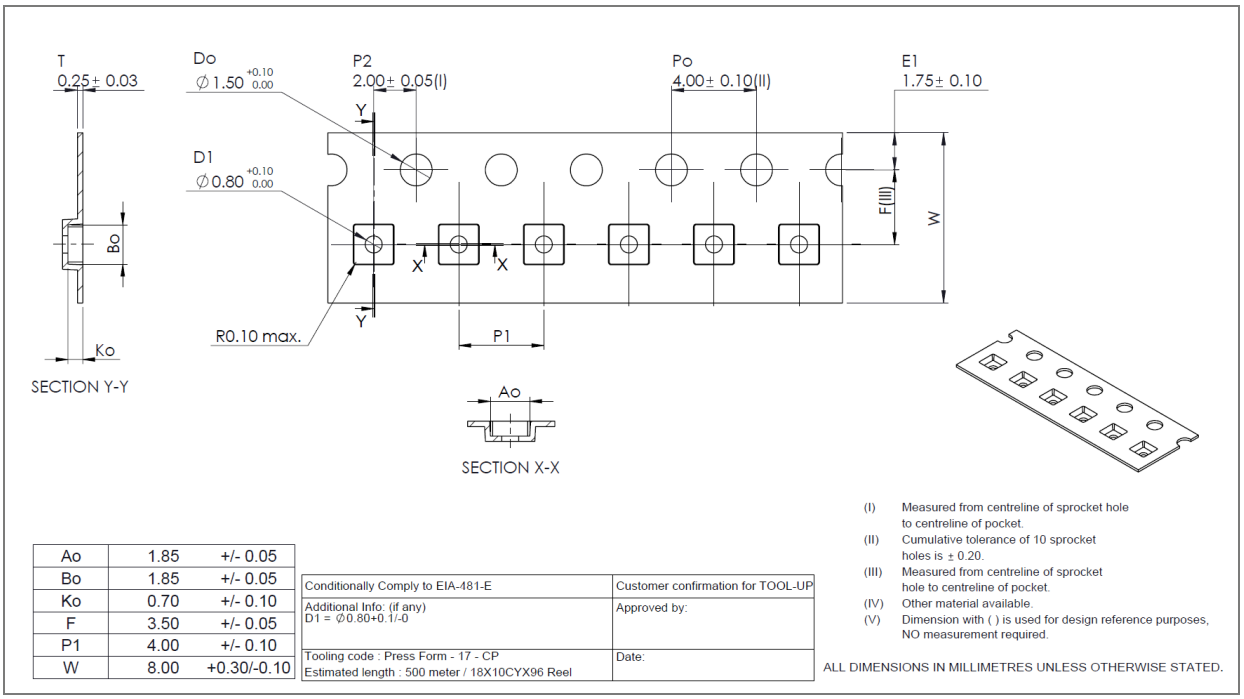
Figure 45: AS7150 package marking/code



xxxxx Tracecode

11 Tape & reel information

Figure 46: AS7150 tape dimensions



Ao	1.85	+/- 0.05
Bo	1.85	+/- 0.05
Ko	0.70	+/- 0.10
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.00	+0.30/-0.10

Conditionally Comply to EIA-481-E	Customer confirmation for TOOL-UP
Additional Info: (if any) D1 = ∅0.80+0.1/-0	Approved by:
Tooling code : Press Form - 17 - CP Estimated length : 500 meter / 18X10CYX96 Reel	Date:

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension with ( ) is used for design reference purposes, NO measurement required.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

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Document status	Product status	Definition
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Changes from previous released version to current revision v1-00	Page
Initial production version	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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