Toradex
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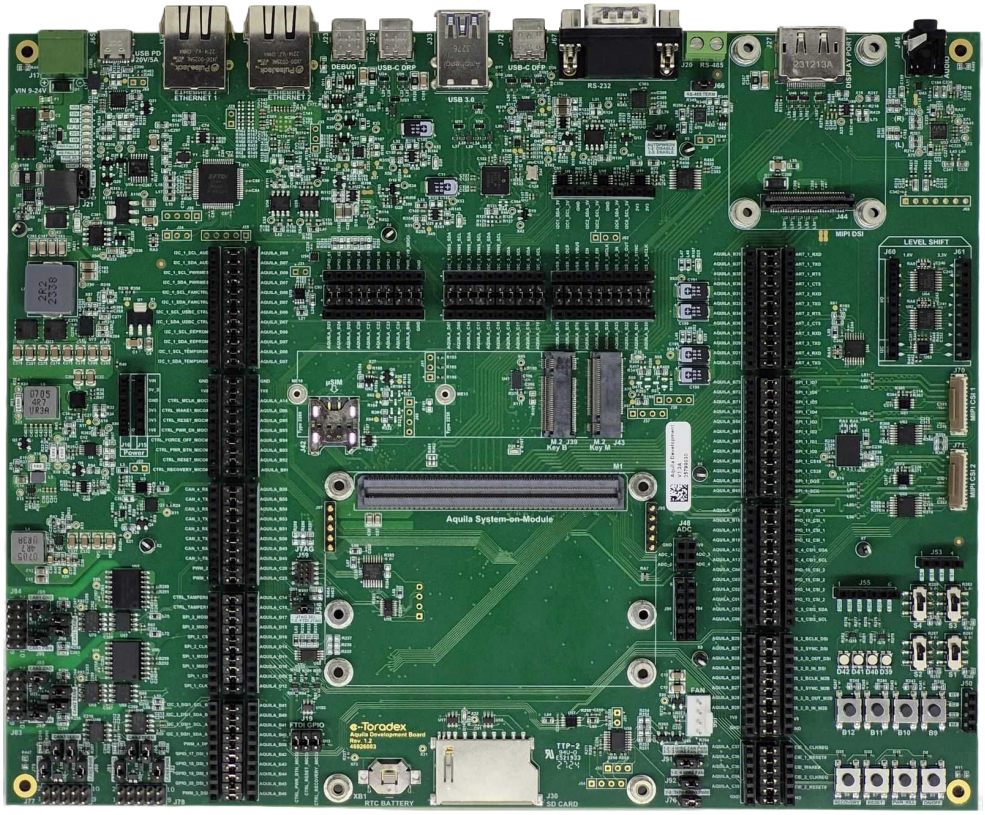
Aquila Development Board

HW Datasheet

Preliminary – Subject to Change



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
30-Jun-2025	Rev. 0.1	V1.2	Initial release

Contents

1 Introduction

The Aquila Development Board is a flexible and versitile board with which you can explore and evaluate the functionality and performance of the Aquila product family.

The Aquila Development Board:

- Supports a wide variety of industry-standard interfaces
- Provides advanced multimedia and high-speed connectivity options
- Highly configurable signal routing for function evaluation

The Aquila Development Board is built on a 6-layer printed circuit board (PCB), and 2 layers are used for high-speed signal routing.

To ensure optimal compatibility and user experience with the Aquila Development Board, it must be ordered with the Toradex DSI to HDMI Adapter. This adapter uses a MIPI DSI interface to provide an HDMI output that seamlessly integrates with all Aquila System on Modules, guaranteeing an enhanced and comprehensive user experience.

1.1 Reference Documents

For detailed technical information, please refer to the documents listed below.

1.1.1 Aquila Family Specification

https://tezi.toradex.com/artifactory/website-hwdocs-prod-frankfurt/aquila/design-resources/plain/v1_0/rev_1_0/aquila_family_specification.pdf

1.1.2 Aquila Carrier Board Design Guide

https://tezi.toradex.com/artifactory/website-hwdocs-prod-frankfurt/aquila/design-resources/design_guide_prerelease/n_a/rev_0_2/aquila_carrier_board_design_guide.pdf

1.1.3 Aquila Computer on Module Family Overview

https://www.toradex.com/computer-on-modules/aquila-arm-family

1.1.4 Toradex Developer Website – Aquila Computer on Module Documents

https://developer.toradex.com/hardware/aquila-som-family/modules/

1.1.5 Carrier Board Layout Guide

https://docs.toradex.com/102492-layout-design-guide.pdf

1.1.6 Push-button On/Off Controller Datasheet

https://www.analog.com/media/en/technical-documentation/data-sheets/2954fb.pdf

1.1.7 EEPROM Datasheet

https://www.st.com/resource/en/datasheet/m24c02-w.pdf

1.1.8 Temperature Sensor Datasheet

https://www.ti.com/lit/ds/symlink/tmp1075.pdf

1.1.9 USB HUB Datasheet

https://ww1.microchip.com/downloads/aemDocuments/documents/UNG/ProductDocuments/DataSheets/USB5744-Data-Sheet-DS00001855.pdf

1.1.10 Gigabit Ethernet Transceiver Datasheet

https://www.ti.com/lit/gpn/dp83867is

1.1.11 RS232 Transceiver Datasheet

https://www.ti.com/lit/gpn/TRS3122E

1.1.12 RS485 Transceiver Datasheet

https://www.ti.com/lit/gpn/sn65hvd01

1.1.13 Audio Codec Datasheet

https://statics.cirrus.com/pubs/proDatasheet/WM8904_Rev4.1.pdf

1.1.14 USB Type-C Configuration Channel Logic IC Datasheet

https://www.ti.com/lit/gpn/TUSB321AI

1.1.15 UV/OV and Reverse Protection Controller Datasheet

https://www.analog.com/media/en/technical-documentation/data-sheets/ltc4368.pdf

1.1.16 USB Type-C Port Power Sink Controller Datasheet

https://www.infineon.com/dgdl/Infineon-EZ-PD_BCR_Datasheet_USB_Type-C_Port_Controller_for_Power_Sinks-DataSheet-v03_00-EN.pdf?fileId=8ac78c8c7d0d8da4017d0ee7ce9d70ad

1.1.17 Toradex Website - Toradex DSI to HDMI Adapter

https://developer.toradex.com/hardware/accessories/add-ons/dsi-hdmi-adapter

1.2 Abbreviations

Table 1: Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card

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Table 1: Abbreviations (Continued)

Abbreviation	Explanation
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

2 Features

2.1 Overview

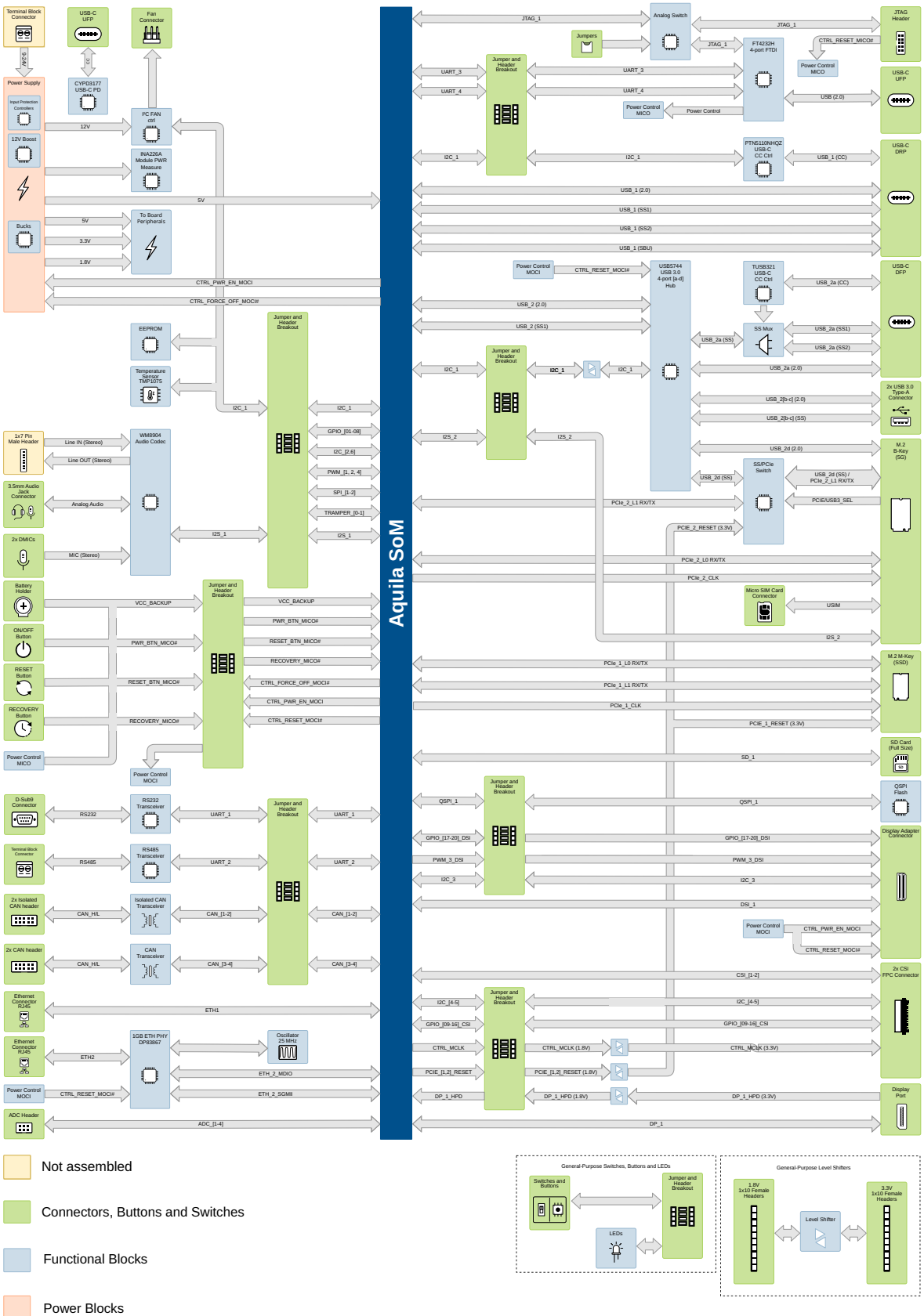
The Aquila Development Board provides the following features and communication interfaces:

- 1x USB-C connector providing USB Dual-Role-Port (DRP) or host/client functionality
- 1x stacked USB 3.0 Type-A connector, featuring 2x USB ports through the on-board USB HUB
- 1x USB-C DFP connector
- 2x RJ45 connectors featuring 10/100/1000 Mbps Ethernet interfaces (1x Ethernet transceiver placed on the Development Board)
  - 1x Gigabit Ethernet to SOM
  - 1x Gigabit Ethernet SGMII (DP83867)
- 1x M.2 M-Key SSD over PCIe
- 1x M2. B-Key 5G module over PCIe with micro-sim holder
- 1x DisplayPort connector
- 2x CSI FPC connectors
- 1x JTAG header
- 1x Full Size SD Card holder
- 1x QSPI NOR Flash
- 1x RS232 over DB9 connector
- 1x RS485 terminal connector
- Audio Codec over I2S with Audio Jack TRS
- 8x GPIO jumpers
- 2x GP-I2C jumpers
- 2x GP-SPI jumpers
- 2x PWM out jumpers
- 2x Non-isolated CAN
- 2x Isolated CAN
- 4x ADC jumpers
- 4x 1.8 V to 3.3 V Signal Translator
- 4x 3.3 V to 1.8 V Signal Translator
- 1x 1.8 V to 3.3 V I2C Translator
- 4x general-purpose LEDs, switches and pushbuttons
- DSI + I2C (touch) + PWM mezzanine connector
- 1x EEPROM 2kBit
- 1x Temperature Sensor
- CR1025 Batt holder
- Fan connector and fan controller
- USB-C Power Delivery
- 9-24V input power terminal connector
- Aquila Module Connector
- Power monitor
- 1x Power Button
- 1x Reset Button

- 1x Recovery Button
- Extremely flexible and easy to use low-speed signal breakout and jumper area allowing easy signal re-routing, external connection, and measurement/probing
- Undervoltage, overvoltage, overcurrent and reverse voltage protected power input

2.2 Hardware Architecture Block Diagram

Figure 1: Aquila Development Board Hardware Architecture



2.3 Physical Drawing

2.3.1 Top Side Connectors

Figure 2: Aquila Development Board connectors and controls

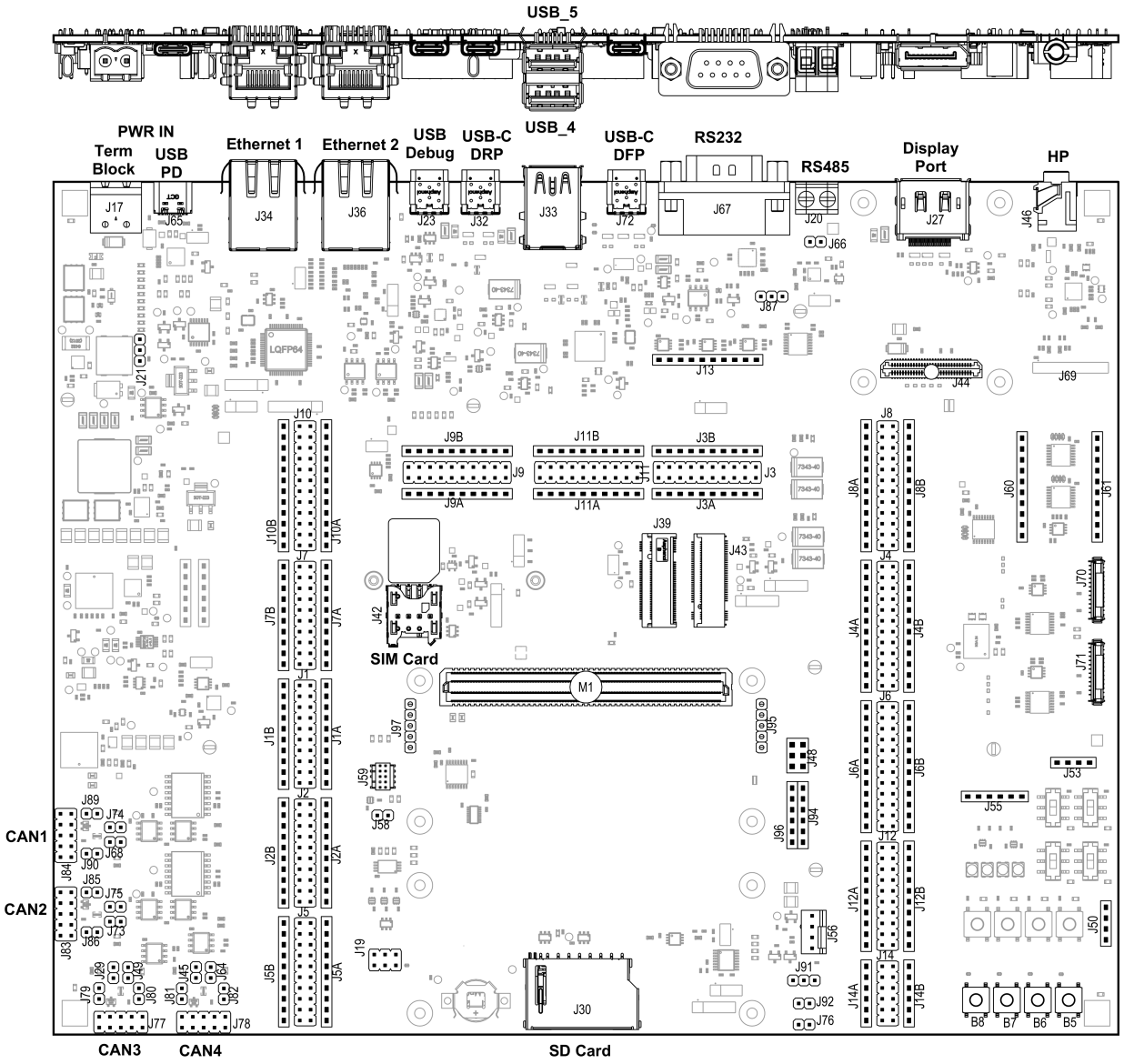


Table 2: Top Side Connectors

Designator	Description	Remarks
J11	+V3.3	
J13	+V3.3	
J17	Terminal Block Power Supply connector	9-28V
J20	RS485 connector	
J23	USB-C Debug Connection	
J27	DisplayPort Connector	
J30	Full Size SD Card 4-bit connector	
J32	USB-C OTG	
J33	2x USB-3.0 x HOST connector	
J34	Ethernet connector	Ethernet_1
J36	Ethernet connector	Ethernet_2
J39	M.2 B-Key connector	
J42	SIM Card holder	Micro SIM
J43	M.2 B-Key connector	
J44	MIPI DSI Display Adapter connector	
J46	Analog audio AUX OUT jack	
J48	ADC input header	
J56	Fan Connector	
J59	JTAG connector	
J60	Level shifter header	1.8V
J61	Level shifter header	3.3V
J65	USB-C Power Supply connector	20V
J67	RS232 connector	
J69	Speaker header	
J70	MIPI CSI Camera connector	
J71	MIPI CSI Camera connector	
J72	USB-C to Serial	
J77	CAN3	Non-Isolated
J78	CAN4	Non-Isolated
J83	CAN2	Isolated
J84	CAN1	Isolated

3 Interface Description

3.1 Aquila System-On-Module

Connector Type: 400 pin APM6-100-01.5-L-04-0-A-TR socket

Manufacturer: Samtec Inc.

For the pinout of the Aquila module, please refer to the applicable Aquila module datasheet or to the Aquila Family Specification / Aquila Carrier Board Design Guide for the abstract pinout. Stand-offs are available on Aquila Development Board for affixing the Aquila module. It is recommended to use M2×0.4 size screws to fasten the Aquila module with the stand-offs.

3.2 Power Supply

The Aquila Development Board has two different power supply connectors:

- J17: Terminal Block Power Supply (9-28V)
- J65: USB-C PD (20V)

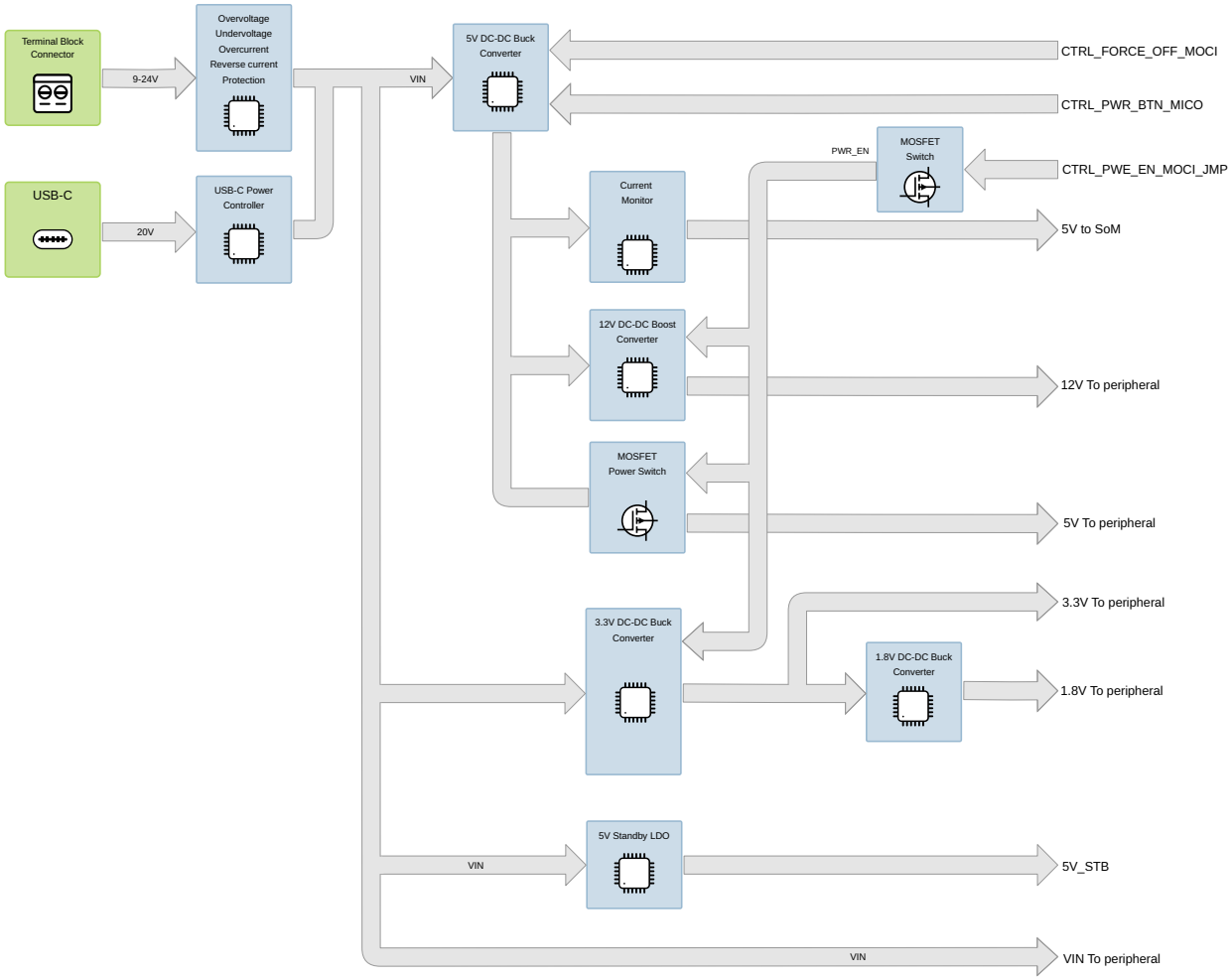
The estimated power consumption is up to 100W, but can vary with the type of SOM, connected peripherals and usage.

The USB Power Supply connector J65 and the Terminal Block Power Supply connector J17 are electrically connected, and only one of these connectors should be used for powering the board. The simultaneous connection the two power supplies is not allowed. Violating this requirement may damage the power supply or the Development Board.

Input voltage through the Terminal Block Power Supply can vary across a range of 9-24V. The maximum input current is limited to 12.5A. If you are using 9V as input and your application dissipates more than 112.5W, please work with a higher input voltage, up to 24V.

Several power domains are available on the Development Board. The board's power supply architecture is shown in the picture below.

Figure 3: Power supply architecture



The on-board power supplies provide the following nominal voltages and currents.

Table 3: On-Board Power Supplies

Nominal Voltage	Maximum current	Maximum power
12V	2.3A	27.6W
5V	20A	100W
3.3V	8A	26.4W
1.8V	3A	9-28V

3.2.1 Power Out Headers (J15, J16)

Two female pin headers J15 and J16, with main system voltages, are available on the Aquila Development Board, and can be used for powering external boards and modules. The pinouts of both J15 and J16 connectors are identical.

The connectors of pins J15 and J16 are rated for maximum current of 3A

Connector Type: 1×6 Pin Header Female, 2.54mm pitch

Table 4: Power Out Headers $J15, J16$

Pin	Signal Label	Remarks
1	VIN	Outputs the voltage supplied to the board. Connects to the Terminal Block and USB-C supplies after their protection and control circuits
2	5V_S	Switched 5V
3	GND	
4	3V3	
5	3V3	
6	1V8	

3.2.2 Power Control

The Aquila Development Board power control is implemented using the Linear LTC2954 Push-button On/Off controller and with the signal CTRL_PWR_EN_MOCI, used to enable the peripheral power supplies. For further information about the signals provided by the LTC2954 controller, please refer to its datasheet. For more information regarding the power-up sequence implemented on the board, please refer to the Aquila Carrier Board Design Guide. The buttons B7 and B5 have been assigned to the RESET and ON/OFF functions, respectively. B8 is used to put the installed Aquila Computer Module into RECOVERY mode. Board power also can be controlled by the Aquila Computer Module with an open drain (OD) CTRL_FORCE_OFF_MOCI# signal. This feature allows the Aquila module to perform a proper power-down procedure. For more details, please refer to the Aquila Carrier Board Design Guide.

3.2.3 Power Supply Input Protection

Supply input is protected against ESD strikes, reverse voltage polarity, overvoltage, undervoltage, and short circuits. The protection circuit is based on an LTC4368 IC from Analog Devices. For detailed information, please refer to the LTC4368 datasheet.

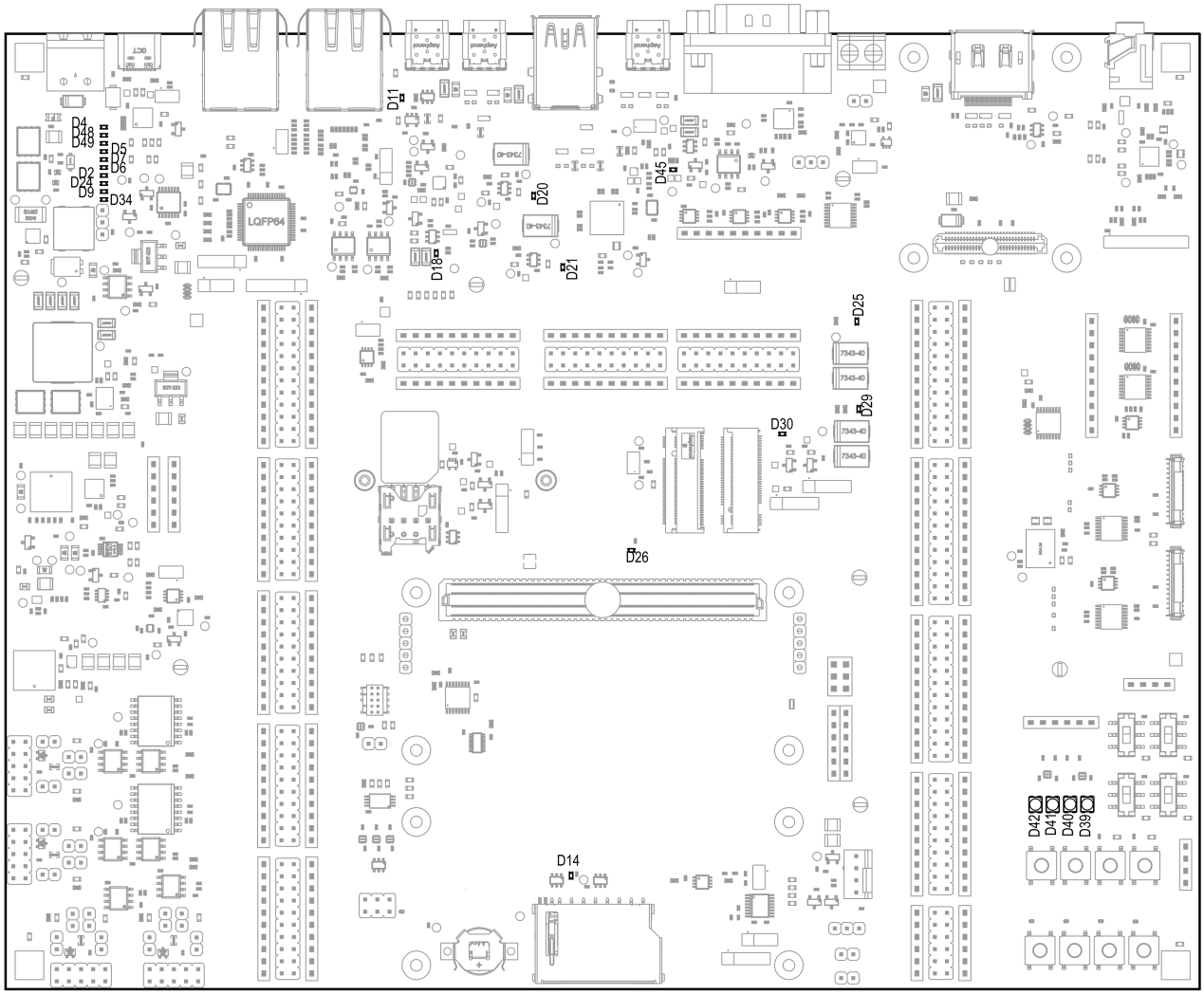
Table 5: Power Supply Input Ratings

Parameter Name	Min	Typ	Max	Unit
Input voltage (Absolute maximum, limited with an ESD diode)			30	V
Undervoltage threshold	7.49	7.6	7.71	V
Overvoltage threshold	27.09	27.5	27.91	V
Overcurrent threshold	13.33	16.67	20	A
Reverse current protection	0.33	1	1.67	A
Recommended input voltage		9-24		V

3.3 Indicator LEDs

The Aquila Development Board features 24 LEDs. These LEDs indicate the statuses of the main power supplies, all power gated peripherals. LEDs are also used for indicating the activity of some peripherals.

Figure 4: Indicator LEDs



The LEDs and their functions are listed in the table below.

Table 6: LED designators and description

Designator	Color	Side	Description
D2	Red	Top	LED is lit when power fault occours
D4	Green	Top	LED is lit when 5V Buck Converter is active
D5	Green	Top	LED is lit when Switched 5V is active
D6	Green	Top	LED is lit when 1.8V Buck Converter is active
D7	Green	Top	LED is lit when 3.3V Buck Converter is active
D9	Green	Top	LED is lit when Peripheral Power is ON
D11	Green	Top	LED is lit when Debug USB Rail is active
D14	Green	Top	LED is lit when SD Card Voltage is active
D18	Green	Top	LED is lit when USB-OTG Rail is active

Continued on next page

Table 6: LED designators and description (Continued)

Designator	Color	Side	Description
D20	Green	Top	LED is lit when USB 3.0 Type A Top Rail is active
D21	Green	Top	LED is lit when USB 3.0 Type A Bottom Rail is active
D24	Red	Top	LED is lit when USB-PD fault occours
D25	Green	Top	LED is lit when M.2 B-Key Rail is active
D26	Green	Top	M.2 B-Key LED_1#
D29	Green	Top	LED is lit when M.2 M-Key Rail is active
D30	Green	Top	M.2 M-Key LED_1#
D34	Red	Top	Reset State LED
D39	Green	Top	User LED. It is lit when the LED1 signal is High
D40	Green	Top	User LED. It is lit when the LED2 signal is High
D41	Green	Top	User LED. It is lit when the LED3 signal is High
D42	Green	Top	User LED. It is lit when the LED4 signal is High
D45	Green	Top	LED is lit when USB-DFP Rail is active
D48	Green	Top	LED is lit when 12V Boost Converter is active
D49	Green	Top	LED is lit when Input Voltage is active

3.4 Ethernet Interface

The Aquila Development Board provides 2x RJ45 connectors with integrated magnetics for 10/100/1000Mb Ethernet. The Ethernet 1 transceiver is located on the SoM while the Ethernet 2 transceiver is placed on the Aquila Development Board.

3.4.1 Ethernet 1 Connector (J34)

Connector Type: RJ45, Pulse JXD0-0025NL

Table 7: Ethernet 1 Connector (J34)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Description
1	GND		PWR		Ground
2	ETH_1_MDI3_N	A98	I/O (Analog)		Media Dependent Interface
3	ETH_1_MDI3_P	A97	I/O (Analog)		Media Dependent Interface
4	ETH_1_MDI2_N	A95	I/O (Analog)		Media Dependent Interface
5	ETH_1_MDI2_P	A94	I/O (Analog)		Media Dependent Interface
6	ETH_1_MDI1_N	A92	I/O (Analog)		Media Dependent Interface
7	ETH_1_MDI1_P	A91	I/O (Analog)		Media Dependent Interface
8	ETH_1_MDI0_N	A89	I/O (Analog)		Media Dependent Interface
9	ETH_1_MDI0_P	A88	I/O (Analog)		Media Dependent Interface
11	+V3.3		Power	+3.3V	Power supply for the indication LEDs
12	ETH_1_LED2	A100	O (OD)		LED for indicating established Ethernet link
13	+V3.3		Power	+3.3V	Power supply for the indication LEDs

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Table 7: Ethernet 1 Connector (J34) (Continued)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Description
14	ETH_1_LED1	A99	O (OD)		LED for indicating Ethernet receive/transmit activity
S	GND_CHASSIS		PWR		Shield Protection

3.4.2 Ethernet 2 Connector (J36)

The Ethernet_2 interface is based on the DP83867ISRGZ 10/100/1000 Mbps Ethernet PHY which is using ETH_2_XGMII interface of the module. For more information, refer to the DP83867ISRGZ IC datasheet.

Connector Type: RJ45, Pulse JXD0-0025NL

Table 8: Ethernet 2 Connector (J36)

Pin	Signal name	I/O Type	Voltage	Description
1	GND	PWR		Ground
2	ETH_2_D3_N	I/O (Analog)		Media Dependent Interface
3	ETH_2_D3_P	I/O (Analog)		Media Dependent Interface
4	ETH_2_D2_N	I/O (Analog)		Media Dependent Interface
5	ETH_2_D2_P	I/O (Analog)		Media Dependent Interface
6	ETH_2_D1_N	I/O (Analog)		Media Dependent Interface
7	ETH_2_D1_P	I/O (Analog)		Media Dependent Interface
8	ETH_2_D0_N	I/O (Analog)		Media Dependent Interface
9	ETH_2_D0_P	I/O (Analog)		Media Dependent Interface
11	+V3.3	Power	+3.3V	Power supply for the indication LEDs
12	ETH_2_LINK	O (OD)		LED for indicating established Ethernet link
13	+V3.3	Power	+3.3V	Power supply for the indication LEDs
14	ETH_2_ACT	O (OD)		LED for indicating Ethernet receive/transmit activity
S	GND_CHASSIS	PWR		Shield Protection

3.5 USB Interface

The Aquila Family features two USB ports, which are connected to the Aquila Development Board as follows:

- USB_1: Connects to a Dual Role Port (DRP) USB-C connector (J32). This port is primarily used in recovery mode.
- USB_2: Connects to a USB Hub, allowing communication via USB with 4 different connectors
  - A USB-C Dual Facing Port (DFP) connector (J72)
  - A dual-stacked USB 3.0 Type-A connectors (J33)
  - A M.2 Key-B connector

More details on each port's functionality in the following sections

3.5.1 Aquila USB_1 Port

The Aquila Development Board integrates a USB-C connector (J32), which connects to the Aquila USB_1 port. The USB_1 port supports USB 2.0 only and serves primarily in recovery mode for loading new software onto the module.

The J32 connector functions as a Dual-Role Port (DRP), meaning it can act as either Host or Device. This is similar to USB On-The-Go (OTG) functionality.

- As a Peripheral (UFP): Indicates VBUS current supplied by the host using GPIO pins
- As a Host (DFP): Advertises VBUS current to connected peripherals

The USB Type-C receptacle lacks an ID pin. Instead, it uses Configuration Channel (CC) pins to:

- Determine whether the connected device acts as host, device, or both
- Detect connection presence or disconnection

To manage USB dual-role operations, the board uses the TUSB321AI chip. For in-depth details, refer to the TUSB321AI datasheet

On the Development Board, USB_1 port is configured as a dual-role port (DRP) by default, and its output current is limited to 1A.

3.5.1.1 USB-C DRP (USB_1) Connector (J32)

Connector Type: USB-C, Amphenol ICC 12401826E412A

Table 9: USB_1 Connector (J32)

Pin	Signal Name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
A1	GND		PWR			
A2	USB_1_SSTX1_P	A64	I			Positive differential USB 3.x transmit signal
A3	USB_1_SSTX1_N	A65	I			Negative differential USB 3.x transmit signal
A4	USB_1_VBUS	B76	PWR	+5V		
A5	USB_CC1					USB-C configuration channel signal 1
A6	USB_1_D_P	A70	I/O			Positive differential USB 2.0 signal
A7	USB_1_D_N	A71	I/O			Negative differential USB 2.0 signal
A8	USB_1_SBU1	A68				USB-C SideBand Use 1
A9	USB_1_VBUS	B76	PWR	+5V		
A10	USB_1_SSRX2_N	A73	O			Negative differential USB 3.x receive signal
A11	USB_1_SSRX2_P	A74	O			Positive differential USB 3.x receive signal
A12	GND		PWR			
B1	GND		PWR			
B2	USB_1_SSTX2_P	A76	I			Positive differential USB 3.x transmit signal
B3	USB_1_SSTX2_N	A77	I			Negative differential USB 3.x transmit signal
B4	USB_1_VBUS	B76	PWR	+5V		
B5	USB_CC2					USB-C configuration channel signal 2
B6	USB_1_D_P	A70	I/O			Positive differential USB 2.0 signal

Continued on next page

Table 9: USB_1 Connector (J32) (Continued)

Pin	Signal Name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
B7	USB_1_D_N	A71	I/O			Negative differential USB 2.0 signal
B8	USB_1_SBU2	A67				USB-C SideBand Use 2
B9	USB_1_VBUS	B76	PWR	+5V		
B10	USB_1_SSRX1_N	A62	O			Negative differential USB 3.x receive signal
B11	USB_1_SSRX1_P	A61	O			Positive differential USB 3.x receive signal
B12	GND		PWR			
SH1	GND		PWR			
SH2	GND		PWR			
SH3	GND		PWR			
SH4	GND		PWR			

3.5.2 Aquila USB_2 Port

The Aquila Development Board integrates a 4-port USB hub (Microchip USB5744T-I/2G), which is connected to the SoM's USB_2 port. This setup provides 4x USB 3.x / USB 2.0 Host interfaces, which are connected to:

- USB_2a: USB-C DFP Connector (J72)
- USB_2b and USB_2c: Dual-stacked USB 3.0 Type-A Connector (J33)
- USB_2d: PCIe M.2 Key-B Connector (J39)

In the Aquila Development Board schematics, the USB_2[a-b] signals appear as USB_[3-6] for USB Hub SoC and connectors.

The OC (Over-Current) sensing pin of the USB_2 port is not used, and the USB hub handles OC conditions.

The level of USB 3.x support depends on the specific System on Module (SoM) used, some SoMs may not support USB 3.x at all. For detailed information about supported USB interfaces and their speeds, refer to the respective SoM datasheet.

3.5.2.1 USB-C DFP (USB_2) Connector (J72)

Connector Type: USB-C, Amphenol ICC 12401826E412A

Table 10: USB-C DFP Connector (J72)

Pin	Signal Name	I/O Type	Voltage	Description
A1	GND	PWR		
A2	USB_3_SSTX1_P	I		Positive differential USB 3.x transmit signal
A3	USB_3_SSTX1_N	I		Negative differential USB 3.x transmit signal
A4	USB_3_VBUS	PWR	+5V	
A5	USB_3_CC1			USB-C configuration channel signal 1
A6	USB_3_P	I/O		Positive differential USB 2.0 signal

Continued on next page

Table 10: USB-C DFP Connector (J72) (Continued)

Pin	Signal Name	I/O Type	Voltage	Description
A7	USB_3_N	I/O		Negative differential USB 2.0 signal
A8	NC			Not Connected
A9	USB_3_VBUS	PWR	+5V	
A10	USB_3_SSRX2_N	O		Negative differential USB 3.x receive signal
A11	USB_3_SSRX2_P	O		Positive differential USB 3.x receive signal
A12	GND	PWR		
B1	GND	PWR		
B2	USB_3_SSTX2_P	I		Positive differential USB 3.x transmit signal
B3	USB_3_SSTX2_N	I		Negative differential USB 3.x transmit signal
B4	USB_3_VBUS	PWR	+5V	
B5	USB_CC2			USB-C configuration channel signal 2
B6	USB_3_P	I/O		Positive differential USB 2.0 signal
B7	USB_3_N	I/O		Negative differential USB 2.0 signal
B8	NC			Not Connected
B9	USB_3_VBUS	PWR	+5V	
B10	USB_3_SSRX1_N	O		Negative differential USB 3.x receive signal
B11	USB_3_SSRX1_P	O		Positive differential USB 3.x receive signal
B12	GND	PWR		
SH1	GND			
SH2	GND			
SH3	GND			
SH4	GND			

3.5.2.2 USB Type-A (USB_2) Stacked Connector (J33)

Connector Type: Stacked USB 3.0 Type-A, Amphenol GSB4112312HR (Pins starting with U connect to the UPPER, pins starting with L connect to the LOWER port)

Table 11: USB Type-A Stacked Connector (J33)

Pin	Signal Name	I/O Type	Voltage	Description
U1	USB4_5V	PWR	+5V	
U2	USB4_N	I/O		Negative differential USB 2.0 signal
U3	USB4_P	I/O		Positive differential USB 2.0 signal
U4	GND	PWR		
U5	USB_4_SSRX_N	I		Negative differential USB 3.x receive signal
U6	USB_4_SSRX_P	I		Positive differential USB 3.x receive signal
U7	GND	PWR		
U8	USB_4_SSTX_N	O		Negative differential USB 3.x transmit signal
U9	USB_4_SSTX_P	O		Positive differential USB 3.x transmit signal

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Table 11: USB Type-A Stacked Connector (J33) (Continued)

Pin	Signal Name	I/O Type	Voltage	Description
L1	USB5_5V	PWR	+5V	
L2	USB_5_N	I/O		Negative differential USB 2.0 signal
L3	USB_5_P	I/O		Positive differential USB 2.0 signal
L4	GND	PWR		
L5	USB_5_SSRX_N	I		Negative differential USB 3.x receive signal
L6	USB_5_SSRX_P	I		Positive differential USB 3.x receive signal
L7	GND	PWR		
L8	USB_5_SSTX_N	O		Negative differential USB 3.x transmit signal
L9	USB_5_SSTX_P	O		Positive differential USB 3.x transmit signal
S1	GND	PWR		
S2	GND	PWR		
S3	GND	PWR		
S4	GND	PWR		

3.6 PCIe Interface

The Aquila Development Board makes the standard PCIe interface on the Aquila SoMs available on a Mini PCIe slot. PCI Express Mini Card is a replacement for the Mini PCI form factor. Mini PCIe provides both the standard PCI Express and USB 2.0 signals, allowing flexibility in peripheral design. PCI Express Mini Card edge connectors provide multiple connections and buses, such as listed below:

- PCI Express 1 lane (with SMBus)
- USB 2.0
- Indication LEDs for wireless network status
- SIM card for cellular applications (UIM signals)

The Aquila Development Board provides both M.2 Key-B and M.2 Key-M connectors (J39 and J43 respectively) for PCIe communication. The connectors' pinouts are listed in the next sections.

3.6.1 M.2 Key-B Connector (J39)

Connector Type: Mini Card M.2 PCIe connector, Key B, Amphenol FCI MDT420B01001

Table 12: M.2 Key-B Connector (J39)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	CONFIG_3		O		10k to M2B_3V3	Config 0 and 3 control whether the PCIe or USB3 is selected
3	GND		PWR			
5	GND		PWR			
7	USB6_P		I/O			Positive differential USB 2.0 data signal
9	USB6_N		I/O			Negative differential USB 2.0 data signal
11	GND		PWR			

Continued on next page

Table 12: M.2 Key-B Connector (J39) (Continued)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
13	NC					Not connected
15	NC					Not connected
17	NC					Not connected
19	NC					Not connected
21	CONFIG_0		O		10k to M2B_3V3	Config 0 and 3 control whether the PCIe or USB3 is selected
23	M2_GPIO_11		I/O			M.2 General purpose I/O
25	DPR		I/O			Device present signal. Connected to header J37 pin 3
27	GND		PWR			
29	MUX_PCIE_2_L1_USB6_RX_N		O			Negative differential PCIe Lane 1 or USB6 receive signal
31	MUX_PCIE_2_L1_USB6_RX_P		O			Positive differential PCIe Lane 1 or USB6 receive signal
33	GND		PWR			
35	MUX_PCIE_2_L1_USB6_TX_N		I			Negative differential PCIe Lane 1 or USB6 transmit signal
37	MUX_PCIE_2_L1_USB6_TX_P		I			Positive differential PCIe Lane 1 or USB6 transmit signal
39	GND		PWR			
41	PCIE_2_L0_RX_N	C29	O			Negative differential PCIe Lane 0 receive signal
43	PCIE_2_L0_RX_P	C28	O			Positive differential PCIe Lane 0 receive signal
45	GND		PWR			
47	PCIE_2_L0_TX_N	D31	I			Negative differential PCIe Lane 0 transmit signal
49	PCIE_2_L0_TX_P	D30	I			Positive differential PCIe Lane 0 transmit signal
51	GND		PWR			
53	PCIE_2_CLK_N	D28	I			Negative differential PCIe reference clock signal
55	PCIE_2_CLK_P	D27	I			Positive differential PCIe reference clock signal
57	GND		PWR			
59	NC					Not connected
61	NC					Not connected
63	NC					Not connected
65	NC					Not connected
67	M2_RESET#		I	+3.3V	27k to 1V8	Set to high to not reset WWAN
69	NC					Not connected
71	GND		PWR			
73	GND		PWR			
75	NC					Not connected
2	M2M_3V3		PWR	+3.3V		+3.3V Power input
4	M2M_3V3		PWR	+3.3V		+3.3V Power input
6	M2_FULL_CARD_POWER_OFF		I	+3.3V	1.87k to M2B_3V3	Set to high to not turn off WWAN

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Table 12: M.2 Key-B Connector (J39) (Continued)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
8	M2_W_DISABLE#		I	+3.3V	27k to 1V8	Set to high to not disable WWAN
10	M2_GPIO9/DAS/DSS/LED_1#		O	+3.3V	1.87k to M2B_3V3	WWAN status indicator LED
12	NC					Not connected
14	NC					Not connected
16	NC					Not connected
18	NC					Not connected
20	I2S_2_BCLK_M2B	B26	O			Serial audio bit clock
22	I2S_2_D_OUT_M2B	B28	O			Serial audio output data
24	I2S_2_D_IN_M2B	B29	I			Serial audio input data
26	M2_GPIO_10		I/O			M.2 General purpose I/O
28	I2S_2_SYNC_M2B	B27	O			Synchronization/ field select/ left-right channel select
30	UIM_RST		O			SIM Card RESET
32	UIM_CLK		O			SIM Card Clock
34	UIM_DATA		I/O			SIM Card Data
36	UIM_PWR		PWR			SIM Card Power
38	DEVSLP		I			Device sleep. Connected to GND
40	M2_SMB_CLK/GPIO_0		I			System management bus clock. Connected to header J37 pin 1
42	M2_SMB_DATA/GPIO_1		I/O			System management bus data. Connected to header J37 pin 2
44	ALERT#/GPIO_2		O			System management alert signal. Connected to header J37 pin 4
46	M2_GPIO_3		I/O			M.2 General purpose I/O
48	M2_GPIO_4		I/O			M.2 General purpose I/O
50	PCIE_2_RESET#_3V		I			PCIE 2 Reset signal
52	PCIE_2_CLKREQ		O		10k to 1V8	PCIE 2 clock request
54	PCIE_WAKE#		O		10k to 1V8	PCIE wake signal
56	NC					Not connected
58	NC					Not connected
60	NC					Not connected
62	NC					Not connected
64	NC					Not connected
66	UIM_PWR		PWR			Detect SIM card presense
68	NC					Not connected
70	M2M_3V3		PWR	+3.3V		+3.3V Power input
72	M2M_3V3		PWR	+3.3V		+3.3V Power input
74	M2M_3V3		PWR	+3.3V		+3.3V Power input

3.6.2 M.2 Key-M Connector (J43)

Connector Type: Mini Card M.2 PCIe connector, Key M, Amphenol FCI MDT850M01501

Table 13: M.2 Key-M Connector (J43)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
3	GND		PWR			
5	NC					Not connected
7	NC					Not connected
9	GND		PWR			
11	NC					Not connected
13	NC					Not connected
15	GND		PWR			
17	NC					Not connected
19	NC					Not connected
21	GND		PWR			
23	NC					Not connected
25	NC					Not connected
27	GND		PWR			
29	PCIE_1_L1_RX_N	C44	O			Negative differential PCIe receive signal
31	PCIE_1_L1_RX_P	C43	O			Positive differential PCIe receive signal
33	GND		PWR			
35	PCIE_1_L1_TX_N	D43	I			Negative differential PCIe receive signal
37	PCIE_1_L1_TX_P	D42	I			Positive differential PCIe receive signal
39	GND		PWR			
41	PCIE_1_L0_RX_N	C41	O			Negative differential PCIe receive signal
43	PCIE_1_L0_RX_P	C40	O			Positive differential PCIe receive signal
45	GND		PWR			
47	PCIE_1_L0_TX_N	D40	I			Negative differential PCIe receive signal
49	PCIE_1_L0_TX_P	D39	I			Positive differential PCIe receive signal
51	GND		PWR			
53	PCIE_1_CLK_N	D37	I			Negative differential PCIe reference clock signal
55	PCIE_1_CLK_P	D36	I			Positive differential PCIe reference clock signal
57	GND		PWR			
59	NC					Not connected
61	NC					Not connected
63	NC					Not connected
65	NC					Not connected
67	NC					Not connected
69	NC					Not connected
71	GND		PWR			
73	GND		PWR			
75	GND		PWR			

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Table 13: M.2 Key-M Connector (J43) (Continued)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
2	M2M_3V3		PWR	+3.3V		+3.3V Power input
4	M2M_3V3		PWR	+3.3V		+3.3V Power input
6	NC					Not connected
8	NC					Not connected
10	M2M_3V3		PWR	+3.3V		+3.3V Power input (LED)
12	M2M_3V3		PWR	+3.3V		+3.3V Power input
14	M2M_3V3		PWR	+3.3V		+3.3V Power input
16	M2M_3V3		PWR	+3.3V		+3.3V Power input
18	M2M_3V3		PWR	+3.3V		+3.3V Power input
20	NC					Not connected
22	NC					Not connected
24	NC					Not connected
26	NC					Not connected
28	NC					Not connected
30	NC					Not connected
32	NC					Not connected
34	NC					Not connected
36	NC					Not connected
38	NC					Not connected
40	NC					Not connected
42	NC					Not connected
44	NC					Not connected
46	NC					Not connected
48	NC					Not connected
50	PCIE_1_RESET#_3V	C38	I			PCIE 1 Reset signal
52	PCIE_1_CLKREQ	C37	O		27k to 1V8	PCIE 1 clock request
54	PCIE_WAKE#	C36	O			PCIE wake signal
56	NC					Not connected
58	NC					Not connected
68	NC					Not connected
70	M2M_3V3		PWR	+3.3V		+3.3V Power input
72	M2M_3V3		PWR	+3.3V		+3.3V Power input
74	M2M_3V3		PWR	+3.3V		+3.3V Power input

3.7 SD Card Interface (J30)

Table 14: SD Card 4-bit Connector (J30)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	SD_1_D3	A08	I/O			Serial Data 3
2	SD_1_CMD		I/O			Command
3	GND		PWR			
4	3V3_SD		PWR	+3.3V		SD Card power input
5	SD_1_CLK	A05	O			Serial Clock
6	GND		PWR			
7	SD_1_D0	A03	I/O			Serial Data 0
8	SD_1_D1	A02	I/O			Serial Data 1
9	SD_1_D2	A10	I/O			Serial Data 2
10	SD_1_CD#	A01	I			Card Detect
11	NC					Not Connected
12	GND		PWR			

3.8 Display Interface

The Aquila Development Board provides two options for connecting LCD panels and monitors via the following two interfaces supported:

- DisplayPort
- MIPI DSI

Almost any TFT display can be connected to the Aquila module by DisplayPort connector J27 or via the DSI interface connector J44. J44 features a universal mezzanine board connector. This solution allows for connecting various types of display interface mezzanine boards and converters, e.g., DSI to HDMI, DSI to LVDS, DSI to RGB, etc. Custom boards with the appropriate MIPI DSI connector can also be used.

3.8.1 DisplayPort Connector (J27)

Connector Type: DisplayPort Receptacle Connector, Right Angle, Molex 0472720001

Table 15: DisplayPort Connector (J27)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	DP__1_LANE0_P	A59	O			DisplayPort differential data lane 0, positive
2	GND		PWR			
3	DP__1_LANE0_N	A58	O			DisplayPort differential data lane 0, negative
4	DP__1_LANE1_P	A56	O			DisplayPort differential data lane 1, positive
5	GND		PWR			
6	DP__1_LANE1_N	A55	O			DisplayPort differential data lane 1, negative
7	DP__1_LANE2_P	A53	O			DisplayPort differential data lane 2, positive
8	GND		PWR			
9	DP__1_LANE2_N	A52	O			DisplayPort differential data lane 2, negative

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Table 15: DisplayPort Connector (J27) (Continued)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
10	DP__1_LANE3_P	A50	O			DisplayPort differential data lane 3, positive
11	GND		PWR			
12	DP__1_LANE3_N	A49	O			DisplayPort differential data lane 3, negative
13					100k pull-down	DisplayPort Consumer Electronic Control
14					100k pull-down	DisplayPort Consumer Electronic Control
15	DP__1_AUX_P	A47	O			DisplayPort differential auxiliary data, positive
16	GND		PWR			
17	DP__1_AUX_N	A46	O			DisplayPort differential auxiliary data, negative
18	DP_1_HPD_3V	B59	I	+3.3V	100k pull-down	Hot Plug Detect
19	GND					DisplayPort return
20	DP_3V3		PWR	+3.3V		
S1/S2/S3/S4	GND					

3.8.2 DSI Display Adapter Connector (J44)

Connector Type: Samtec LSS-130-03-L-DV-A-K-TR

Table 16: DSI Display Adapter Connector (J44)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Description
1	NC				Not connected
3	GND		PWR		
5	NC				Not connected
7	VIN_DSI		PWR	9-24V	
9	VIN_DSI		PWR	9-24V	
11	VIN_DSI		PWR	9-24V	
13	VIN_DSI		PWR	9-24V	
15	VIN_DSI		PWR	9-24V	
17	NC				Not connected
19	5V_S		PWR	+5V	
21	5V_S		PWR	+5V	
23	5V_S		PWR	+5V	
25	5V_S		PWR	+5V	
27	5V_S		PWR	+5V	
29	NC				Not connected
31	3V3		PWR	+3.3V	
33	3V3		PWR	+3.3V	
35	3V3		PWR	+3.3V	
37	3V3		PWR	+3.3V	
39	3V3		PWR	+3.3V	

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Table 16: DSI Display Adapter Connector (J44) (Continued)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Description
41	NC				Not connected
43	1V8		PWR	+1.8V	
45	1V8		PWR	+1.8V	
47	1V8		PWR	+1.8V	
49	1V8		PWR	+1.8V	
51	1V8		PWR	+1.8V	
53	NC				Not connected
55	GND		PWR		
57	CTRL_RESET_MOCI#	D05	I		Board peripheral RESET
59	CTRL_PWR_EN_MOCI	B95	I		Board peripheral Power Enable
2	NC				Not connected
4	I2C_3_DSI_SDA	B40	I/O		DSI adapters DDC Data
6	I2C_3_DSI_SCL	B41	I		DSI adapters DDC Clock
8	GPIO_17_DSI_1	B42	I		Dedicated general-purpose I/O for DSI display adapters
10	GND		PWR		
12	DSI__D0_P	A44	I/O		DSI Interface differential data lane 0, positive
14	DSI__D0_N	A43	I/O		DSI Interface differential data lane 0, negative
16	GND		PWR		
18	DSI__D1_P	A41	I/O		DSI Interface differential data lane 1, positive
20	DSI__D1_N	A40	I/O		DSI Interface differential data lane 1, negative
22	GND		PWR		
24	DSI__CLK_P	A38			DSI interface differential clock, positive
26	DSI__CLK_N	A37			DSI interface differential clock, negative
28	GND		PWR		
30	DSI__D2_P	A35	I/O		DSI Interface differential data lane 2, positive
32	DSI__D2_N	A34	I/O		DSI Interface differential data lane 2, negative
34	GND		PWR		
36	DSI__D3_P	A32	I/O		DSI Interface differential data lane 3, positive
38	DSI__D3_N	A31	I/O		DSI Interface differential data lane 3, negative
40	GND		PWR		
42	I2S_2_BCLK_DSI / GPIO_18_DSI_1	B26 / B43	I		Serial audio bit clock \verify
44	I2S_2_SYNC_DSI	B27	I		Synchronization/ field select/ left-right channel select
46	I2S_2_D_OUT_DSI / GPIO_19_DSI_1	B28 / B44	I		Serial audio output data \verify
48	I2S_2_D_IN_DSI	B29	O		Serial audio input data
50	GND		PWR		
52	I2C_3_DSI_SCL	B41	I		DSI adapters DDC Clock
54	I2C_3_DSI_SDA	B40	O		DSI adapters DDC Data
56	GPIO_20_DSI_1	B45	I		Dedicated general-purpose I/O for DSI display adapters

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Table 16: DSI Display Adapter Connector (J44) (Continued)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Description
58	PWM_3_DSI	B46	I		DSI Display adapters PWM brightness control
60	GND		PWR		

3.9 Audio

The Aquila Development Board offers two audio interfaces: an analog audio interface and a digital audio interface (routed to DSI display adapter connector J44).

3.9.1 Analog Audio

The Analog Audio interface is based on the WM8904CGEFL/RV audio codec IC from Cirrus Logic. For more detailed info, refer to the WM8904CGEFL/RV datasheet.

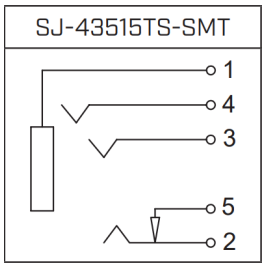
The Analog Audio interface is available on the connectors J46 and J69.

J46 is a 3.5 mm TRRS (stereo-plus-mic) audio jack connector for active loudspeakers or headphones and microphone input. The audio jack follows the CTIA (AHJ) pinout standard. page to view the compatible headphones list.

Table 17: Audio Jack (J46)

Pin	Signal name	I/O Type	3.5mm Jack pin	Description
1	HP_FB	I	Sleeve	Headphone feedback. Shorted to GND
2	HP_RIGHT	O	Tip	Headphone output (Right channel)
3	HP_LEFT	O	Ring	Headphone output (Left channel)
4	HP_MICIN	I	Ring	Microphone input (Left channel)
5	NC		Tip switch	Not connected

Figure 5: Audio Jack Pinout



3.9.2 Digital Audio

Digital audio on the Aquila Development Board is available as an I2S interface (I2S_2). It is provided on the J44 connector (MIPI DSI interface) to provide the option of using an audio interface along with display solutions. For detailed information, refer to DSI Display Adapter Connector (J44).

3.10 MIPI CSI Camera Interface

The MIPI CSI Camera Interfaces on connectors J70 and J71 are intended for applications requiring image capture capability from CMOS or CDD image sensors. For details, please see the relevant Aquila module datasheet.

3.10.1 MIPI CSI_1 Camera Connector (J70)

Connector Type: 24 Position FFC, FPC, vertical 0.5mm, Hirose FH12-24S-0.5SVA(54)

Table 18: MIPI CSI_1 Camera Connector (J70)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
2	CSI_C1_D0_N	A29	I/O			CSI differential data lane 0, negative
3	CSI_C1_D0_P	A28	I/O			CSI differential data lane 0, positive
4	GND		PWR			
5	CSI_C1_D1_N	A26	I			CSI differential data lane 1, negative
6	CSI_C1_D1_P	A25	I			CSI differential data lane 1, positive
7	GND		PWR			
8	CSI_C1_CLK_N	A23	I			CSI differential clock, negative
9	CSI_C1_CLK_P	A22	I			CSI differential clock, positive
10	GND		PWR			
11	CAM_1_CON_RST	B17	O			Camera RESET
12	CAM_1_CON_MCLK	A14	O			CSI camera master clock
13	I2C_4_CSI1_SCL	A13	O		4.7k to 3V3	CSI Camera I2 C bus Clock
14	I2C_4_CSI1_SDA	A12	I/O		4.7k to 3V3	CSI Camera I2 C bus Data
15	3V3		PWR	+3.3V		
16	CSI_C1_D2_N	A20	I			CSI differential data lane 2, negative
17	CSI_C1_D2_P	A19	I			CSI differential data lane 2, positive
18	GND		PWR			
19	CSI_C1_D3_N	A17	I			CSI differential data lane 3, negative
20	CSI_C1_D3_P	A16	I			CSI differential data lane 3, positive
21	5V_S		PWR	+5V		
22	CAM_1_CON_PWRDWN	B18	O			Camera Power Down
23	CAM_1_CON_IC_DETECT	A11	I		100k to GND	Camera Identification
24	CAM_1_CON_PWRCTRL	B19	O			Power Supply Control

3.10.2 MIPI CSI_2 Camera Connector (J71)

Connector Type: 24 Position FFC, FPC, vertical 0.5mm, Hirose FH12-24S-0.5SVA(54)

Table 19: MIPI CSI_2 Camera Connector (J71)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
2	CSI_C2_D0_N	B15	I/O			CSI differential data lane 0, negative
3	CSI_C2_D0_P	B14	I/O			CSI differential data lane 0, positive
4	GND		PWR			
5	CSI_C2_D1_N	B12	I			CSI differential data lane 1, negative
6	CSI_C2_D1_P	B11	I			CSI differential data lane 1, positive
7	GND		PWR			
8	CSI_C2_CLK_N	B09	I			CSI differential clock, negative
9	CSI_C2_CLK_P	B08	I			CSI differential clock, positive
10	GND		PWR			
11	CAM_2_CON_RST	C01	O			Camera RESET
12	CAM_2_CON_MCLK	A14	O			CSI camera master clock
13	I2C_5_CSI2_SCL	C06	O		4.7k to 3V3	CSI Camera I2 C bus Clock
14	I2C_5_CSI2_SDA	C05	I/O		4.7k to 3V3	CSI Camera I2 C bus Data
15	3V3		PWR	+3.3V		
16	CSI_C2_D2_N	B06	I			CSI differential data lane 2, negative
17	CSI_C2_D2_P	B05	I			CSI differential data lane 2, positive
18	GND		PWR			
19	CSI_C2_D3_N	B03	I			CSI differential data lane 3, negative
20	CSI_C2_D3_P	B02	I			CSI differential data lane 3, positive
21	5V_S		PWR	+5V		
22	CAM_2_CON_PWRDWN	C02	O			Camera Power Down
23	CAM_2_CON_IC_DETECT	C03	I		100k to GND	Camera Identification
24	CAM_2_CON_PWRCTRL	C04	O			Power Supply Control

3.11 Digital and Analog I/O

3.11.1 Communication Interface

3.11.1.1 CAN

The Aquila Development Board uses two non-isolated CAN transceivers and two isolated CAN transceivers. CAN buses are equipped with 120 ohm termination that is set through jumpers. The CAN bus signals are accessible on header J1.

The CAN Rx/Tx are 1V8 level

Table 20: Jumpers for CAN Interface

Jumper	Status	Function
J68	Closed	CAN1 split terminated, positive

Continued on next page

Table 20: Jumpers for CAN Interface (Continued)

Jumper	Status	Function
J74	Closed	CAN1 split terminated, negative
J89	Closed	CAN1 GND
J90	Closed	CAN1 5V
J73	Closed	CAN2 split terminated, positive
J75	Closed	CAN2 split terminated, negative
J85	Closed	CAN2 GND
J86	Closed	CAN2 5V
J29	Closed	CAN3 split terminated, negative
J49	Closed	CAN3 split terminated, positive
J79	Closed	CAN3 GND
J80	Closed	CAN3 5V
J45	Closed	CAN4 split terminated, negative
J64	Closed	CAN4 split terminated, positive
J81	Closed	CAN4 GND
J82	Closed	CAN4 5V

Table 21: CAN Bus pinout on connector J77, J78, J83, J84

J13 Pin number	Signal
1	NC
2	GND Jumper
3	CAN_N
4	CAN_P
5	120Ω to GND
6	NC
7	NC
8	5V Jumper
9	NC
10	NC

3.11.2 UART Interfaces

The Aquila Development Board features 2 UART interfaces that are connected to the following connectors:

- UART1 to the connector J67 through an RS232 transceiver.
- UART2 to the connector J20 through an RS485 transceiver.

3.11.2.1 RS232 Connector (J67)

Connector Type: D-Sub 9-pin Male, Amphenol Commercial Products L717SDEH09POL2RM8

Table 22: RS232 Connector (J67)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	NC					Not connected
2	UART_1_RXD	B35	I			RS232 Receive Data
3	UART_1_TXD	B37	O		10k to 1V8	RS232 Transmit Data
4	NC					Not connected
5	GND		PWR			
6	NC					Not connected
7	UART_1_RTS	B38	O		10k to 1V8	RS232 Request to Send (RTS)
8	UART_1_CTS	B36	I			RS232 Clear to Send (CTS)
9	NC					Not connected
10	GND		PWR			
11	GND		PWR			

3.11.2.2 RS485 Connector (J20)

Connector Type: 2 Position Wire to Board Terminal Block Connector, Würth Elektronik 691137710002

Table 23: RS485 Connector (J20)

Pin	Signal name	I/O Type	Description
1	RS485_A	I/O	Digital bus I/O, A
2	RS485_B	I/O	Digital bus I/O, B

3.12 Digital Interfaces

3.12.1 Switches / LEDs / Push-Buttons

The Aquila Development Board features four general-purpose green LEDs (D39, D40, D41, D42), four general-purpose switches (S1, S2, S3, S4), and four general-purpose buttons (B9, B10, B11, B12, with outputs B1, B2, B3, B4 respectively). They can be directly connected to the GPIO breakout connectors or specific custom hardware. Please note that the buttons and switches are not de-bounced.

3.12.1.1 Switches Connector (J53)

Connector Type: 1×4 Pin Header Female, 2.54 mm pitch, Wurth Elektronik 61300411821

Table 24: Switches Connector (J53)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down
1	S4_SW	O	+1.8V	510 to 1.8V, 86.6k to GND
2	S3_SW	O	+1.8V	510 to 1.8V, 86.6k to GND
3	S2_SW	O	+1.8V	510 to 1.8V, 86.6k to GND
4	S1_SW	O	+1.8V	510 to 1.8V, 86.6k to GND

3.12.1.2 LEDs Connector (J55)

Connector Type: 1×6 Pin Header Female, 2.54 mm pitch, Wurth Elektronik 61300611821

Table 25: LED Connector (J55)

Pin	Signal name	Linked LED	I/O Type	Voltage	Pull-up/Pull-down
1	GND				
2	LED4	D42	I	+1.8V	86.6k to GND
3	LED3	D41	I	+1.8V	86.6k to GND
4	LED2	D40	I	+1.8V	86.6k to GND
5	LED1	D39	I	+1.8V	86.6k to GND
6	1V8			+1.8V	

3.12.1.3 Push-button Connector (J50)

Connector Type: 1×4 Pin Header Female, 2.54 mm pitch, Wurth Elektronik 61300411821

Table 26: Push-button Connector (J50)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down
1	B9_SW	O	+1.8V	86.6k to GND
2	B10_SW	O	+1.8V	86.6k to GND
3	B11_SW	O	+1.8V	86.6k to GND
4	B12_SW	O	+1.8V	86.6k to GND

3.12.2 Level Shifters

Two level-shifters with push-pull outputs (U64, U62) and one with open-drain outputs (U83) have been placed on the Aquila Development Board. The I/O pins of these level shifters are connected to female pin headers J60, J61. These general-purpose level shifters can be used to connect external 3.3V compatible hardware with the jumper wires.

3.12.2.1 Level Shifter Connector (J60)

Connector Type: 1×10 Pin Header Female, 2.54 mm pitch, Wurth Elektronik 61301011821

Table 27: Level Shifter Connector (J60)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	LS_1V8_GPIO_1	O	+1.8V		General-purpose 1.8V level-shifted outputs
2	LS_1V8_GPIO_2	O	+1.8V		General-purpose 1.8V level-shifted outputs
3	LS_1V8_GPIO_3	O	+1.8V		General-purpose 1.8V level-shifted outputs
4	LS_1V8_GPIO_4	O	+1.8V		General-purpose 1.8V level-shifted outputs
5	LS_1V8_GPIO_5	I	+1.8V	10k to 1V8_B	General-purpose 1.8V level-shifted inputs
6	LS_1V8_GPIO_6	I	+1.8V	10k to 1V8_B	General-purpose 1.8V level-shifted inputs
7	LS_1V8_GPIO_7	I	+1.8V	10k to 1V8_B	General-purpose 1.8V level-shifted inputs
8	LS_1V8_GPIO_8	I	+1.8V	10k to 1V8_B	General-purpose 1.8V level-shifted inputs

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Table 27: Level Shifter Connector (J60) (Continued)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down	Description
9	LS_1V8_SCL	I/O (OD)	+1.8V	1.87k to 1V8_B	General-purpose 1.8V level-shifted bidirectional Inputs/Outputs with an Open Drain (OD) configuration
10	LS_1V8_SDA	I/O (OD)	+1.8V	1.87k to 1V8_B	General-purpose 1.8V level-shifted bidirectional Inputs/Outputs with an Open Drain (OD) configuration

3.12.2.2 Level Shifter Connector (J61)

Connector Type: 1×10 Pin Header Female, 2.54 mm pitch, Wurth Elektronik 61301011821

Table 28: Level Shifter Connector (J61)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	LS_3V3_GPIO_1	I	+3.3V		General-purpose 3.3V level-shifted inputs
2	LS_3V3_GPIO_2	I	+3.3V		General-purpose 3.3V level-shifted inputs
3	LS_3V3_GPIO_3	I	+3.3V		General-purpose 3.3V level-shifted inputs
4	LS_3V3_GPIO_4	I	+3.3V		General-purpose 3.3V level-shifted inputs
5	LS_3V3_GPIO_5	O	+3.3V	10k to 3V3_B	General-purpose 3.3V level-shifted outputs
6	LS_3V3_GPIO_6	O	+3.3V	10k to 3V3_B	General-purpose 3.3V level-shifted outputs
7	LS_3V3_GPIO_7	O	+3.3V	10k to 3V3_B	General-purpose 3.3V level-shifted outputs
8	LS_3V3_GPIO_8	O	+3.3V	10k to 3V3_B	General-purpose 3.3V level-shifted outputs
9	LS_3V3_SCL	I/O (OD)	+3.3V	1.87k to 3V3_B	General-purpose 3.3V level-shifted bidirectional Inputs/Outputs with an Open Drain (OD) configuration
10	LS_3V3_SDA	I/O (OD)	+3.3V	1.87k to 3V3_B	General-purpose 3.3V level-shifted bidirectional Inputs/Outputs with an Open Drain (OD) configuration

3.12.3 Analog Interface

The Analog inputs of an Aquila module are connected to the dedicated connector J48. For detailed information about ADC features, please refer to the respective Aquila module datasheet.

3.12.3.1 ADC Input (J48)

Connector Type: 2×3 Pin Header Female, 2.54 mm pitch, Wurth Elektronik 61300621821

Table 29: ADC Input (J48)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Description
1	ADC_4	D04	I (Analog)	+1.8V	Analog Input 4
2	ADC_3	D03	I (Analog)	+1.8V	Analog Input 3
3	ADC_2	D02	I (Analog)	+1.8V	Analog Input 2
4	ADC_1	D01	I (Analog)	+1.8V	Analog Input 1
5	PWR_1V8_MOCI	B96	PWR	+1.8V	SoM's 1.8V Power Output
6	GND		PWR		

3.13 Backup Battery

A backup battery holder (XB1) is available on the Aquila Development Board to provide backup power to the RTC of a Aquila module when the main power is turned off.

For more details on how the backup voltage is used, please refer to the respective Aquila computer-on-module datasheet.

A 10 mm (diameter) coin cell/battery should be used with the Battery Holder (XB1). A coin-cell battery can be used to provide power backup to the Aquila module RTC circuit when an external power supply is not available. Supported batteries: CR1025 or compatible coin-cell batteries.

3.14 Temperature Sensor

Aquila Development Board provides the Digital Temperature Sensor feature (TMP1075DSGR) with an I2C interface. The sensor is connected to the general-purpose I2C_1 bus. The default I2C address of the sensor is 0×4F. For details, please check the TMP1075DSGR sensor datasheet.

3.15 EEPROM

A 2-Kbit EEPROM (U55) with a I2C interface is installed on the Development Board. The EEPROM can be used to store important data or for board identification. For EEPROM's technical details, please check the M24C02-FDW6TP datasheet. The EEPROM is accessible at the address 0×57 on the generic serial bus I2C_1.

3.16 JTAG

The Aquila Development Board provides a JTAG interface to the JTAG port available on Aquila modules. Connector J59 provides an interface to an external JTAG device via a Cortex Debug Connector, which is a 10-pin 1.27mm header. The Aquila Development Board also has an on-board JTAG debugger feature. Please check the USB Debugger section of this datasheet and the Aquila Development Board schematic file for detailed information. This document is available on the Toradex developer website, on the Development Board Design page.

If an external JTAG debugger is used with a Aquila Development Board, jumper J58 should be removed. Simultaneous usage of the on-board and external JTAG Debugger is not allowed. Violating this requirement may damage the debugger or the Aquila Development Board.

3.16.1 JTAG Connector (J59)

Connector Type: 2×5 Pin Shrouded Header Male, 1.27mm, Samtec FTSH-105-01-L-DV-007-K

Table 30: JTAG Connector (J59)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	JTAG_1_VREF	C12	PWR	+1.8V		1.8V reference output for JTAG adapter
2	EXT_JTAG_TMS	C13	I			Test Mode Select
3	GND		PWR			
4	EXT_JTAG_TCK	C11	I			Test Clock
5	GND		PWR			
6	EXT_JTAG_TDO	C10	O			Test Data Out
7	NC					Not connected

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Table 30: JTAG Connector (J59) (Continued)

Pin	Signal name	BTB Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
8	EXT_JTAG_TDI	C08	I			Test Data In
9	GND		PWR			
10	CTRL_RESET_MICO		I (OD)			Aquila Module RESET

3.17 USB Debugger - FTDI

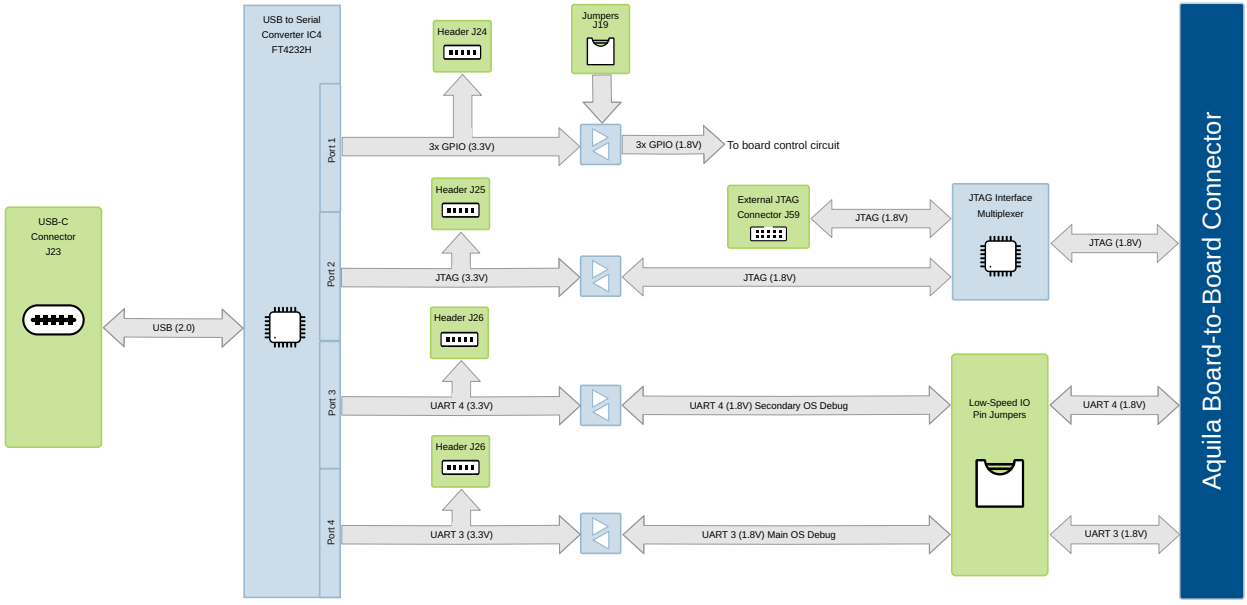
The Aquila Development Board provides an on-board Universal USB Debugger (U15). The debugger is based on the FT4232H chip and provides the following features:

- 2x UART ports connected to the Aquila Module's UART3 and UART4
  - UART3: Primary operating system debug port. Gives access to a Linux console
  - UART4: Secondary real-time OS debug port. Might also be used as a general purpose UART
- JTAG Debugger/Programmer
- 3x GPIO used for performing basic Development Board control features: Power ON/OFF, Reset and Recovery

For more information on the scope of each debug interface, please refer to the Aquila Family Specification.

The simplified USB Debugger architecture is shown below.

Figure 6: USB debugger architecture



The pin assignments of the FT4232HL are shown in the table below.

Table 31: FT4232HL pin assignments

Pin	Pin name	I/O Type	Interface	Connected/Controlled Net	Description
22	ADBUS5	O	GPIO	CTRL_RESET_MICO	Aquila Module RESET
23	ADBUS6	O	GPIO	CTRL_PWR_BTN_MICO	Aquila Development Board POWER ON/OFF
24	ADBUS7	O	GPIO	CTRL_RECOVERY_MICO	Aquila Module RECOVERY mode
26	ACBUS0	O	JTAG	JTAG_1_TCK	JTAG Test Clock
27	ACBUS1	O	JTAG	JTAG_1_TDI	JTAG Test Data Input
28	ACBUS2	I	JTAG	JTAG_1_TDO	JTAG Test Data Output
29	ACBUS3	O	JTAG	JTAG_1_TMS	JTAG Test Mode Select
30	ACBUS4	O	JTAG	JTAG1_TRST#	JTAG Test Mode Reset
38	BDBUS0	O	UART	UART4_RXD_3V	Receiver Data of RTOS debug or general purpose UART
39	BDBUS1	I	UART	UART4_TXD_3V	Transmitter Data of RTOS debug or general purpose UART
40	BDBUS2	I	UART	UART4_RTS_3V	Request to Send of RTOS debug or general purpose UART
41	BDBUS3	O	UART	UART4_CTS_3V	Clear to Send of RTOS debug or general purpose UART
48	BCBUS0	O	UART	UART3_RXD_3V	Receiver Data of Main OS debug UART
52	BCBUS1	I	UART	UART3_TXD_3V	Transmitter Data of Main OS debug UART
53	BCBUS2	I	UART	UART3_RTS_3V	Request to Send of Main OS debug UART
54	BCBUS3	O	UART	UART3_CTS_3V	Clear to Send of Main OS debug UART

The debug interface is accessible via the separate USB-C connector J23.

3.17.1 USB Debugger Connector (J23)

Connector Type: USB-C, Amphenol ICC 12401826E412A

Table 32: USB Debugger Connector (J23)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down	Description
A1	GND	PWR			
A2	NC				Not connected
A3	NC				Not connected
A4	VBUS	PWR	+3.3V		
A5	FTUSB_CC1			5.1k to GND	Type-C configuration channel signal 1
A6	FTUSB_P	I/O			Positive Differential USB 2.0 Signal
A7	FTUSB_N	I/O			Negative Differential USB 2.0 Signal
A8	NC				Not connected
A9	VBUS	PWR	+3.3V		
A10	NC				Not connected
A11	NC				Not connected
A12	GND	PWR			
B1	GND	PWR			
B2	NC				Not connected

Continued on next page

Table 32: USB Debugger Connector (J23) (Continued)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down	Description
B3	NC				Not connected
B4	VBUS	PWR	+3.3V		
B5	FTUSB_CC2			5.1k to GND	Type-C configuration channel signal 2
B6	FTUSB_P	I/O			Positive Differential USB 2.0 Signal
B7	FTUSB_N	I/O			Negative Differential USB 2.0 Signal
B8	NC				Not connected
B9	VBUS	PWR	+3.3V		
B10	NC				Not connected
B11	NC				Not connected
B12	GND	PWR			
SH1/SH2/SH3/SH4	GND	PWR		1M to GND	

3.18 Low-Speed IO Pins Configuration

The Low-speed IO pins' breakout connectors provide flexibility in routing the IO pins of the Aquila module. You can map them either:

- To the on-board function
- To external hardware

The default setting uses a straight-through jumper configuration: The A row is directly connected to the B row.

All signals on the male header are also available on a parallel female connector, which allows for:

- Easy measurement
- Probing
- Signal re-routing

To map the BTB Pin to its corresponding SoC ball name, refer to the datasheet of the specific Aquila module you are using, as this mapping is module-specific.

3.18.1 Low-Speed IO Pins (Left-side headers)

Connector Types:

- 2×30Pin Male, 2.54mm
- 1×30Pin Female, 2.54mm

Figure 7: Aquila Development Board connectors and controls

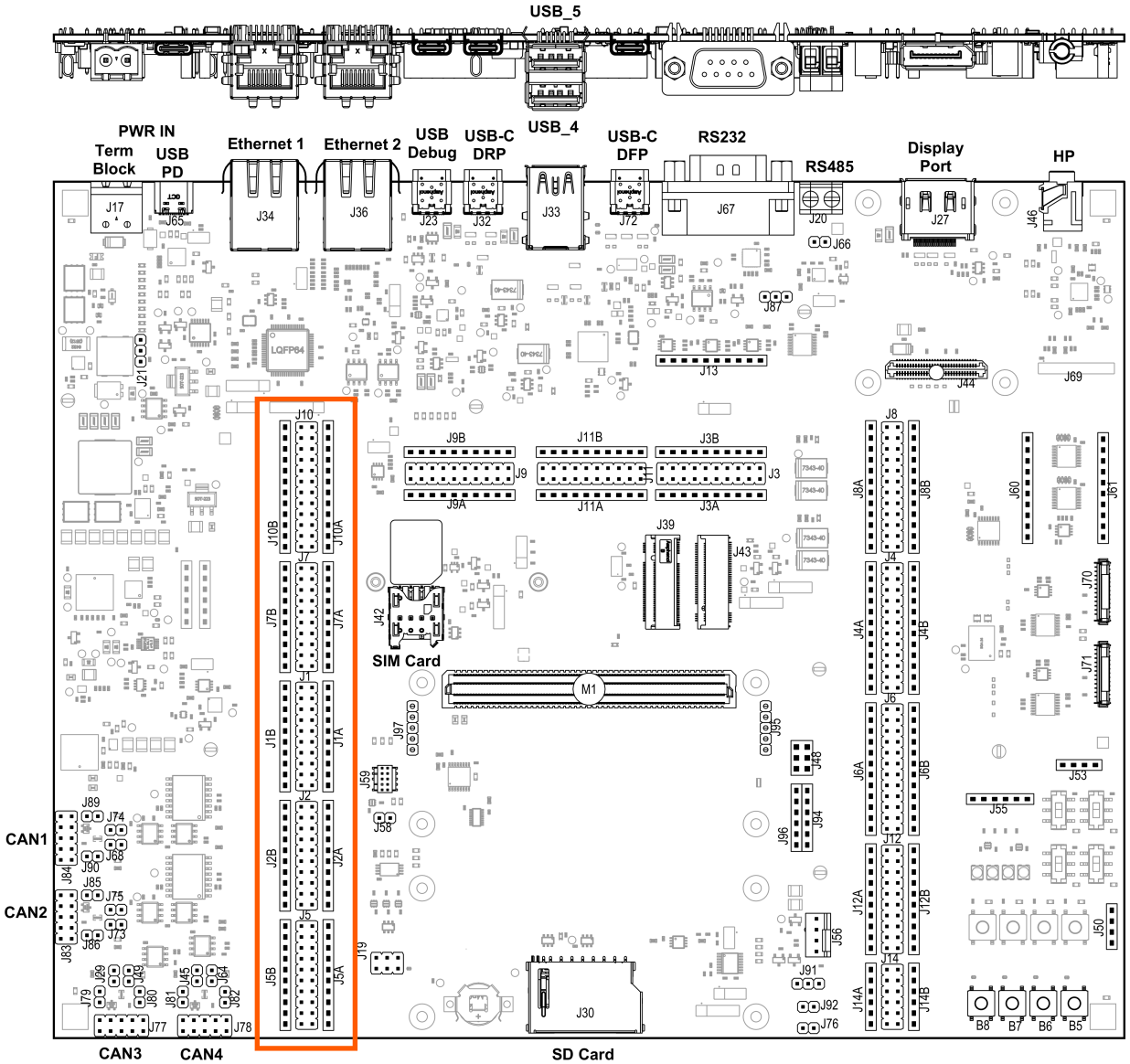


Table 33: Low-speed IO pins (Left-side headers)

BTB Pin	Signal Name (SoM)	Signal Name (Peripheral)	I/O Type	Voltage	Pull-up/Pull-down	Description
B46	AQUILA_B46	PWM_3_DSI	O			DSI Display adapter's PWM brightness control
B45	AQUILA_B45	GPIO_20_DSI_1	I/O			Dedicated general-purpose I/O reserved for DSI_1 display adapter
B44	AQUILA_B44	GPIO_19_DSI_1	I/O			Dedicated general-purpose I/O reserved for DSI_1 display adapter
B43	AQUILA_B43	GPIO_18_DSI_1	I/O			Dedicated general-purpose I/O reserved for DSI_1 display adapter
B42	AQUILA_B42	GPIO_17_DSI_1	I/O			Dedicated general-purpose I/O reserved for DSI_1 display adapter
B58	AQUILA_B58	PWM_4_DP	O			DisplayPort adapter's PWM
B40	AQUILA_B40	I2C_3_DSI1_SDA_A	I/O		1.87k to 1V8	DSI display adapter DDC Data
B41	AQUILA_B41	I2C_3_DSI1_SCL_A	O		1.87k to 1V8	DSI display adapter DDC Clock
B40	AQUILA_B40	I2C_3_DSI1_SDA_B	I/O		1.87k to 1V8	DSI display adapter DDC Data
B41	AQUILA_B41	I2C_3_DSI1_SCL_B	O		1.87k to 1V8	DSI display adapter DDC Clock
D12	AQUILA_D12	SPI_1_CLK	O			SPI Serial Clock
D09	AQUILA_D09	SPI_1_CS	O			SPI Slave Select
D10	AQUILA_D10	SPI_1_MISO	O			SPI Master Input, Slave Output
D11	AQUILA_D11	SPI_1_MOSI	O			SPI Master Output, Slave Input
D14	AQUILA_D14	SPI_2_CLK	O			SPI Serial Clock
D16	AQUILA_D16	SPI_2_CS	O			SPI Slave Select
D15	AQUILA_D15	SPI_2_MISO	O			SPI Master Input, Slave Output
D17	AQUILA_D17	SPI_2_MOSI	O			SPI Master Output, Slave Input
C15	AQUILA_C15	CTRL_TAMPER1				??
C14	AQUILA_C14	CTRL_TAMPER0				??
C25	AQUILA_C25	PWM_1	O			General-purpose PWM
C26	AQUILA_C26	PWM_2	O			General-purpose PWM
B48	AQUILA_B48	CAN_1_TX	O			CAN port 1 transmit pin

Continued on next page

Table 33: Low-speed IO pins (Left-side headers) (Continued)

BTB Pin	Signal Name (SoM)	Signal Name (Peripheral)	I/O Type	Voltage	Pull-up/Pull-down	Description
B49	AQUILA_B49	CAN_1_RX	I			CAN port 1 receive pin
B50	AQUILA_B50	CAN_2_TX	O			CAN port 2 transmit pin
B51	AQUILA_B51	CAN_2_RX	I			CAN port 2 receive pin
B53	AQUILA_B53	CAN_3_TX	O			CAN port 3 transmit pin
B54	AQUILA_B54	CAN_3_RX	I			CAN port 3 receive pin
B55	AQUILA_B55	CAN_4_TX	O			CAN port 4 transmit pin
B56	AQUILA_B56	CAN_4_RX	I			CAN port 4 receive pin
B91	AQUILA_B91	CTRL_RECOVERY_MICO#	I (OD)			SoM RECOVERY mode control
B92	AQUILA_B92	CTRL_RESET_MICO#	I (OD)			SoM's RESET signal
B93	AQUILA_B93	CTRL_PWR_BTN_MICO#	I			SoM POWER button control input
B94	AQUILA_B94	CTRL_FORCE_OFF_MOCI#	O			General board FORCE OFF control
B95	AQUILA_B95	CTRL_PWR_EN_MOCI	O			Power enable for the on-board peripherals
D05	AQUILA_D05	CTRL_RESET_MOCI#	O			Reset for the on-board peripherals
D06	AQUILA_D06	CTRL_WAKE1_MICO#	I			Wake-capable signal to resume SoM from SLEEP mode
A14	AQUILA_A14	CTRL_MCLK_MOCI	O ??			General board Master Clock signal ??
	1V8	1V8	PWR	+1.8V		+1.8V Power supply output
	GND	GND	PWR			
D07	AQUILA_D07	I2C_1_SDA_TEMPSNSR	I/O			Temperature Sensor signal Data
D08	AQUILA_D08	I2C_1_SCL_TEMPSNSR	O			Temperature Sensor signal Clock
D07	AQUILA_D07	I2C_1_SDA_EEPROM	I/O			EEPROM memory signal Data
D08	AQUILA_D08	I2C_1_SCL_EEPROM	O			EEPROM memory signal Clock
D07	AQUILA_D07	I2C_1_SDA_USBC_CTRL	I/O			USB-C Control signal Data
D08	AQUILA_D08	I2C_1_SCL_USBC_CTRL	O			USB-C Control signal Clock

Continued on next page

Table 33: Low-speed IO pins (Left-side headers) (Continued)

BTB Pin	Signal Name (SoM)	Signal Name (Peripheral)	I/O Type	Voltage	Pull-up/Pull-down	Description
D07	AQUILA_D07	I2C_1_SDA_FANCTRL	I/O			Fan Control signal Data
D08	AQUILA_D08	I2C_1_SCL_FANCTRL	O			Fan Control signal Clock
D07	AQUILA_D07	I2C_1_SDA_PWRMES	I/O			Power measurement signal Data
D08	AQUILA_D08	I2C_1_SCL_PWRMES	O			Power measurement signal Clock
D07	AQUILA_D07	I2C_1_SDA_AUD	I/O			Audio codec signal Data
D08	AQUILA_D08	I2C_1_SCL_AUD	O			Audio codec signal Clock

3.18.2 Low-Speed IO Pins (Upper headers)

Connector Types:

- 2×30Pin Male, 2.54mm
- 1×30Pin Female, 2.54mm

Figure 8: Aquila Development Board connectors and controls

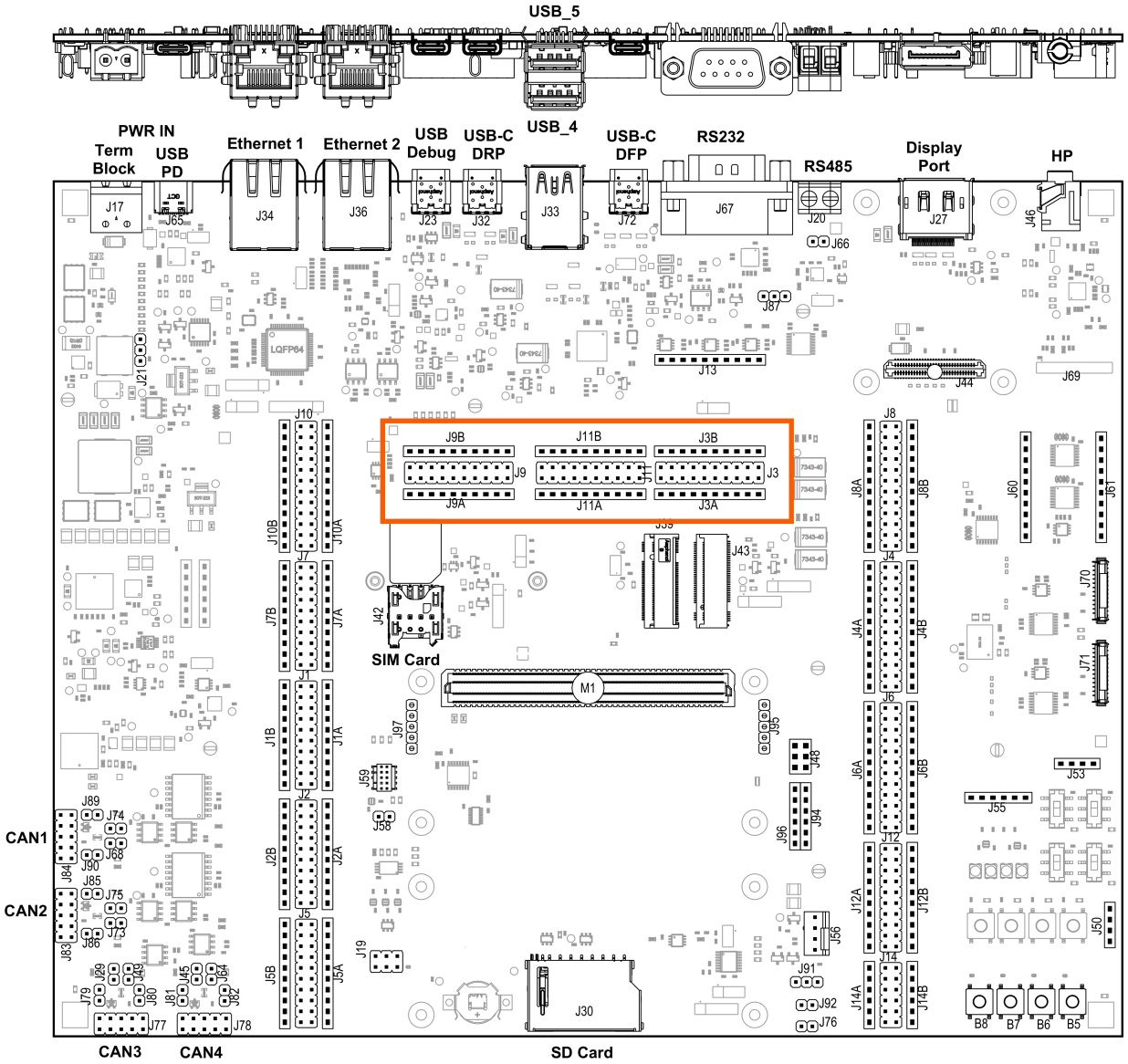


Table 34: Low-speed IO pins (Upper headers)

BTB Pin	Signal Name (SoM)	Signal Name (Peripheral)	I/O Type	Voltage	Pull-up/Pull-down	Description
D23	AQUILA_D23	GPIO_01	I/O			General-purpose I/O
D24	AQUILA_D24	GPIO_02	I/O			General-purpose I/O
D25	AQUILA_D25	GPIO_03	I/O			General-purpose I/O
C20	AQUILA_C20	GPIO_04	I/O			General-purpose I/O
C21	AQUILA_C21	GPIO_05	I/O			General-purpose I/O
C22	AQUILA_C22	GPIO_06	I/O			General-purpose I/O
C23	AQUILA_C23	GPIO_07	I/O			General-purpose I/O
C24	AQUILA_C24	GPIO_08	I/O			General-purpose I/O
B96	AQUILA_B96	PWR_1V8_MOCI	PWR	+1.8V		+1.8V SoM power output
	GND	GND	PWR			
D07	AQUILA_D07	I2C_1_TRNS_SDA	I/O		10k to 1V8	I2C 1 Voltage Translator Data
D08	AQUILA_D08	I2C_1_TRNS_SCL	O		10k to 1V8	I2C 1 Voltage Translator Clock
C16	AQUILA_C16	I2C_2_TRNS_SDA	I/O		4.7k to 1V8	I2C 2 Voltage Translator Data
C17	AQUILA_C17	I2C_2_TRNS_SCL	O		4.7k to 1V8	I2C 2 Voltage Translator Clock
C18	AQUILA_C18	I2C_6_TRNS_SDA	I/O		4.7k to 1V8	I2C 6 Voltage Translator Data
C19	AQUILA_C19	I2C_6_TRNS_SCL	O		4.7k to 1V8	I2C 6 Voltage Translator Clock
C16	AQUILA_C16	I2C_2_SDA	I/O		4.7k to 1V8	General purpose I2C 2 Data
C17	AQUILA_C17	I2C_2_SCL	O		4.7k to 1V8	General purpose I2C 2 Clock
C18	AQUILA_C18	I2C_6_SDA	I/O		4.7k to 1V8	General purpose I2C 6 Data
C19	AQUILA_C19	I2C_6_SCL	O		4.7k to 1V8	General purpose I2C 6 Clock
B74	AQUILA_B74	USB_1_INT#	I			USB 1 interrupt signal
B75	AQUILA_B75	USB_1_OC#	I			USB 1 over-current signal
B76	AQUILA_B76	USB_1_VBUS	I			USB 1 power supply output

Continued on next page

Table 34: Low-speed IO pins (Upper headers) (Continued)

BTB Pin	Signal Name (SoM)	Signal Name (Peripheral)	I/O Type	Voltage	Pull-up/Pull-down	Description
B77	AQUILA_B77	USB_1_EN	O			USB 1 enable signal
B80	AQUILA_B80	USB_2_EN	O			USB 2 enable signal
B24	AQUILA_B24	I2S_1_MCLK	O			I2S (audio codec) Master Clock
B23	AQUILA_B23	I2S_1_D_IN	I			I2S (audio codec) Field Select (Transmit Frame Sync)
B22	AQUILA_B22	I2S_1_D_OUT	O			I2S (audio codec) Data Output
B21	AQUILA_B21	I2S_1_SYNC	O			I2S (audio codec) Data Input
B20	AQUILA_B20	I2S_1_BCLK	O			I2S (MIPI DSI) Serial Clock (Transmit Bit Clock)

3.18.3 Low-Speed IO Pins (Right-side headers)

Connector Types:

- 2×30Pin Male, 2.54mm
- 1×30Pin Female, 2.54mm

Figure 9: Aquila Development Board connectors and controls

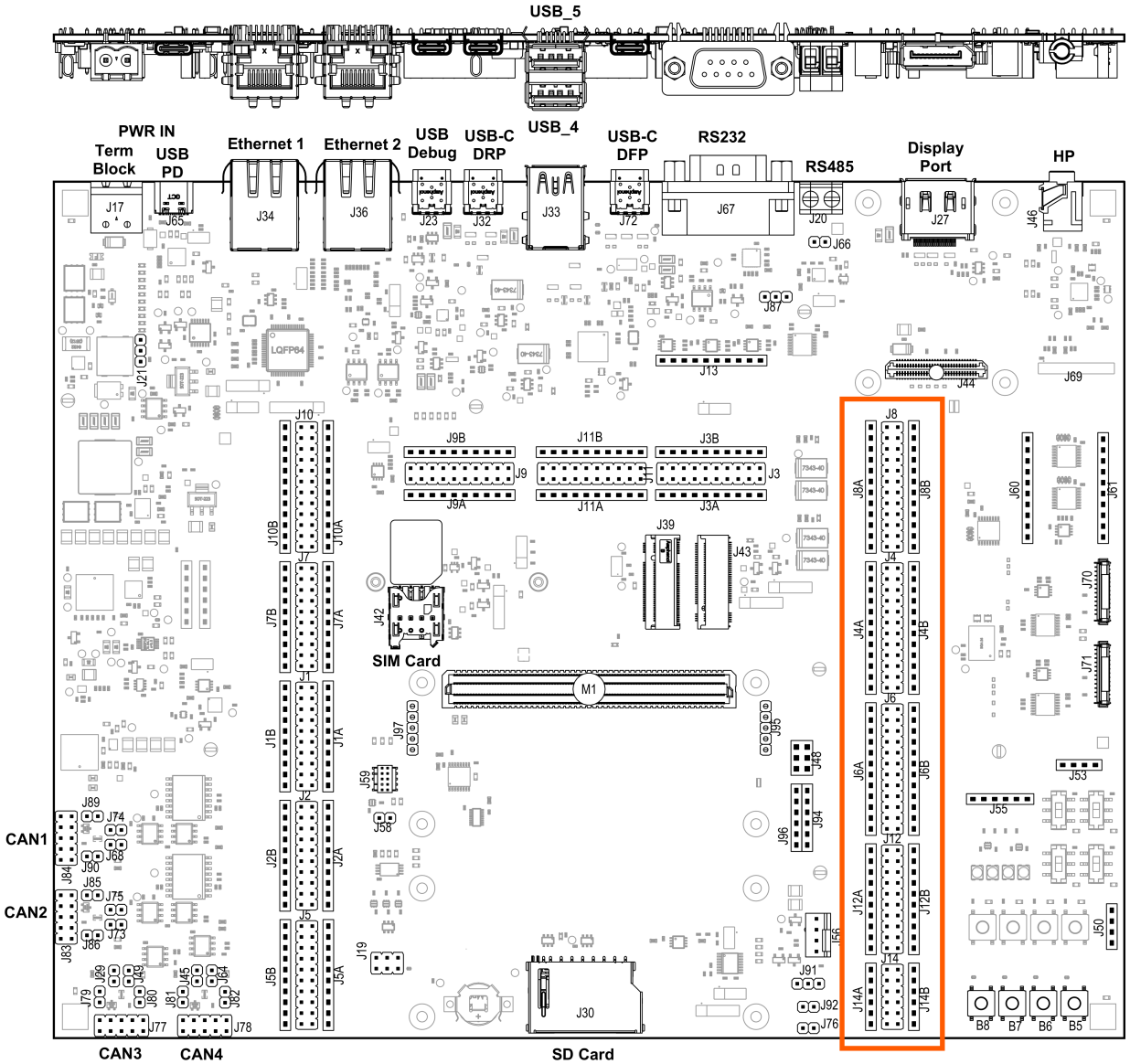


Table 35: Low-speed IO pins (Right-side headers)

BTB Pin	Signal Name (SoM)	Signal Name (Peripheral)	I/O Type	Voltage	Pull-up/Pull-down	Description
B35	AQUILA_B35	UART_1_RXD	I			UART_1 Receive Data
B37	AQUILA_B37	UART_1_TXD	O			UART_1 Transmit Data
B38	AQUILA_B38	UART_1_RTS	O			UART_1 Request to Send (RTS)
B36	AQUILA_B36	UART_1_CTS	I			UART_1 Clear to Send (CTS)
B31	AQUILA_B31	UART_2_RXD	I			UART_2 Receive Data
B33	AQUILA_B33	UART_2_TXD	O			UART_2 Transmit Data
B34	AQUILA_B34	UART_2_RTS	O			UART_2 Request to Send (RTS)
B36	AQUILA_B36	UART_2_CTS	I			UART_2 Clear to Send (CTS)
D19	AQUILA_D19	UART_3_RXD	I			Main OS UART Receive Data
D20	AQUILA_D20	UART_3_TXD	O			Main OS UART Transmit Data
D21	AQUILA_D21	UART_4_RXD	I			Real time OS debug Receive Data
D22	AQUILA_D22	UART_4_TXD	O			Real time OS debug Transmit Data
B73	AQUILA_B73	OSPI_1_IO7	I/O			
B72	AQUILA_B72	OSPI_1_IO6	I/O			
B71	AQUILA_B71	OSPI_1_IO5	I/O			
B70	AQUILA_B70	OSPI_1_IO4	I/O			
B60	AQUILA_B60	QSPI_1_IO3	I/O			QSPI Serial I/Os for command, address, and data
B61	AQUILA_B61	QSPI_1_IO2	I/O			QSPI Serial I/Os for command, address, and data
B67	AQUILA_B67	QSPI_1_IO1	I/O			QSPI Serial I/Os for command, address, and data
B68	AQUILA_B68	QSPI_1_IO0	I/O			QSPI Serial I/Os for command, address, and data
B66	AQUILA_B66	QSPI_1_CS1#	O			QSPI Chip Select 1
B62	AQUILA_B62	QSPI_1_CS2#	O			QSPI Chip Select 2
B63	AQUILA_B63	QSPI_1_DQS	I			QSPI Data Strobe signal

Continued on next page

Table 35: Low-speed IO pins (Right-side headers) (Continued)

BTB Pin	Signal Name (SoM)	Signal Name (Peripheral)	I/O Type	Voltage	Pull-up/Pull-down	Description
B65	AQUILA_B65	QSPI_1_SCK	O			QSPI Serial Clock
B17	AQUILA_B17	GPIO_09_CSI_1	I/O			General-purpose I/Os dedicated for the CSI 1 camera interface
B18	AQUILA_B18	GPIO_10_CSI_1	I/O			General-purpose I/Os dedicated for the CSI 1 camera interface
A11	AQUILA_A11	GPIO_11_CSI_1	I/O			General-purpose I/Os dedicated for the CSI 1 camera interface
B19	AQUILA_B19	GPIO_12_CSI_1	I/O			General-purpose I/Os dedicated for the CSI 1 camera interface
A12	AQUILA_A12	I2C_4_CSI1_SDA	I/O		1.87k to 1V8	CSI 1 Camera control I2C bus Data
A13	AQUILA_A13	I2C_4_CSI1_SCL	O		1.87k to 1V8	CSI 1 Camera control I2C bus Clock
C04	AQUILA_C04	GPIO_16_CSI_2	I/O			General-purpose I/Os dedicated for the CSI 2 camera interface
C03	AQUILA_C03	GPIO_15_CSI_2	I/O			General-purpose I/Os dedicated for the CSI 2 camera interface
C02	AQUILA_C02	GPIO_14_CSI_2	I/O			General-purpose I/Os dedicated for the CSI 2 camera interface
C01	AQUILA_C01	GPIO_13_CSI_2	I/O			General-purpose I/Os dedicated for the CSI 2 camera interface
C05	AQUILA_C05	I2C_5_CSI2_SDA	I/O		1.87k to 1V8	CSI 2 Camera control I2C bus Data
C06	AQUILA_C06	I2C_5_CSI2_SCL	O		1.87k to 1V8	CSI 2 Camera control I2C bus Clock
B26	AQUILA_B26	I2S_2_BCLK_DSI	O			I2S (MIPI DSI) Serial Clock (Transmit Bit Clock)
B27	AQUILA_B27	I2S_2_SYNC_DSI	O			I2S (MIPI DSI) Field Select (Transmit Frame Sync)
B28	AQUILA_B28	I2S_2_D_OUT_DSI	O			I2S (MIPI DSI) Data Output
B29	AQUILA_B29	I2S_2_D_IN_DSI	I			I2S (MIPI DSI) Data Input
B26	AQUILA_B26	I2S_2_BCLK_M2B	O			I2S (M.2 B-Key) Serial Clock (Transmit Bit Clock)
B27	AQUILA_B27	I2S_2_SYNC_M2B	O			I2S (M.2 B-Key) Field Select (Transmit Frame Sync)
B28	AQUILA_B28	I2S_2_D_OUT_M2B	O			I2S (M.2 B-Key) Data Output
B29	AQUILA_B29	I2S_2_D_IN_M2B	I			I2S (M.2 B-Key) Data Input
	1V8	1V8	PWR	+1.8V		+1.8V Power supply output
	GND	GND	PWR			

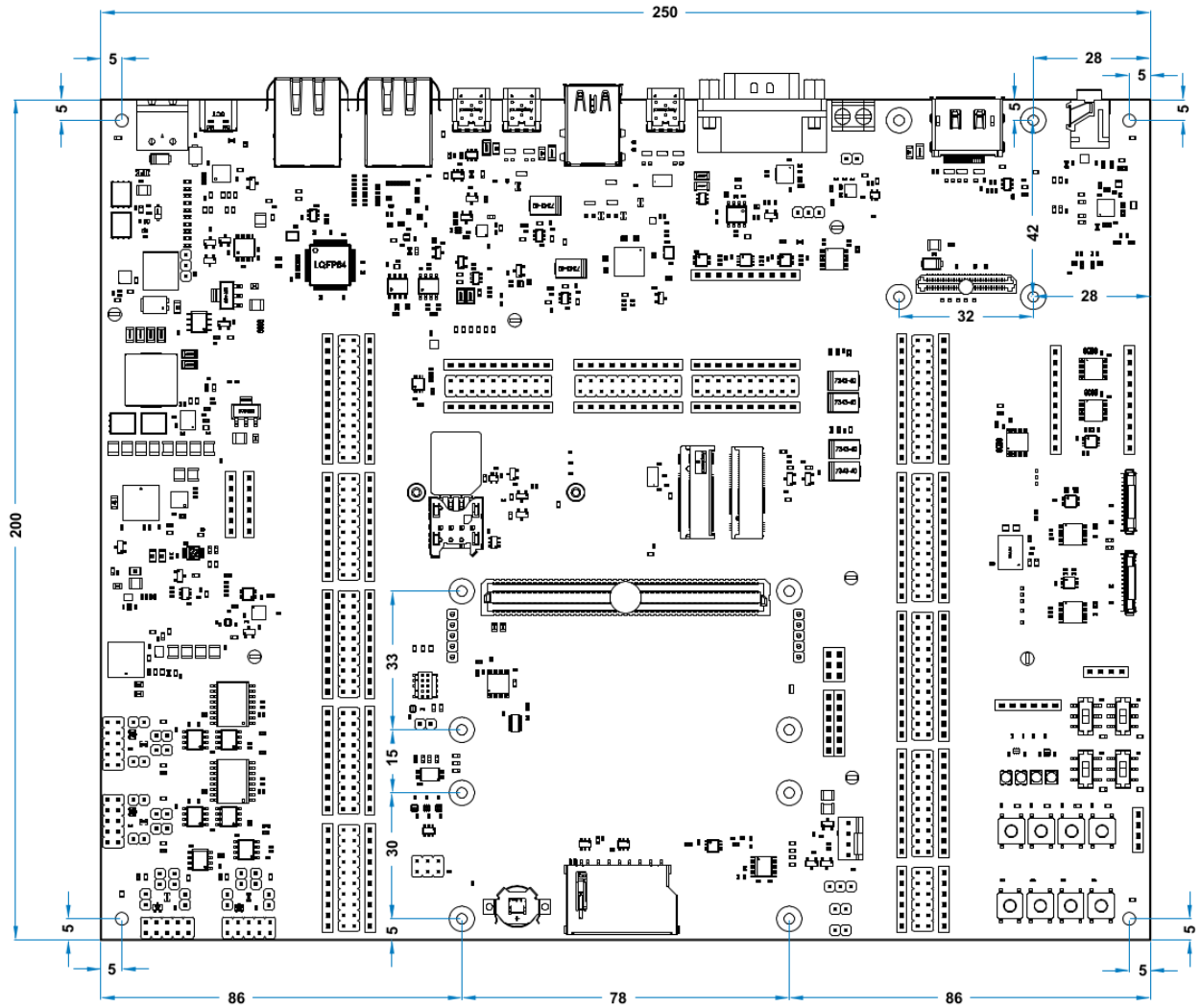
Continued on next page

Table 35: Low-speed IO pins (Right-side headers) (Continued)

BTB Pin	Signal Name (SoM)	Signal Name (Peripheral)	I/O Type	Voltage	Pull-up/Pull-down	Description
C37	AQUILA_C37	PCIE_1_CLKREQ				PCIe 1 clock request
C38	AQUILA_C38	PCIE_1_RESET#				PCIe 1 reset signal
C36	AQUILA_C36	PCIE_WAKE#				PCIe wake signal
C34	AQUILA_C34	PCIE_2_CLKREQ				PCIe 2 clock request
C35	AQUILA_C35	PCIE_2_RESET#				PCIe 2 reset signal
	GND	GND	PWR			

4 Mechanical Data

Figure 10: Aquila Development Board dimensions (in millimeters)



5 Design Data

The design data for Toradex Development Boards is freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.

To download the Development Board design data, please use the link below: http://developer.toradex.com/carrier-board-design

6 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Minerals, REACH, etc. can be found on our website.

7 Device and Documentation Support

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