OSDZU3 Datasheet

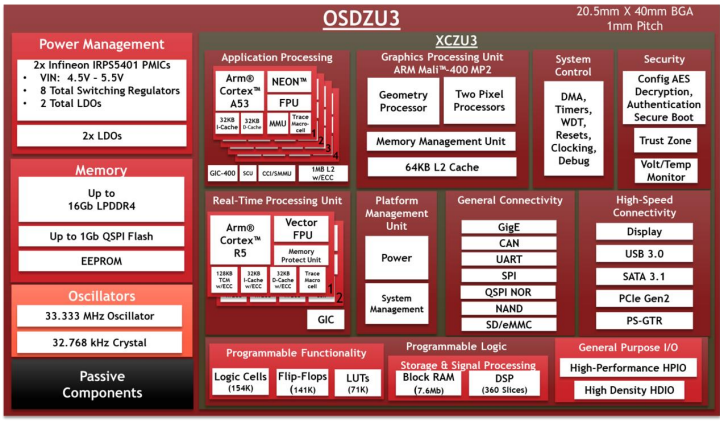
Rev. 4.0 12/1/2024

Introduction

The OSDZU3 System-in-Package (SiP) device is based on Zynq® UltraScale+™ MPSoC. This device integrates a feature-rich 64-bit quad-core Arm®-A53 and dual-core Arm Cortex®-R5 based processing system (PS) and AMD programmable logic (PL) UltraScale architecture, along with LPDDR4, QSPI and power management into a single package.

Specifically, OSDZU3 integrates Zynq UltraScale+ ZU3 MPSoC, LPDDR4, QPSI flash memory, two Infineon IRPS5401 Power Management ICs (PMICs), two LDO power supplies, an EEPROM, 2 Oscillators, and associated passives into a single easy to use BGA package.

This integration enables faster designs with the AMD ZU3 MPSoC by removing the tedious design tasks that do not add value to an end system while allowing low cost-manufacturing and miniaturized products.



Features

- Integrated into the OSDZU3 SiP are an AMD ZU3 device, two IRPS5401s, up to 16Gb (2GB) LPDDR4, up to 1Gb (128MB) QSPI Flash, EEPROM, two oscillators and passive components.
- ZU3 Features:
  - Quad-core Arm® Cortex®-A-53 processors up to 1.5 GHz
  - Dual-core Arm® Cortex®-R5 based real-time processing unit (RPU) up to 600 MHz
  - Programmable Logic (PL) Array with 154,350 System Logic Cells, 141,120 CLB flip-flops, 70,560 CLB LUTs and 360 DSP slices
  - 2Mb on-chip RAM (OCM) in the PS with ECC
  - 7.6Mb on-chip RAM (block RAM) with ECC (PL)
  - 1.8Mb on-Chip RAM (distributed RAM) (PL)
- Access to all I/O Signals of the ZU3 SFVC784 (784 Pin) Package
- LPDDR4
- QSPI Flash
- 33.333 MHz Oscillator
- 32.768 kHz Crystal Oscillator
- Single Voltage Input: 4.5V-5.5V
- 4 System Usable Power Outputs

Benefits

- Single power input
- Low-cost PCB design
- Compatible with ZU3 development tools and software
- Significantly reduces design time
- Decreases layout complexity
- Optimized BGA ball layout allows low-cost assembly
- Simplifies component sourcing
- Increased reliability through reduced number of components

Package

- Temp Range: 0° to 85°C, -40° to 85°C, -40° to 100°C
- Size: 20.5mm x 40mm
- BGA pitch: 1mm

Table of Contents

1 Revision History

Revision Number	Revision Date	Changes	Author
1.0	9/22/2023	Initial Production Release	Neeraj Dantu, Eshtaartha Basu
2.0	12/15/2023	Update to Integrated Resistors Table also addressed Typos	Neeraj Dantu
3.0	3/7/2024	Updated Table 4-3 to show Capacitance of B/I Devices and H Devices, updated recommended external capacitance and corrected footnote #1 on Table 4-4, Added Section for PMIC Switching Frequency, Added section on Part Marking	Neeraj Dantu, Greg Sheridan
3.1	3/13/2024	Updated the Total Capacitance column in Table 4-4 so it matches the required capacitor values for PMIC2_VOUT_D. Fixed a number of small typos	Greg Sheridan
4.0	12/1/2024	Updated Storage Requirements	Greg Sheridan

NOTICE: These devices are susceptible to moisture and are classified as **MSL 4**. Ensure you are following the guidelines in the **Storage Requirements** section in this document.

2 Product Number Information

Figure 2-1 shows an example of an orderable product number for the OSDZU3 family. This section explains the different sections of the product number. It also lists the valid entries and their meaning for each designator.

Figure 2-1 - Example Product Number

Product Designator – Three letters that designate the family of device. Table 2-1 shows the family designator.

Table 2-1 - Family Designator

Family Designator	Product Line
OSD	OSD Product Line.

Processor Designator – A set of letters and numbers that designate the specific processor in the device. Table 2-2 shows the valid values for the Processor Designator.

Table 2-2 - Processor Designators

Processor Designator	Processor
ZU3	AMD ZU3

Device Designator – A set of letters that designate the specific device in the AMD Processor family. Table 2-3 shows the valid values for the Device Designator.

Table 2-3 - Device Designators

Device Designator	Processor
EG	AMD ZU3EG

Speed Designator – A set of letters and numbers that designate the speed grade of the ZU3 device. The speed grades are equivalent to the AMD speed grades unless otherwise stated. Table 2-4 shows the valid values for the Speed Designator.

Table 2-4 - Speed Designator

Speed Designator	Speed
1	AMD -1 Speed Grade

Memory Designator – A set of letters and numbers that designate the LPDDR4 memory size in the device. Table 2-5 shows the valid values for the Memory Designator.

Table 2-5 - Memory Designator

Memory Designator	DDR Memory Size
2G	2GB LPDDR4 (x32)

Temp Designator – A letter or number that designates the operating junction temperature range of the device. Table 2-6 shows the valid values for the Temp Designator.

Table 2-6 - Temp Designator

Temp Designator	Temperature Range
B	Commercial: 0 to 85°C
I	Industrial: -40 to 85°C
H	Industrial Extended High: -40 to 100°C

Option Designator – A set of two letters or numbers that designates the set of features in the device. Table 2-7 shows the valid values for the Option Designator unique for the OSDZU3 devices.

Table 2-7 - Option Designator

Option Designator	Device Options
FA-ES	Engineering Sample Device – See ES Sample Errata for variations from this datasheet. 33.333 MHz Main Oscillator, 4KB EEPROM, 128MB NAND QSPI @ 3.3V, 32.768 kHz RTC Crystal Oscillator
FA	33.333 MHz Main Oscillator, 4KB EEPROM, 32MB NOR QSPI @ 3.3V, 32.768 kHz RTC Crystal Oscillator
FB	33.333 MHz Main Oscillator, 4KB EEPROM, 32MB NOR QSPI @ 1.8V, 32.768 kHz RTC Crystal Oscillator

3 Reference Documents

3.1 Data Sheets

Table 3-1 lists links to documents for the key devices used in the OSDZU3. Please refer to them for specifics on each device. The remainder of this document will describe how the devices are used in the OSDZU3 system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSDZU3.

Table 3-1 - Integrated Component Reference Documents

Component	Type	Document	Link
ZU3	**Processor**	Data Sheet	https://www.xilinx.com/support/documentation/data_sheets/ds891-zynq-ultrascale-plus-overview.pdf
		Functional Details	https://www.xilinx.com/support/documentation/user_guides/ug1085-zynq-ultrascale-trm.pdf
		PCB Design Guide	https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf
		DC and AC specification	https://www.xilinx.com/support/documentation/data_sheets/ds925-zynq-ultrascale-plus.pdf
		I/O options	https://www.xilinx.com/support/documentation/user_guides/ug571-ultrascale-selectio.pdf
		ZU3 Package, Reflow, Thermal specifications	https://www.xilinx.com/support/documentation/user_guides/ug1075-zynq-ultrascale-pkg-pinout.pdf
		Device Registers Reference	https://docs.xilinx.com/r/en-US/ug1087-zynq-ultrascale-registers/Overview
IRPS5401	**PMIC**	Data Sheet	https://www.infineon.com/dgdl/Infineon-IRPS5401M-DataSheet-v02_04-EN.pdf?fileId=5546d4625cc9456a015cd69d402139db
		Programming Guide	https://www.infineon.com/dgdl/Infineon-DC-DC_POL_IRPS5401_Programming_Guide-AdditionalTechnicalInformation-v01_08-EN.pdf?fileId=5546d46262b31d2e01632da26adb3419
		User guide	https://www.infineon.com/dgdl/Infineon-UG-IRSP5401Demoboard-UM-v01_02-EN.pdf?fileId=5546d4625e37f35a015e37f7da400002

3.2 Other References

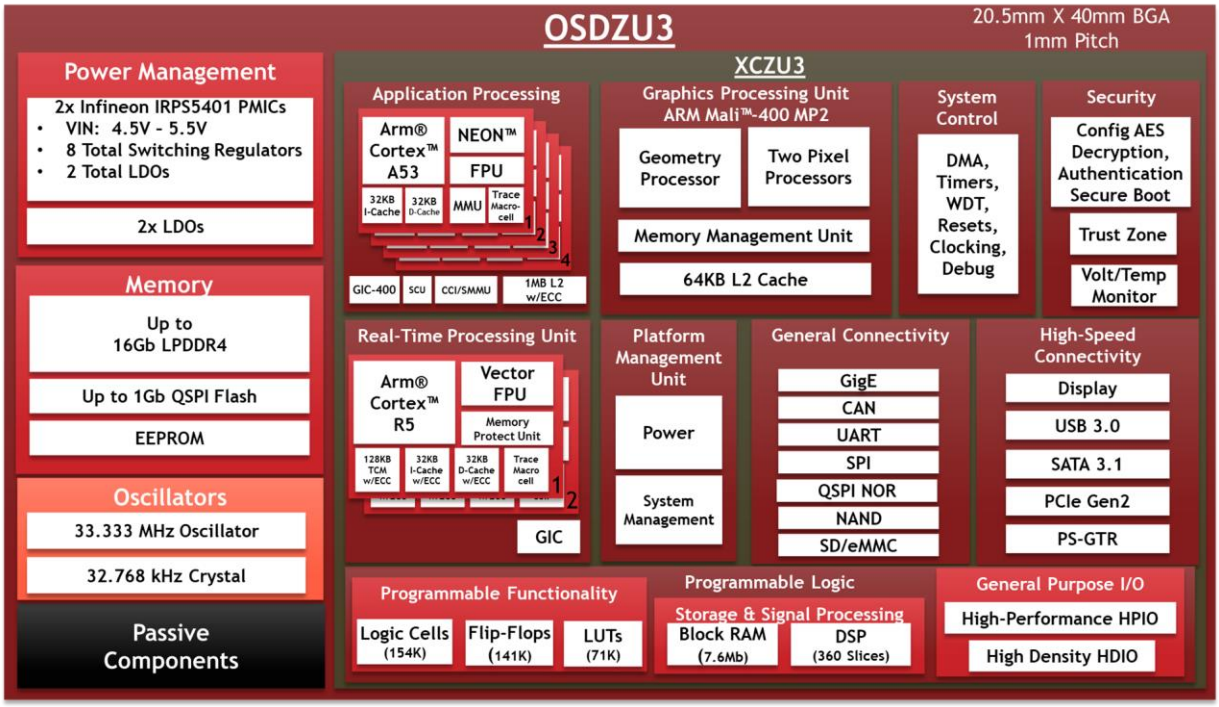
This section contains links to other reference documents helpful when using the OSDZU3 device. Some are referenced in this document.

- OSDZU3 Layout Guide: **https://octavosystems.com/app_notes/osdzu3-layout-guide**
- OSDZU3 Power application note: **https://octavosystems.com/app_notes/osdzu3-power-application-note**
- OSDZU3 Ball Mapping to ZU3: **https://octavosystems.com/app_notes/osdzu3-to-zu3-sfvc784-pin-mapping/**
- OSDZU3 Thermal Guide: **https://octavosystems.com/app_notes/osdzu3-thermal-management-application-note**
- OSDZU3 Schematic Check List: **https://octavosystems.com/app_notes/osdzu3-schematic-checklist/**
- OSDZU3 PMIC Programming Application Note: **https://octavosystems.com/app_notes/osdzu3-pmic-programming-guide/**
- OSDZU3 PMIC Configuration Files: **https://octavosystems.com/files/osdzu3-pmic-configuration-settings/**
- OSDZU3 Footprint and Symbol: **https://octavosystems.com/octavo_products/osdzu3/#Symbols**
- OSDZU3 Vivado Board Definition and Timing Delay Files: **https://octavosystems.com/octavo_products/osdzu3/#Design%20Tools**
- AMD XAPP427 - Implementation and Solder Reflow Guidelines for Pb-Free Packages: **https://www.xilinx.com/support/documentation/application_notes/xapp427.pdf**

4 Block Diagram

The OSDZU3 devices consist of 8 main components serving 5 distinct functions. The main processor is the ZU3 from AMD featuring a Quad-core Arm® Cortex®-A53 running up to 1.5GHz with Dual Arm® Cortex® R5 up to 600MHz and Programmable Logic (PL) Array with 154,350 System Logic Cells, 141,120 CLB flip-flops, 70,560 CLB LUTs and 360 DSP slices. The power system consists of two Infineon IRPS5401 Power Management ICs (PMIC) and two additional LDOs. The system memory includes up to 16Gb (2GB) of LPDDR4 and up to 1Gb (128MB) QSPI flash. An EEPROM provides nonvolatile memory for configuration. Finally, there is a 33.333 MHz Oscillator and a 32.768 kHz crystal to provide system clocks. Figure 4-1 shows a block diagram of the OSDZU3 and breaks out the key functions of the ZU3.

Figure 4-1 – OSDZU3 Detailed Block Diagram



4.1 Passives

Besides the 8 major components, the OSDZU3 also integrates capacitors, resistors, and inductors (Passives). Section 4.1.1 details the relevant integrated resistors, Section 4.1.2 details the required external resistors, and Section 4.1.3 details the recommended external capacitors you may need for proper operation of the OSDZU3 and for external use of the internal power rails listed in Table 7-2.

4.1.1 Integrated Resistors

Table 4-1 lists the relevant pull-up/down resistor locations and values integrated into the OSDZU3.

Table 4-1 - OSDZU3 Integrated resistors

From	To	Device	Description	Value
PS_JTAG_TMS	VCCO_PSIO_503	ZU3EG	PS_JTAG_TMS Pull up	10k
PS_JTAG_TDI	VCCO_PSIO_503	ZU3EG	PS_JTAG_TDI Pull up	10k
PS_JTAG_TCK	VCCO_PSIO_503	ZU3EG	PS_JTAG_TCK Pull up	10k
PS_INIT_B	VCCO_PSIO_503	ZU3EG	Pull up for open drain PS_INIT_B output	10k
PS_DONE	VCCO_PSIO_503	ZU3EG	Pull up for open drain PS_DONE output	10k
PS_POR_B	VCCO_PSIO_503	ZU3EG	PS_POR_B Pull up that brings device out of power on reset after PS_POR_B is released	10k
PS_PROG_B	VCCO_PSIO_503	ZU3EG	Pull up needed for PS_PROG_B input	10k
PS_SRST_B	VCCO_PSIO_503	ZU3EG	PS_SRST_B Pull up to bring ZU3 system out of reset	10k
PUDC_B	VCCAUX	ZU3EG	PUDC_B Pull up to disable preconfiguration IO pull-up resistors	10k
POR_OVERRIDE	GND	ZU3EG	POR_OVERRIDE Pull down to set standard PL power on delay time	10k
64_T0	GND	ZU3EG BANK 64	IO_T0U_N12_VRP Pull down	240
65_T0	GND	ZU3EG BANK 65	IO_T0U_N12_VRP Pull down	240
66_T0	GND	ZU3EG BANK 66	IO_T0U_N12_VRP Pull down	240
PWR_EN	+3V3_ON	PMIC	Pull up to enable PMIC1/PMIC2 output rails	10k
PGOOD	VCCO_PSIO_503	PMIC	Same as PS_POR_B Pull up for open drain PGOOD output of PMIC1/PMIC2	10k
PMIC_SCL	VDDIO	PMIC	I2C CLK Pull up	10k
PMIC_SDA	VDDIO	PMIC	I2C DATA Pull up	10k
PMIC_IRQB	VDDIO	PMIC	PMIC1/PMIC2 Alert# Pull up	10k
PMIC2_VOUTC_FB	PMIC2_C	PMIC2	Feedback resistor	240
PMIC2_VOUTC_FB	GND	PMIC2	Feedback resistor	240
ADDR_PROT	GND_ANA	PMIC	Internal resistor to set PMIC1 I2C address offset	2.32k
ADDR_PROT	GND_ANA	PMIC	Internal resistor to set PMIC2 I2C address offset	2.87k
MIO2	VCCO_PSIO_500	QSPI	QSPI /WP(IO2) Pull up	10k
MIO5	VCCO_PSIO_500	QSPI	QSPI /CS Pull up	10k
MIO3	VCCO_PSIO_500	QSPI	QSPI /HOLD(IO3) Pull up	10k
PMIC_SLEEP	+5V_IN	PMIC/LDO	Pull up to bring PMIC1/PMIC2 out of sleep mode and enable +3V3_ON	10k
EEPROM_WP	+3V3_ON	EEPROM	EEPROM Write Protect Pull up	10k
OSC_OE	VCC_PSAUX	Oscillator	33MHz Oscillator Enable Pull up	10k

4.1.2 External Resistors

Table 4-2 lists the resistors that are required to be placed external to the OSDZU3 for certain features to function properly.

Table 4-2 - OSDZU3 Required External resistors.

From	To	Device	Description	Value
PMIC1_MTP	GND	PMIC1	PMIC MTP resistor setting. Required for default operation.	2.32k
PMIC2_MTP	GND	PMIC2	PMIC MTP resistor setting. Required for default operation.	2.87k
PS_PADI	PS_PADO	RTC	Required to use the RTC (can be left off if RTC is not being used)	10M

4.1.3 Capacitors

The OSDZU3 includes many of the capacitors which AMD recommends (see AMD's recommendation in the "UltraScale Architectural PCB Design" user guide UG583 linked in the Reference Documents). External capacitors may need to be added to the OSDZU3 to ensure proper operation. This section will cover the list of capacitors integrated into the OSDZU3 and those recommended to be included externally.

4.1.3.1 Internal Capacitors

Table 4-3 lists relevant internal capacitors in the OSDZU3.

Table 4-3 - OSDZU3 internal bulk capacitors

Voltage Rail	Device	OSDZU3 Voltage Rail Pin Name	Total Internal Capacitance (µF) B, I Temp Grades (approx.)	Total Internal Capacitance[4] (µF) H Temp Grade (approx.)
VIN_*X*	PMIC1, PMIC2	+5V_IN	190	90
VCC_PSBATT	ZU3	VCC_PSBATT	5	5
PMIC1_VOUT_A[2]	PMIC1	VCCAUX	100	50
PMIC1_VOUT_B[2]	PMIC1	PMIC1_B	100	50
PMIC1_VOUT_C[2]	PMIC1	VCCO_PSDDR	160	80
PMIC1_VOUT_D[2]	PMIC1	VCCINT	100	50
PMIC1_VO_LDO[2]	PMIC1	+MGTRAVTT	1	1
LDO2	LDO2	+MGTRAVCC	5	5
PMIC2_VOUT_A[2]	PMIC2	VCC_PSAUX	120	70
PMIC2_VOUT_B[2]	PMIC2	VCC_PSINTLP	100	50
PMIC2_VOUT_C[2]	PMIC2	PMIC2_C	70	50
PMIC2_VOUT_D[2]	PMIC2	VCC_PSINTFP	100	50
PMIC2_VO_LDO[2]	PMIC2	VCC_PSPLL	0.1	0.1
LDO1	LDO1	+3V3_ON	5	5
External input[3]	ZU3	VCCO_HDIO_24[1]	5	5
		VCCO_HDIO_25[1]	5	5
		VCCO_HDIO_26[1]	5	5
		VCCO_HDIO_44[1]	5	5
External input[3]	ZU3	VCCO_HPIO_64[1]	5	5
		VCCO_HPIO_65[1]	5	5
		VCCO_HPIO_66[1]	5	5
External input[3]	ZU3	VCCO_PSIO_500[1]	5	5
		VCCO_PSIO_501[1]	5	5
		VCCO_PSIO_502[1]	5	5
		VCCO_PSIO_503[1]	5	5
External input[3]	ZU3	VCC_PSDDR_PLL	1	1
External input[3]	ZU3	VCCADC	1	1
External input[3]	ZU3	VCC_PSADC	1	1

1. Per AMD recommendations each bank should have (47µF + 10µF) Cap (Banks 24 – 26, 44 and 64 – 66) or (100µF + 10µF) Cap (Banks 500 – 503) from the voltage rail to VSS. But if multiple HDIOs, HPIOs or PSIOs are tied to the same input voltage rail they can share (47µF + 10µF) Capacitance to VSS up to four HDIOs and HPIOs, or (100µF + 10µF) Capacitance for up to all four PSIOs.
2. PMIC*X* is inserted in front of the PMIC signal name to differentiate between the 2 PMICs inside OSDZU3
3. These voltage rails are directly connected to the ball map. They will need to be connected to voltage rails on the PCB.
4. The capacitor values were modified to meet the temperature requirements. The PMIC switching frequency was updated as per Section 7.1.1 to ensure the OSDZU3 meets the specifications outlined in this datasheet.

4.1.3.2 External Capacitors

The system designer will need to add the necessary bulk capacitors to ensure proper operation of the OSDZU3.

Table 4-4 is a list of recommended bulk capacitors that you should include in your PCB design.

Note: The 47µF Capacitors for the banks in Table 4-4 may have up to 4 banks (e.g., HDIO, HPIO or PSIO) connected to the same capacitor given the selected banks are all powered by the same voltage source.

4.1.3.3 External Capacitor Placement

It is recommended that the external bulk capacitors be placed as near to the appropriate power balls of the OSDZU3 SiP as possible.

Note: The bulk capacitors may be placed on either side of the PCB.

If space is available, it is recommended that additional capacitor footprints be added to the PCB design which will accept a variety of capacitor values and sizes. Capacitors can be inserted when needed or the footprints left unpopulated (DNI).

Table 4-4 - OSDZU3 Recommended Capacitors

Integrated Source	Device	OSDZU3 Voltage Rail	Total Capacitance (µF)	Capacitor size (µF)							
				220	100	47	22	10	4.7	1	0.1
VIN_*X*	PMIC1/ PMIC2	+5V_IN	368.1	1	1	1				1	1
VCC_PSBATT	ZU3	VCC_PSBATT	4.7						1		
PMIC1_VOUT_A[2]	PMIC1	VCCAUX	10					1			
PMIC1_VOUT_B[2]	PMIC1	PMIC1_B	0[4]								
PMIC1_VOUT_C[2]	PMIC1	VCCO_PSDDR	0								
PMIC1_VOUT_D[2]	PMIC1	VCCINT	310.1		3			1			1
PMIC1_VO_LDO[2]	PMIC1	+MGTRAVTT	10					1			
LDO2	LDO2	+MGTRAVCC	4.8						1		1
PMIC2_VOUT_A[2]	PMIC2	VCC_PSAUX	100		1						
PMIC2_VOUT_B[2]	PMIC2	VCC_PSINTLP	10					1			
PMIC2_VOUT_C[2]	PMIC2	PMIC2_C	0[4]								
PMIC2_VOUT_D[2,5]	PMIC2	VCC_PSINTFP	147		1	1					
PMIC2_VO_LDO[2]	PMIC2	VCC_PSPLL	110		1			1			
LDO1	LDO1	+3V3_ON	0								
External input[3]	ZU3	VCCO_HDIO_24[1]	57			1		1			**
		VCCO_HDIO_25[1]	57			1		1			
		VCCO_HDIO_26[1]	57			1		1			
		VCCO_HDIO_44[1]	57			1		1			
External input[3]	ZU3	VCCO_HPIO_64[1]	57			1		1			**
		VCCO_HPIO_65[1]	57			1		1			
		VCCO_HPIO_66[1]	57			1		1			
External input[3]	ZU3	VCCO_PSIO_500[1]	110		1			1			**
		VCCO_PSIO_501[1]	110		1			1			
		VCCO_PSIO_502[1]	110		1			1			
		VCCO_PSIO_503[1]	110		1			1			
External input[3]	ZU3	VCC_PSDDR_PLL	10					1			
External input[3]	ZU3	VCCADC	4.8						1		1
External input[3]	ZU3	VCC_PSADC	4.8						1		1

1. AMD recommends each bank should have (47µF + 10µF) Cap (Banks 24 – 26, 44 and 64 – 66) or (100µF + 10µF) Cap (Banks 500 – 503) from the voltage rail to VSS. But if multiple HDIOs, HPIOs or PSIOs are tied to the same input voltage rail they may share one 47µF Capacitance to VSS up to all four HDIOs and all three HPIOs or one 100µF Capacitance for up to four PSIOs.
2. PMIC*X* is inserted in front of the PMIC signal name to differentiate between the 2 PMICs inside OSDZU3
3. These voltage rails are directly connected to the ball map. They will need to be connected to voltage rails on the PCB.
4. PMIC1_B and PMIC2_C have capacitance internal to the SiP. The external capacitance needed depends on the requirements for devices they are powering.
5. Recommended capacitance is for Maximum Current Output listed in Table 8-3

** AMD recommends many 0.1µF capacitors for return current paths and high frequency noise mitigation for the signal banks of the ZU3. Please ensure that your design has enough 0.1µF capacitors to not cause EMI / EMC issues. From a design perspective, it is better to have more capacitor locations and not populate them,

4.1.4 Additional Capacitors for External Power Requirements

The internal and external capacitors discussed in Sections 4.1.3.1 and 4.1.3.2 do not include the external use of OSDZU3 power supplied to external circuits. Refer to Table 7-2 for a list of internal power rails that may be used for external components. Also refer to Table 8-4 for current limits on external uses of power from OSDZU3 internal supplies. Table 4-5 lists the various internal power rails available for external use with recommended additional external capacitance to support the additional power requirements.

Table 4-5 - OSDZU3 Recommended Additional Capacitors for Power Rails if Used to Power External Components

From	To	Voltage	Device	Description	Minimum Value
PMIC1_B	GND	0.25 -2.55	PMIC1 B	PMIC1_B Capacitance	47µF
PMIC2_C	GND	2.55 - 5.1	PMIC2 C	PMIC2_C Capacitance	47µF
VCC_PSAUX	GND	1.8	PMIC2 A	VCC_PSAUX Capacitance	47µF
VCCAUX	GND	1.8	PMIC1 A	VCCAUX capacitance	47µF

5 Ball Map

The pins on the OSDZU3 belong to 4 distinct categories: 1) ZU3 signals, 2) PMIC signals, 3) control signals for internal components and 4) Power Domains. The signal names in the OSDZU3 Ball Map for the ZU3 and the PMICs devices have been named so they can be cross-referenced to the corresponding pin in the ZU3 and PMIC support documents.

Many of the ZU3 signals on the OSDZU3 Ball Map match the signal names of the ZU3 support documentation. Although some of the signal names have been shortened. For example, the HPIO & HDIO signals have short-hand names in the OSDZU3 Ball Map. The ZU3 names for those signals include characters which describe all the possible functions which could be multiplexed onto them in addition to their single-ended or differential I/O functionality. For the OSDZU3 Ball Map a shorthand name was used which includes only the bank number, the single or differential line number, and the polarity (for differential pairs). Table 5-1 lists several examples:

Table 5-1 - Short-hand names in the OSDZU3 Ball Map

XCZU3 Datasheet Name	OSDZU3 Ball Name	Comment
IO_L12N_AD0N_26	26N_L12	differential pair
IO_L12P_AD0P_26	26P_L12	
IO_L8N_HDGC_AD4N_44	44N_L8	differential pair
IO_L8P_HDGC_AD4P_44	44P_L8	
IO_T1U_N12_66	66_T1	single ended line
IO_T0U_N12_VRP_66	66_T0	single ended line

Refer to Table 5-7 through Table 5-21 for more detailed signal name mapping between OSDZU3 pin names and ZU3 pin names. In these tables, both the long hand names in the ZU3 list and the shorthand names in the OSDZU3 list are listed.

The arrangement of the signals has been optimized for easy escape from the BGA. Table 5-2 through Table 5-6 show the ball map for the OSDZU3. Each is shown in a top view looking through the package. See Layout Guide in the Reference Documents section for more details.

Table 5-2 - OSDZU3 Ball Map Top View

	1	2	3	4	5	6
A	VSS	GND_ANA	66P_L10	66P_L19	65_T3	65P_L19
B	VSS	66P_L9	66N_L10	66N_L19	65_T2	65N_L19
C	66P_L8	66N_L9	66_T1	66P_L11	65P_L21	65P_L24
D	66N_L8	66P_L12	PMIC2_MTP	66N_L11	65N_L21	65N_L24
E	66P_L7	66N_L12	RSVD	66P_L14	65P_L14	65P_L23
F	66N_L7	66P_L5	66_T0	66N_L14	65N_L14	65N_L23
G	66P_L2	66N_L5	65_T1	66P_L6	65P_L13	65P_L18
H	66N_L2	66P_L4	PWR_EN	66N_L6	65N_L13	65N_L18
J	66P_L1	66N_L4	PGOOD	65P_L10	64_T0	65P_L17
K	66N_L1	66P_L3	PMIC_IRQB	65N_L10	64_T3	65N_L17
L	65P_L8	66N_L3	PS_ERR_OUT	65P_L11	65P_L6	65P_L5
M	65N_L8	65P_L9	PS_ERR_STAT	65N_L11	65N_L6	65N_L5
N	65P_L7	65N_L9	VDDIO	65P_L22	65P_L4	65P_L3
P	65N_L7	65P_L12	65_T0	65N_L22	65N_L4	65N_L3
R	64P_L18	65N_L12	64_T2	65P_L15	65P_L2	65P_L1
T	64N_L18	64P_L17	PMIC_SLEEP	65N_L15	65N_L2	65N_L1
U	64P_L24	64N_L17	PMIC1_MTP	65P_L16	64P_L14	64P_L15
V	64N_L24	64P_L16	64_T1	65N_L16	64N_L14	64N_L15
W	VSS	64N_L16	64P_L23	64P_L22	64P_L21	64P_L20
Y	VSS	GND_ANA	64N_L23	64N_L22	64N_L21	64N_L20

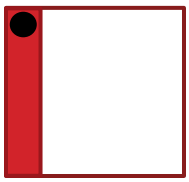


Table 5-3 – OSDZU3 Ball Map Top View

	7	8	9	10	11	12
A	66P_L21	66P_L13	66P_L23	66P_L18	RSVD	25P_L11
B	66N_L21	66N_L13	66N_L23	66N_L18	25P_L10	25P_L12
C	66_T3	66P_L15	66P_L24	66P_L17	25N_L10	25P_L5
D	66_T2	66N_L15	66N_L24	66N_L17	25P_L9	25P_L4
E	66P_L20	65P_L20	66P_L22	66P_L16	25N_L9	25P_L3
F	66N_L20	65N_L20	66N_L22	66N_L16	25P_L1	25N_L1
G	VSS	VSS	VSS	VSS	VSS	VSS
H	VSS	+5V_IN	+5V_IN	VSS	VSS	VSS
J	VSS	+5V_IN	+5V_IN	PMIC2_C	VSS	VSS
K	VSS	+5V_IN	+5V_IN	PMIC2_C	VSS	VSS
L	VSS	+5V_IN	+5V_IN	PMIC2_C	VCCINT	VSS
M	VSS	+5V_IN	+5V_IN	PMIC2_C	VCCINT	VSS
N	VSS	+5V_IN	+5V_IN	VSUPPLY	VSS	VSS
P	VSS	VSS	VSS	VSS	VSS	VSS
R	64P_L6	64P_L5	64P_L3	64P_L11	44P_L10	44N_L10
T	64N_L6	64N_L5	64N_L3	64N_L11	44P_L9	44N_L9
U	64P_L13	64P_L4	64P_L1	64P_L12	64P_L2	44P_L8
V	64N_L13	64N_L4	64N_L1	64N_L12	64N_L2	44P_L7
W	64P_L19	64P_L10	64P_L8	64P_L9	64P_L7	44P_L4
Y	64N_L19	64N_L10	64N_L8	64N_L9	64N_L7	44P_L1

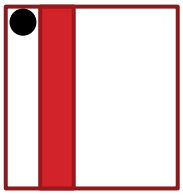


Table 5-4 – OSDZU3 Ball Map Top View

	13	14	15	16	17	18
A	25N_L11	26P_L3	26N_L3	26P_L1	26N_L1	VCC_PSBATT
B	25N_L12	26P_L2	26N_L2	26P_L4	26N_L4	VCC_PSDDR_PLL
C	25N_L5	25P_L8	25N_L8	26P_L5	26N_L5	26P_L7
D	25N_L4	25P_L6	25N_L6	26P_L6	26N_L6	26P_L8
E	25N_L3	25P_L7	25N_L7	26P_L9	26N_L9	26P_L11
F	25P_L2	25N_L2	26P_L10	26N_L10	26P_L12	26N_L12
G	VSS	PMIC1_B	VCCO_HPIO_65	VCCO_HPIO_66	VSS	VSS
H	VSS	VSS	VREF_65	VREF_66	VSS	VSS
J	VSS	VSS	VSS	VSS	VSS	VSS
K	VSS	VSS	VSS	VSS	VSS	VSS
L	VCC_PSINTLP	VSS	VSS	VSS	VCC_PSPLL	VSS
M	VCC_PSINTLP	VSS	VSS	RSVD	RSVD	VSS
N	VSS	VREF_64	VSS	VSS	VSS	RSVD
P	VSS	VCCO_HPIO_64	PMIC1_B	RSVD	RSVD	VCCO_HDIO_44
R	44P_L11	44N_L11	24P_L11	24N_L11	24P_L9	24N_L9
T	44P_L12	44N_L12	24P_L12	24N_L12	24P_L10	24N_L10
U	44N_L8	44P_L6	44N_L6	24P_L7	24N_L7	24P_L8
V	44N_L7	44P_L5	44N_L5	24P_L6	24N_L6	24P_L5
W	44N_L4	44P_L2	44N_L2	24P_L4	24N_L4	24P_L1
Y	44N_L1	44P_L3	44N_L3	24P_L3	24N_L3	24P_L2

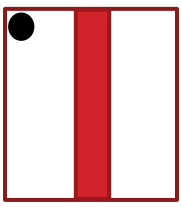


Table 5-5 – OSDZU3 Ball Map Top View

	19	20	21	22	23	24
A	DXN	VCCADC	VP	VN	GNDADC	MIO65
B	DXP	VCCADC	VCCADC	GNDADC	GNDADC	MIO67
C	26N_L7	VCCADC	VREFP	VREFN	GNDADC	MIO70
D	26N_L8	MIO57	VCCADC	GNDADC	MIO62	MIO68
E	26N_L11	MIO55	MIO59	MIO60	MIO69	MIO74
F	MIO56	MIO53	MIO54	MIO61	MIO63	MIO64
G	VSS	VCCO_HDIO_25	VCCO_HDIO_26	VCCAUX	PS_MODE0	PS_MODE1
H	VSS	VSS	VSS	PUDC_B	VCCO_PSIO_503	VCC_PSAUX
J	VCC_PSINTFP	VSS	VSS	POR_OVERRIDE	PS_MODE2	PS_MODE3
K	VCC_PSINTFP	VSS	VSS	VSS	VSS	VSS
L	RSVD	VSS	VCCO_PSDDR	VSS	VSS	VSS
M	VSS	VSS	RSVD	RSVD	VSS	VSS
N	RSVD	RSVD	VSS	VSS	VCC_PSAUX	+3V3_ON
P	VCCAUX	VCCO_HDIO_24	RSVD	RSVD	VCCO_PSIO_500	+3V3_ON
R	MIO30	MIO31	MIO35	MIO38	MIO39	MIO41
T	MIO29	MIO27	MIO32	MIO37	MIO36	MIO40
U	24N_L8	MIO28	MIO26	MIO33	MIO34	MIO42
V	24N_L5	MIO2	MIO6	MIO8	MIO9	MIO11
W	24N_L1	MIO0	MIO1	MIO7	MIO5	MIO15
Y	24N_L2	MIO3	MIO4	MIO13	MIO14	MIO16

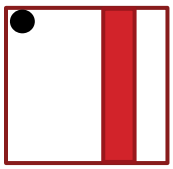
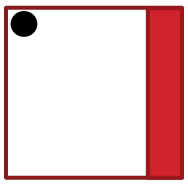


Table 5-6 – OSDZU3 Ball Map Top View

	25	26	27	28	29	30
A	MIO75	VSS	GTR_TX_P3	GTR_TX_N3	VSS	VSS
B	VSS	PS_REF_CLK	VSS	VSS	GTR_CLK_P3	GTR_CLK_N3
C	MIO71	VSS	GTR_RX_P3	GTR_RX_N3	VSS	VSS
D	VSS	PS_PADI	VSS	VSS	GTR_RX_P2	GTR_RX_N2
E	MIO76	VSS	GTR_CLK_P2	GTR_CLK_N2	VSS	VSS
F	OSC_OE	PS_PADO	VSS	VSS	GTR_TX_P2	GTR_TX_N2
G	VCCO_PSIO_502	VSS	GTR_TX_P1	GTR_TX_N1	VSS	VSS
H	VSS	PS_MGTRREF	VSS	VSS	GTR_CLK_P1	GTR_CLK_N1
J	VCCO_PSIO_501	VSS	GTR_RX_P1	GTR_RX_N1	VSS	VSS
K	VSS	+MGTRAVCC	VSS	VSS	GTR_RX_P0	GTR_RX_N0
L	MIO58	VSS	GTR_CLK_P0	GTR_CLK_N0	VSS	VSS
M	VSS	+MGTRAVTT	VSS	VSS	GTR_TX_P0	GTR_TX_N0
N	MIO77	VSS	EEPROM_WP	PS_DONE	VSS	VSS
P	MIO52	MIO72	PMIC_SCL	PS_PROG_B	PS_INIT_B	PS_POR_B
R	MIO66	MIO73	PMIC_SDA	PS_TMS	PS_TDI	PS_TDO
T	MIO44	MIO46	MIO45	MIO48	PS_SRST_B	PS_TCK
U	MIO43	MIO47	MIO51	MIO49	MIO50	MIO25
V	MIO23	MIO24	MIO20	MIO18	MIO22	MIO21
W	MIO12	MIO17	RSVD	VSS	VSS	VSS
Y	MIO10	MIO19	RSVD	VSS	VCC_PSADC	GND_PSADC



5.1 Ball Description

Table 5-7 through Table 5-21 list the unique signals and pin numbers of the OSDZU3. Where applicable they also provide the signal name and ball number of the equivalent signal of the ZU3 SFVC784 package. All the processor signals have the same function as the equivalent pin in the ZU3 except where noted.

The tables below are organized by Bank Number. Figure 5-1 shows the set of banks found in the ZU3 device. Further details can be found in the Zynq UltraScale+ MPSoC Overview (DS891) and Zynq UltraScale+ Packaging and Pinouts (UG1075) documents which can be found in Table 3-1.

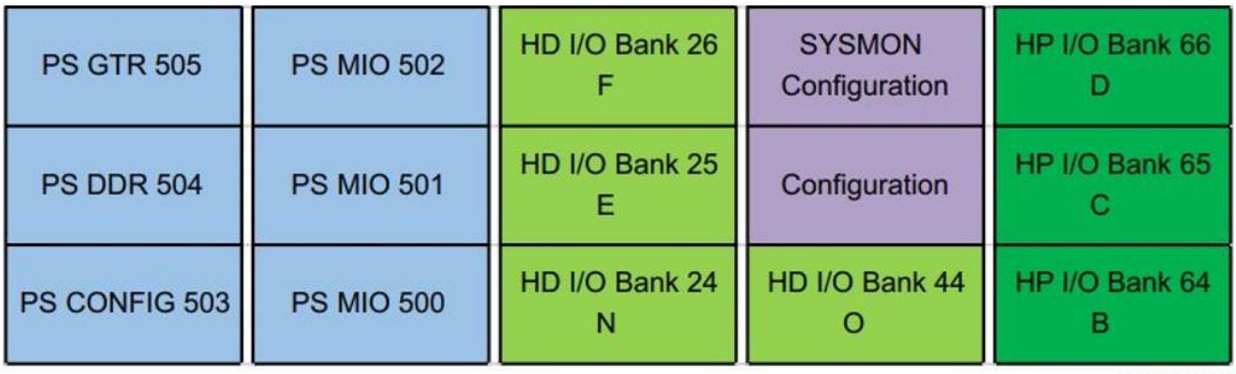


Figure 5-1 - The banks in the ZU3

Table 5-7 - ZU3 Ball Descriptions for Power and Grounds

OSDZU3		XCZU3		
Pin Name	**Pin Number**	**Pin Name**	**Pin Number**	**Comments**
+5V_IN	H8, J8, K8, L8, M8, N8, H9, J9, K9, L9, M9, N9		Not Connected to the ZU3	Power Input to OSDZU3 Device
VSUPPLY	N10		Not Connected to the ZU3	Power Input to OSDZU3 Device
VSS	A1, Y1, B1, W1, G7, H7, J7, K7, L7, M7, N7, P7, G8, P8, G9, P9, G10, H10, P10, G11, H11, J11, K11, N11, P11, G12, H12, J12, K12, L12, M12, N12, P12, G13, H13, J13, K13, N13, P13, H14, J14, K14, L14, M14, J15, K15, L15, M15, N15, J16, K16, L16, N16, G17, H17, J17, K17, N17, G18, H18, J18, K18, L18, M18, G19, H19, M19, H20, J20, K20, L20, M20, H21, J21, K21, N21, K22, L22, N22, K23, L23, M23, K24, L24, M24, B25, D25, H25, K25, M25, A26, C26, E26, G26, J26, L26, N26, B27, D27, F27, H27, K27, M27, B28, D28, F28, H28, K28, M28, W28, Y28, A29, C29, E29, G29, J29, L29, N29, W29, A30, C30, E30, G30, J30, L30, N30, W30	GND	A20, A24, A27, A28, AA1, AA19, AA2, AA24, AA3, AA4, AA5, AA6, AA9, AB12, AB27, AC15, AC20, AC25, AD18, AD3, AE1, AE11, AE21, AE26, AE6, AF14, AF19, AF4, AF9, AG2, AG22, AG27, AH5, B17, B2, B21, B25,B26, C10, C20, C24, C27, C28, C5, D13, D21, D26, D8, E16, E20, E24, E27, E28, F19, F21, F25, F26, F4, F9, G12, G2, G22, G23, G24, G27, G28, G7, H10, H15, H25, J13, J18, J23, J8, K11, K16, K21, K26, K6, L24, L9, M1, M2, M22, M27, M3, M4, M5, M7, N10, N12, N14, N20, N25, N5, P11, P3, P5, P8, R1, R15, R2, R21, R26, R5, T10, T14, T19, T3, T5, T9, U1, U11, U17, U2, U22, U27, U6, V13, V15, V3, V7, W1, W18, W2, W23, W6, Y11, Y16, Y3, Y7	
VCC_PSBATT	A18	VCC_PSBATT	Y18	Battery Input
VCC_PSADC	Y29	VCC_PSADC	Y20	PS SYSMON ADC supply voltage
GND_PSADC	Y30	GND_PSADC	W20	
VCCADC	A20, B20, C20, B21, D21	VCCADC	P12	PL System Monitor supply
GNDADC	B22, D22, A23, B23, C23	GNDADC	P13	
GND_ANA	A2, Y2		Not connected to ZU3	PMIC analog GND
VCCAUX	G22, P19	VCCAUX	M16, N16	Powered by PMIC1 VOUT_A
VCCAUX	G22, P19	VCCAUX_IO	M13, M14, M15	Powered by PMIC1 VOUT_A
VCCO_PSDDR	L21	VCCO_PSDDR	AB22, AD23, AF24, P23, T24, V25, Y26	Powered by PMIC1 VOUT_C
VCCINT	L11, M11	VCCINT	N11, N13, N15, P10, P14, P15, R10, R11, R14, T11, T15, U10, U14, U15, V10, V11, V12, V14	Powered by PMIC1 VOUT_D
VCCINT	L11, M11	VCCINT_IO	K10, L10, M10, M9	Powered by PMIC1 VOUT_D
VCCINT	L11, M11	VCCBRAM	L11, L12, M11, M12	Powered by PMIC1 VOUT_D
+MGTRAVTT	M26	PS_MGTRAVTT	A23, C23, D25, E23	Powered by PMIC1 VO_LDO
+MGTRAVCC	K26	PS_MGTRAVCC	B22, D22	Powered by LDO2
VCC_PSAUX	N23, H24	VCC_PSAUX	U19, U20, V19, W19	Powered by PMIC2 VOUT_A
VCC_PSINTLP	L13, M13	VCC_PSINTLP	V16, V17, V18, W15, W16, W17	Powered by PMIC2 VOUT_B
VCC_PSINTFP	J19, K19	VCC_PSINTFP	AA15, AA16, AA17, AA18, AB16, Y15, Y17	Powered by PMIC2 VOUT_D
VCC_PSINTFP	J19, K19	VCC_PSINTFP_DDR	AA20, AA21, Y19	Powered by PMIC2 VOUT_D
VCC_PSPLL	L17	VCC_PSPLL	T16, T17, T18	Powered by PMIC2 VO_LDO
VCC_PSDDR_PLL	B18	VCC_PSDDR_PLL	U16, U18	

OSDZU3		XCZU3		
Pin Name	**Pin Number**	**Pin Name**	**Pin Number**	**Comments**
PMIC1_B	G14, P15		Not connected to ZU3	External use. Powered by PMIC1 VOUT_B
PMIC2_C	J10, K10, L10, M10		Not connected to the ZU3	Powered by PMIC2 VOUT_C
+3V3_ON	N24, P24		Not connected to the ZU3	Powered by LDO1. Powers EEPROM.

Table 5-8 - ZU3 Ball Descriptions for Miscellaneous Signals

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
DXN	A19	DXN	U12	Temperature sensing diode pin
DXP	B19	DXP	U13	Temperature sensing diode pin
POR_OVERRIDE	J22	POR_OVERRIDE	W7	Power on reset delay override. Pulled low to GND to set standard PL power on delay time
PUDC_B	H22	PUDC_B	U7	Active low input to enable internal pull-ups during configuration on all SelectIO pins. Pin pulled to VCCAUX to disable Weak preconfiguration I/O pull-up resistors
VN	A22	VN	T12	System Monitor dedicated differential analog input. Should be tied to GNDADC if unused
VP	A21	VP	R13	System Monitor dedicated differential analog input. Should be tied to GNDADC if unused
VREFN	C22	VREFN	R12	Voltage reference GND
VREFP	C21	VREFP	T13	Voltage reference input
PMIC_SCL	P27		Not connected to ZU3	Connected to I2C of PMIC1/2 and EEPROM
PMIC_SDA	R27		Not connected to ZU3	Connected to I2C of PMIC1/2 and EEPROM
EEPROM_WP	N27		Not connected to ZU3	EEPROM write protect. Internally pulled up to +3V3_ON to enable Write Protect to EEPROM by default. Connect to GND to disable write protect.
OSC_OE	F25		Not connected to ZU3	33MHz Oscillator enable. Internally pulled up to VCC_PSAUX to enable 33MHz oscillator
VDDIO	N3		Not connected to ZU3	PMIC1/2 IO control voltage, MUST be connected to a 3.3V power source to set 3.3V I2C interface
PGOOD	J3		Not connected to ZU3	PMIC1 and PMIC2 Power Good output indicating proper operation of all power rails
PMIC_IRQB	K3		Not connected to ZU3	PMIC1/2 Alert# line. Pulled up to VDDIO through 10K resistor.
PMIC_SLEEP	T3		Not connected to ZU3	PMIC1/2 sleep mode control, +3V3_ON LDO enable pin, internally pulled up to +5V_IN
PMIC1_MTP	U3		Not connected to ZU3	Tie to GND through a 2.32Kohm Resistor for default operation
PMIC2_MTP	D3		Not connected to ZU3	Tie to GND through a 2.87Kohm Resistor for default operation
PWR_EN	H3		Not connected to Zu3	PMIC1/2 power rails enable pin. Internally pulled up to +3V3_ON
RSVD	A11, L19, M16, M17, M21, M22, N18, N19, N20. P16, P17, P21, P22, W27, Y27, E3		Not connected to ZU3	Reserved for future use. Do not connect
			N1, N2, N3, N4, P1, P2, P4, R3, R4, T1, T2, T4, U21, U3, U4, U5, V1, V2, V20, V21, V4, V5, V6, W21, W3, W4, W5, Y1, Y2, Y21, Y4, Y5, Y6	ZU3 Reserved pins not connected internally

Table 5-9 – ZU3 Ball Descriptions for Bank 24

OSDZU3		XCZU3		
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Comments**
24N_L10	T18	IO_L10N_AD10N_24	Y13	
24P_L10	T17	IO_L10P_AD10P_24	Y14	
24N_L11	R16	IO_L11N_AD9N_24	W11	
24P_L11	R15	IO_L11P_AD9P_24	W12	
24N_L12	T16	IO_L12N_AD8N_24	AA12	
24P_L12	T15	IO_L12P_AD8P_24	Y12	
24N_L1	W19	IO_L1N_AD15N_24	AE14	
24P_L1	W18	IO_L1P_AD15P_24	AE15	
24N_L2	Y19	IO_L2N_AD14N_24	AH14	
24P_L2	Y18	IO_L2P_AD14P_24	AG14	
24N_L3	Y17	IO_L3N_AD13N_24	AH13	
24P_L3	Y16	IO_L3P_AD13P_24	AG13	
24N_L4	W17	IO_L4N_AD12N_24	AF13	
24P_L4	W16	IO_L4P_AD12P_24	AE13	
24N_L5	V19	IO_L5N_HDGC_24	AD14	
24P_L5	V18	IO_L5P_HDGC_24	AD15	
24N_L6	V17	IO_L6N_HDGC_24	AC13	
24P_L6	V16	IO_L6P_HDGC_24	AC14	
24N_L7	U17	IO_L7N_HDGC_24	AB13	
24P_L7	U16	IO_L7P_HDGC_24	AA13	
24N_L8	U19	IO_L8N_HDGC_24	AB14	
24P_L8	U18	IO_L8P_HDGC_24	AB15	
24N_L9	R18	IO_L9N_AD11N_24	W13	
24P_L9	R17	IO_L9P_AD11P_24	W14	
VCCO_HDIO_24	P20	VCCO_24	AA14, AD13	**Need to be Connected externally. See Schematic checklist**

Table 5-10 – ZU3 Ball Descriptions for Bank 25

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
25N_L10	C11	IO_L10N_AD10N_25	A10	
25P_L10	B11	IO_L10P_AD10P_25	B11	
25N_L11	A13	IO_L11N_AD9N_25	A11	
25P_L11	A12	IO_L11P_AD9P_25	A12	
25N_L12	B13	IO_L12N_AD8N_25	C12	
25P_L12	B12	IO_L12P_AD8P_25	D12	
25N_L1	F12	IO_L1N_AD15N_25	J10	
25P_L1	F11	IO_L1P_AD15P_25	J11	
25N_L2	F14	IO_L2N_AD14N_25	K12	
25P_L2	F13	IO_L2P_AD14P_25	K13	
25N_L3	E13	IO_L3N_AD13N_25	G10	
25P_L3	E12	IO_L3P_AD13P_25	H11	
25N_L4	D13	IO_L4N_AD12N_25	H12	
25P_L4	D12	IO_L4P_AD12P_25	J12	
25N_L5	C13	IO_L5N_HDGC_25	F10	
25P_L5	C12	IO_L5P_HDGC_25	G11	
25N_L6	D15	IO_L6N_HDGC_25	F11	
25P_L6	D14	IO_L6P_HDGC_25	F12	
25N_L7	E15	IO_L7N_HDGC_25	D10	
25P_L7	E14	IO_L7P_HDGC_25	E10	
25N_L8	C15	IO_L8N_HDGC_25	D11	
25P_L8	C14	IO_L8P_HDGC_25	E12	
25N_L9	E11	IO_L9N_AD11N_25	B10	
25P_L9	D11	IO_L9P_AD11P_25	C11	
VCCO_HDIO_25	G20	VCCO_25	B12, E11	**Need to be Connected externally. See Schematic checklist.**

Table 5-11 – ZU3 Ball Descriptions for Bank 26

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
26N_L10	F16	IO_L10N_AD2N_26	H13	
26P_L10	F15	IO_L10P_AD2P_26	H14	
26N_L11	E19	IO_L11N_AD1N_26	J14	
26P_L11	E18	IO_L11P_AD1P_26	K14	
26N_L12	F18	IO_L12N_AD0N_26	L13	
26P_L12	F17	IO_L12P_AD0P_26	L14	
26N_L1	A17	IO_L1N_AD11N_26	A15	
26P_L1	A16	IO_L1P_AD11P_26	B15	
26N_L2	B15	IO_L2N_AD10N_26	A14	
26P_L2	B14	IO_L2P_AD10P_26	B14	
26N_L3	A15	IO_L3N_AD9N_26	A13	
26P_L3	A14	IO_L3P_AD9P_26	B13	
26N_L4	B17	IO_L4N_AD8N_26	C13	
26P_L4	B16	IO_L4P_AD8P_26	C14	
26N_L5	C17	IO_L5N_HDGC_AD7N_26	D14	
26P_L5	C16	IO_L5P_HDGC_AD7P_26	D15	
26N_L6	D17	IO_L6N_HDGC_AD6N_26	E13	
26P_L6	D16	IO_L6P_HDGC_AD6P_26	E14	
26N_L7	C19	IO_L7N_HDGC_AD5N_26	F13	
26P_L7	C18	IO_L7P_HDGC_AD5P_26	G13	
26N_L8	D19	IO_L8N_HDGC_AD4N_26	E15	
26P_L8	D18	IO_L8P_HDGC_AD4P_26	F15	
26N_L9	E17	IO_L9N_AD3N_26	G14	
26P_L9	E16	IO_L9P_AD3P_26	G15	
VCCO_HDIO_26	G21	VCCO_26	C15, F14	**Need to be Connected externally. See Schematic checklist.**

Table 5-12 – ZU3 Ball Descriptions for Bank 44

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
44N_L10	R12	IO_L10N_AD2N_44	Y10	
44P_L10	R11	IO_L10P_AD2P_44	W10	
44N_L11	R14	IO_L11N_AD1N_44	AA8	
44P_L11	R13	IO_L11P_AD1P_44	Y9	
44N_L12	T14	IO_L12N_AD0N_44	AB9	
44P_L12	T13	IO_L12P_AD0P_44	AB10	
44N_L1	Y13	IO_L1N_AD11N_44	AH10	
44P_L1	Y12	IO_L1P_AD11P_44	AG10	
44N_L2	W15	IO_L2N_AD10N_44	AG11	
44P_L2	W14	IO_L2P_AD10P_44	AF11	
44N_L3	Y15	IO_L3N_AD9N_44	AH11	
44P_L3	Y14	IO_L3P_AD9P_44	AH12	
44N_L4	W13	IO_L4N_AD8N_44	AF10	
44P_L4	W12	IO_L4P_AD8P_44	AE10	
44N_L5	V15	IO_L5N_HDGC_AD7N_44	AF12	
44P_L5	V14	IO_L5P_HDGC_AD7P_44	AE12	
44N_L6	U15	IO_L6N_HDGC_AD6N_44	AD12	
44P_L6	U14	IO_L6P_HDGC_AD6P_44	AC12	
44N_L7	V13	IO_L7N_HDGC_AD5N_44	AD10	
44P_L7	V12	IO_L7P_HDGC_AD5P_44	AD11	
44N_L8	U13	IO_L8N_HDGC_AD4N_44	AC11	
44P_L8	U12	IO_L8P_HDGC_AD4P_44	AB11	
44N_L9	T12	IO_L9N_AD3N_44	AA10	
44P_L9	T11	IO_L9P_AD3P_44	AA11	
VCCO_HDIO_44	P18	VCCO_44	AC10, AG12	**Need to be Connected externally. See Schematic checklist.**

Table 5-13 – ZU3 Ball Descriptions for Bank 64

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
64N_L10	Y8	IO_L10N_T1U_N7_QBC_AD4N_64	AG5	
64P_L10	W8	IO_L10P_T1U_N6_QBC_AD4P_64	AG6	
64N_L11	T10	IO_L11N_T1U_N9_GC_64	AF6	
64P_L11	R10	IO_L11P_T1U_N8_GC_64	AF7	
64N_L12	V10	IO_L12N_T1U_N11_GC_64	AF5	
64P_L12	U10	IO_L12P_T1U_N10_GC_64	AE5	
64N_L13	V7	IO_L13N_T2L_N1_GC_QBC_64	AD4	
64P_L13	U7	IO_L13P_T2L_N0_GC_QBC_64	AD5	
64N_L14	V5	IO_L14N_T2L_N3_GC_64	AC3	
64P_L14	U5	IO_L14P_T2L_N2_GC_64	AC4	
64N_L15	V6	IO_L15N_T2L_N5_AD11N_64	AB3	
64P_L15	U6	IO_L15P_T2L_N4_AD11P_64	AB4	
64N_L16	W2	IO_L16N_T2U_N7_QBC_AD3N_64	AD1	
64P_L16	V2	IO_L16P_T2U_N6_QBC_AD3P_64	AD2	
64N_L17	U2	IO_L17N_T2U_N9_AD10N_64	AC2	
64P_L17	T2	IO_L17P_T2U_N8_AD10P_64	AB2	
64N_L18	T1	IO_L18N_T2U_N11_AD2N_64	AC1	
64P_L18	R1	IO_L18P_T2U_N10_AD2P_64	AB1	
64N_L19	Y7	IO_L19N_T3L_N1_DBC_AD9N_64	AH4	
64P_L19	W7	IO_L19P_T3L_N0_DBC_AD9P_64	AG4	
64N_L1	V9	IO_L1N_T0L_N1_DBC_64	AD9	
64P_L1	U9	IO_L1P_T0L_N0_DBC_64	AC9	
64N_L20	Y6	IO_L20N_T3L_N3_AD1N_64	AH3	
64P_L20	W6	IO_L20P_T3L_N2_AD1P_64	AG3	
64N_L21	Y5	IO_L21N_T3L_N5_AD8N_64	AF3	
64P_L21	W5	IO_L21P_T3L_N4_AD8P_64	AE3	
64N_L22	Y4	IO_L22N_T3U_N7_DBC_AD0N_64	AF2	
64P_L22	W4	IO_L22P_T3U_N6_DBC_AD0P_64	AE2	
64N_L23	Y3	IO_L23N_T3U_N9_64	AH1	
64P_L23	W3	IO_L23P_T3U_N8_64	AH2	
64N_L24	V1	IO_L24N_T3U_N11_64	AG1	
64P_L24	U1	IO_L24P_T3U_N10_64	AF1	
64N_L2	V11	IO_L2N_T0L_N3_64	AE8	
64P_L2	U11	IO_L2P_T0L_N2_64	AE9	
64N_L3	T9	IO_L3N_T0L_N5_AD15N_64	AC8	
64P_L3	R9	IO_L3P_T0L_N4_AD15P_64	AB8	
64N_L4	V8	IO_L4N_T0U_N7_DBC_AD7N_64	AE7	
64P_L4	U8	IO_L4P_T0U_N6_DBC_AD7P_64	AD7	
64N_L5	T8	IO_L5N_T0U_N9_AD14N_64	AC7	
64P_L5	R8	IO_L5P_T0U_N8_AD14P_64	AB7	
64N_L6	T7	IO_L6N_T0U_N11_AD6N_64	AC6	
64P_L6	R7	IO_L6P_T0U_N10_AD6P_64	AB6	
64N_L7	Y11	IO_L7N_T1L_N1_QBC_AD13N_64	AH9	
64P_L7	W11	IO_L7P_T1L_N0_QBC_AD13P_64	AG9	
64N_L8	Y9	IO_L8N_T1L_N3_AD5N_64	AG8	
64P_L8	W9	IO_L8P_T1L_N2_AD5P_64	AF8	
64N_L9	Y10	IO_L9N_T1L_N5_AD12N_64	AH7	
64P_L9	W10	IO_L9P_T1L_N4_AD12P_64	AH8	
64_T0	J5	IO_T0U_N12_VRP_64	AD6	
64_T1	V3	IO_T1U_N12_64	AH6	
64_T2	R3	IO_T2U_N12_64	AB5	
64_T3	K5	IO_T3U_N12_64	AE4	
VCCO_HP IO_64	P14	VCCO_64	AC5, AD8, AG7	**Need to be Connected externally. See Schematic checklist.**
VREF_64	N14	VREF_64	AA7	

Table 5-14 – ZU3 Ball Descriptions for Bank 65

OSDZU3		XCZU3		Comments
Pin Name	Pin No.	Pin Name	Pin No.	
65N_L10	K4	IO_L10N_T1U_N7_QBC_AD4N_65	H3	
65P_L10	J4	IO_L10P_T1U_N6_QBC_AD4P_65	H4	
65N_L11	M4	IO_L11N_T1U_N9_GC_65	K3	
65P_L11	L4	IO_L11P_T1U_N8_GC_65	K4	
65N_L12	R2	IO_L12N_T1U_N11_GC_65	L2	
65P_L12	P2	IO_L12P_T1U_N10_GC_65	L3	
65N_L13	H5	IO_L13N_T2L_N1_GC_QBC_65	L6	
65P_L13	G5	IO_L13P_T2L_N0_GC_QBC_65	L7	
65N_L14	F5	IO_L14N_T2L_N3_GC_65	L5	
65P_L14	E5	IO_L14P_T2L_N2_GC_65	M6	
65N_L15	T4	IO_L15N_T2L_N5_AD11N_65	N6	
65P_L15	R4	IO_L15P_T2L_N4_AD11P_65	N7	
65N_L16	V4	IO_L16N_T2U_N7_QBC_AD3N_65	P6	
65P_L16	U4	IO_L16P_T2U_N6_QBC_AD3P_65	P7	
65N_L17	K6	IO_L17N_T2U_N9_AD10N_65	N8	
65P_L17	J6	IO_L17P_T2U_N8_AD10P_65	N9	
65N_L18	H6	IO_L18N_T2U_N11_AD2N_65	L8	
65P_L18	G6	IO_L18P_T2U_N10_AD2P_65	M8	
65N_L19	B6	IO_L19N_T3L_N1_DBC_AD9N_65	J4	
65P_L19	A6	IO_L19P_T3L_N0_DBC_AD9P_65	J5	
65N_L1	T6	IO_L1N_T0L_N1_DBC_65	Y8	
65P_L1	R6	IO_L1P_T0L_N0_DBC_65	W8	
65N_L20	F8	IO_L20N_T3L_N3_AD1N_65	H6	
65P_L20	E8	IO_L20P_T3L_N2_AD1P_65	J6	
65N_L21	D5	IO_L21N_T3L_N5_AD8N_65	H7	
65P_L21	C5	IO_L21P_T3L_N4_AD8P_65	J7	
65N_L22	P4	IO_L22N_T3U_N7_DBC_AD0N_65	K7	
65P_L22	N4	IO_L22P_T3U_N6_DBC_AD0P_65	K8	
65N_L23	F6	IO_L23N_T3U_N9_65	J9	
65P_L23	E6	IO_L23P_T3U_N8_I2C_SCLK_65	K9	
65N_L24	D6	IO_L24N_T3U_N11_PERSTN0_65	H8	
65P_L24	C6	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	H9	
65N_L2	T5	IO_L2N_T0L_N3_65	V9	
65P_L2	R5	IO_L2P_T0L_N2_65	U9	
65N_L3	P6	IO_L3N_T0L_N5_AD15N_65	V8	
65P_L3	N6	IO_L3P_T0L_N4_AD15P_65	U8	
65N_L4	P5	IO_L4N_T0U_N7_DBC_AD7N_65	T8	
65P_L4	N5	IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	R8	
65N_L5	M6	IO_L5N_T0U_N9_AD14N_65	T7	
65P_L5	L6	IO_L5P_T0U_N8_AD14P_65	R7	
65N_L6	M5	IO_L6N_T0U_N11_AD6N_65	T6	
65P_L6	L5	IO_L6P_T0U_N10_AD6P_65	R6	
65N_L7	P1	IO_L7N_T1L_N1_QBC_AD13N_65	K1	
65P_L7	N1	IO_L7P_T1L_N0_QBC_AD13P_65	L1	
65N_L8	M1	IO_L8N_T1L_N3_AD5N_65	H1	
65P_L8	L1	IO_L8P_T1L_N2_AD5P_65	J1	
65N_L9	N2	IO_L9N_T1L_N5_AD12N_65	J2	
65P_L9	M2	IO_L9P_T1L_N4_AD12P_65	K2	
65_T0	P3	IO_T0U_N12_VRP_65	W9	
65_T1	G3	IO_T1U_N12_65	H2	
65_T2	B5	IO_T2U_N12_65	P9	
65_T3	A5	IO_T3U_N12_65	K5	
VCCO_HPIO_65	G15	VCCO_65	H5, J3, L4	**Need to be Connected externally. See Schematic checklist.**
VREF_65	H15	VREF_65	R9	

Table 5-15 – ZU3 Ball Descriptions for Bank 66

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
66N_L10	B3	IO_L10N_T1U_N7_QBC_AD4N_66	A4	
66P_L10	A3	IO_L10P_T1U_N6_QBC_AD4P_66	B4	
66N_L11	D4	IO_L11N_T1U_N9_GC_66	C4	
66P_L11	C4	IO_L11P_T1U_N8_GC_66	D4	
66N_L12	E2	IO_L12N_T1U_N11_GC_66	C2	
66P_L12	D2	IO_L12P_T1U_N10_GC_66	C3	
66N_L13	B8	IO_L13N_T2L_N1_GC_QBC_66	D6	
66P_L13	A8	IO_L13P_T2L_N0_GC_QBC_66	D7	
66N_L14	F4	IO_L14N_T2L_N3_GC_66	D5	
66P_L14	E4	IO_L14P_T2L_N2_GC_66	E5	
66N_L15	D8	IO_L15N_T2L_N5_AD11N_66	F6	
66P_L15	C8	IO_L15P_T2L_N4_AD11P_66	G6	
66N_L16	F10	IO_L16N_T2U_N7_QBC_AD3N_66	F7	
66P_L16	E10	IO_L16P_T2U_N6_QBC_AD3P_66	G8	
66N_L17	D10	IO_L17N_T2U_N9_AD10N_66	E8	
66P_L17	C10	IO_L17P_T2U_N8_AD10P_66	F8	
66N_L18	B10	IO_L18N_T2U_N11_AD2N_66	D9	
66P_L18	A10	IO_L18P_T2U_N10_AD2P_66	E9	
66N_L19	B4	IO_L19N_T3L_N1_DBC_AD9N_66	A5	
66P_L19	A4	IO_L19P_T3L_N0_DBC_AD9P_66	B5	
66N_L1	K1	IO_L1N_T0L_N1_DBC_66	F1	
66P_L1	J1	IO_L1P_T0L_N0_DBC_66	G1	
66N_L20	F7	IO_L20N_T3L_N3_AD1N_66	B6	
66P_L20	E7	IO_L20P_T3L_N2_AD1P_66	C6	
66N_L21	B7	IO_L21N_T3L_N5_AD8N_66	A6	
66P_L21	A7	IO_L21P_T3L_N4_AD8P_66	A7	
66N_L22	F9	IO_L22N_T3U_N7_DBC_AD0N_66	B8	
66P_L22	E9	IO_L22P_T3U_N6_DBC_AD0P_66	C8	
66N_L23	B9	IO_L23N_T3U_N9_66	A8	
66P_L23	A9	IO_L23P_T3U_N8_66	A9	
66N_L24	D9	IO_L24N_T3U_N11_66	B9	
66P_L24	C9	IO_L24P_T3U_N10_66	C9	
66N_L2	H1	IO_L2N_T0L_N3_66	D1	
66P_L2	G1	IO_L2P_T0L_N2_66	E1	
66N_L3	L2	IO_L3N_T0L_N5_AD15N_66	E2	
66P_L3	K2	IO_L3P_T0L_N4_AD15P_66	F2	
66N_L4	J2	IO_L4N_T0U_N7_DBC_AD7N_66	F3	
66P_L4	H2	IO_L4P_T0U_N6_DBC_AD7P_66	G3	
66N_L5	G2	IO_L5N_T0U_N9_AD14N_66	E3	
66P_L5	F2	IO_L5P_T0U_N8_AD14P_66	E4	
66N_L6	H4	IO_L6N_T0U_N11_AD6N_66	F5	
66P_L6	G4	IO_L6P_T0U_N10_AD6P_66	G5	
66N_L7	F1	IO_L7N_T1L_N1_QBC_AD13N_66	B1	
66P_L7	E1	IO_L7P_T1L_N0_QBC_AD13P_66	C1	
66N_L8	D1	IO_L8N_T1L_N3_AD5N_66	A1	
66P_L8	C1	IO_L8P_T1L_N2_AD5P_66	A2	
66N_L9	C2	IO_L9N_T1L_N5_AD12N_66	A3	
66P_L9	B2	IO_L9P_T1L_N4_AD12P_66	B3	
66_T0	F3	IO_T0U_N12_VRP_66	G4	
66_T1	C3	IO_T1U_N12_66	D2	
66_T2	D7	IO_T2U_N12_66	E7	
66_T3	C7	IO_T3U_N12_66	C7	
VCCO_HPIO_66	G16	VCCO_66	B7, D3, E6	**Need to be Connected externally. See Schematic checklist.**
VREF_66	H16	VREF_66	G9	

Table 5-16 – ZU3 Ball Descriptions for Bank 500

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
MIO0	W20	PS_MIO0	AG15	
MIO1	W21	PS_MIO1	AG16	
MIO10	Y25	PS_MIO10	AD17	
MIO11	V24	PS_MIO11	AE17	
MIO12	W25	PS_MIO12	AC17	
MIO13	Y22	PS_MIO13	AH18	
MIO14	Y23	PS_MIO14	AG18	
MIO15	W24	PS_MIO15	AE18	
MIO16	Y24	PS_MIO16	AF18	
MIO17	W26	PS_MIO17	AC18	
MIO18	V28	PS_MIO18	AC19	
MIO19	Y26	PS_MIO19	AE19	
MIO2	V20	PS_MIO2	AF15	
MIO20	V27	PS_MIO20	AD19	
MIO21	V30	PS_MIO21	AC21	
MIO22	V29	PS_MIO22	AB20	
MIO23	V25	PS_MIO23	AB18	
MIO24	V26	PS_MIO24	AB19	
MIO25	U30	PS_MIO25	AB21	
MIO3	Y20	PS_MIO3	AH15	
MIO4	Y21	PS_MIO4	AH16	
MIO5	W23	PS_MIO5	AD16	
MIO6	V21	PS_MIO6	AF16	
MIO7	W22	PS_MIO7	AH17	
MIO8	V22	PS_MIO8	AF17	
MIO9	V23	PS_MIO9	AC16	
VCCO_PSIO_500	P23	VCCO_PSIO0_500	AB17, AE16, AG17	**Needs to be connected externally. Should be connected to either 1.8V or 3.3V depending on the version of the device. See Schematic checklist**

Table 5-17 – ZU3 Ball Descriptions for Bank 501

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
MIO26	U21	PS_MIO26	L15	
MIO27	T20	PS_MIO27	J15	
MIO28	U20	PS_MIO28	K15	
MIO29	T19	PS_MIO29	G16	
MIO30	R19	PS_MIO30	F16	
MIO31	R20	PS_MIO31	H16	
MIO32	T21	PS_MIO32	J16	
MIO33	U22	PS_MIO33	L16	
MIO34	U23	PS_MIO34	L17	
MIO35	R21	PS_MIO35	H17	
MIO36	T23	PS_MIO36	K17	
MIO37	T22	PS_MIO37	J17	
MIO38	R22	PS_MIO38	H18	
MIO39	R23	PS_MIO39	H19	
MIO40	T24	PS_MIO40	K18	
MIO41	R24	PS_MIO41	J19	
MIO42	U24	PS_MIO42	L18	
MIO43	U25	PS_MIO43	K19	
MIO44	T25	PS_MIO44	J20	
MIO45	T27	PS_MIO45	K20	
MIO46	T26	PS_MIO46	L20	
MIO47	U26	PS_MIO47	H21	
MIO48	T28	PS_MIO48	J21	
MIO49	U28	PS_MIO49	M18	
MIO50	U29	PS_MIO50	M19	
MIO51	U27	PS_MIO51	L21	
VCCO_PSIO_501	J25	VCCO_PSIO1_501	H20, L19	**Need to be Connected externally. See Schematic checklist.**

Table 5-18 – ZU3 Ball Descriptions for Bank 502

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
MIO52	P25	PS_MIO52	G18	
MIO53	F20	PS_MIO53	D16	
MIO54	F21	PS_MIO54	F17	
MIO55	E20	PS_MIO55	B16	
MIO56	F19	PS_MIO56	C16	
MIO57	D20	PS_MIO57	A16	
MIO58	L25	PS_MIO58	F18	
MIO59	E21	PS_MIO59	E17	
MIO60	E22	PS_MIO60	C17	
MIO61	F22	PS_MIO61	D17	
MIO62	D23	PS_MIO62	A17	
MIO63	F23	PS_MIO63	E18	
MIO64	F24	PS_MIO64	E19	
MIO65	A24	PS_MIO65	A18	
MIO66	R25	PS_MIO66	G19	
MIO67	B24	PS_MIO67	B18	
MIO68	D24	PS_MIO68	C18	
MIO69	E23	PS_MIO69	D19	
MIO70	C24	PS_MIO70	C19	
MIO71	C25	PS_MIO71	B19	
MIO72	P26	PS_MIO72	G20	
MIO73	R26	PS_MIO73	G21	
MIO74	E24	PS_MIO74	D20	
MIO75	A25	PS_MIO75	A19	
MIO76	E25	PS_MIO76	B20	
MIO77	N25	PS_MIO77	F20	
VCCO_PSIO_502	G25	VCCO_PSIO2_502	D18, G17	**Need to be Connected externally. See Schematic checklist.**

Table 5-19 – ZU3 Ball Descriptions for Bank 503

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
PS_DONE	N28	PS_DONE	M21	Indicates the PS configuration is completed
PS_ERR_OUT	L3	PS_ERROR_OUT	P17	Asserted for accidental loss of power, a hardware error, or an exception in the PMU
PS_ERR_STAT	M3	PS_ERROR_STATUS	M20	Indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status
PS_INIT_B	P29	PS_INIT_B	P21	Indicates the PL is initialized after a power-on reset (POR). This signal should not be held Low externally to delay the PL configuration sequence because the signal level is not visible to software. However, if there is a CRC error detected when the PL bit stream is loaded PS_INIT_B will be driven low
PS_TCK	T30	PS_JTAG_TCK	R19	JTAG
PS_TDI	R29	PS_JTAG_TDI	R18	
PS_TDO	R30	PS_JTAG_TDO	T21	
PS_TMS	R28	PS_JTAG_TMS	N21	
PS_MODE0	G23	PS_MODE0	P19	4-bit boot mode pins sampled on POR de-assertion
PS_MODE1	G24	PS_MODE1	P20	
PS_MODE2	J23	PS_MODE2	R20	
PS_MODE3	J24	PS_MODE3	T20	
PS_PADI	D26	PS_PADI	N17	Crystal pad input (RTC) 10 Mohm resistor required to be placed between PS_PADI and PS_PADO to use the RTC.
PS_PADO	F26	PS_PADO	N18	Crystal pad output (RTC) 10 Mohm resistor required to be placed between PS_PADI and PS_PADO to use the RTC.
PS_POR_B	P30	PS_POR_B	P16	Power-on reset signal (connected internally to PGOOD)
PS_PROG_B	P28	PS_PROG_B	R17	PS configuration reset signal
PS_REF_CLK	B26	PS_REF_CLK	R16	System reference clock connected to the output of internal 33MHz oscillator
PS_SRST_B	T29	PS_SRST_B	N19	System reset commonly used during debug
VCCO_PSIO_503	H23	VCCO_PSIO3_503	M17, P18	**Needs to be connected externally. See Schematic checklist.**

Table 5-20 – ZU3 Ball Descriptions for Bank 504

OSDZU3		XCZU3		Comments
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	
VCCO_PSDDR	L21	VCCO_PSDDR_504	AB22, AD23, AF24, P23, T24, V25, Y26	Only used as a test point

Table 5-21 – ZU3 Ball Descriptions for Bank 505

OSDZU3		XCZU3		
Pin Name	**Pin No.**	**Pin Name**	**Pin No.**	**Comments**
GTR_CLK_N0	L28	PS_MGTREFCLK0N_505	F24	GTR Lane 0
GTR_CLK_P0	L27	PS_MGTREFCLK0P_505	F23	
GTR_RX_N0	K30	PS_MGTRRXN0_505	F28	
GTR_RX_P0	K29	PS_MGTRRXP0_505	F27	
GTR_TX_N0	M30	PS_MGTRTXN0_505	E26	
GTR_TX_P0	M29	PS_MGTRTXP0_505	E25	
GTR_CLK_N1	H30	PS_MGTREFCLK1N_505	E22	GTR Lane 1
GTR_CLK_P1	H29	PS_MGTREFCLK1P_505	E21	
GTR_RX_N1	J28	PS_MGTRRXN1_505	D28	
GTR_RX_P1	J27	PS_MGTRRXP1_505	D27	
GTR_TX_N1	G28	PS_MGTRTXN1_505	D24	
GTR_TX_P1	G27	PS_MGTRTXP1_505	D23	
GTR_CLK_N2	E28	PS_MGTREFCLK2N_505	C22	GTR Lane 2
GTR_CLK_P2	E27	PS_MGTREFCLK2P_505	C21	
GTR_RX_N2	D30	PS_MGTRRXN2_505	B28	
GTR_RX_P2	D29	PS_MGTRRXP2_505	B27	
GTR_TX_N2	F30	PS_MGTRTXN2_505	C26	
GTR_TX_P2	F29	PS_MGTRTXP2_505	C25	
GTR_CLK_N3	B30	PS_MGTREFCLK3N_505	A22	GTR Lane 3
GTR_CLK_P3	B29	PS_MGTREFCLK3P_505	A21	
GTR_RX_N3	C28	PS_MGTRRXN3_505	A26	
GTR_RX_P3	C27	PS_MGTRRXP3_505	A25	
GTR_TX_N3	A28	PS_MGTRTXN3_505	B24	
GTR_TX_P3	A27	PS_MGTRTXP3_505	B23	
+MGTRAVCC	K26	PS_MGTRAVCC	B22, D22	Test point for internal power supply for GTRs
+MGTRAVTT	M26	PS_MGTRAVTT	A23, C23, D25, E23	Test point for internal Power supply for GTRs
PS_MGTRREF	H26	PS_MGTRREF_505	F22	Calibration resistor pin for the termination resistor calibration circuit for the PS-GTR transceivers. Needs to be connected externally. See Schematic Checklist

5.2 Reserved and No Connect Balls

The OSDZU3 ball map contains balls which are marked either RSVD or NC. These balls must remain unconnected on the system PCB since they may be used for other purposes in future versions of the OSDZU3.

5.3 Test Point Signals

There are several groups of signals and power that you need to consider bringing to a test point or header. Refer to the OSDZU3 schematic checklist in the Reference Documents for the list of signals that you should consider bringing out to test points or headers.

6 OSDZU3 Components

The OSDZU3 integrates the AMD XCZU3 Multi-Processor System on Chip (MPSoC). Figure 6-1 shows a block diagram for the OSDZU3. Refer to Figure 4-1 and the references listed in Section 3 for more details. Along with the XCZU3 are two (2) Infineon PMICs, two LDOs, LPDDR4 Memory, an EEPROM for hardware configuration information, a QSPI Flash memory, a 33.333 MHz Oscillator for the primary clock input, 32.768 kHz Crystal for the real time clock, and the associated resistors, capacitors, and inductors carefully placed into a single design-in-ready package. The following subsections contain specific device information needed for the integrated components to design your system with the OSDZU3. Specifics on the Power Management System will be covered in Section 7.

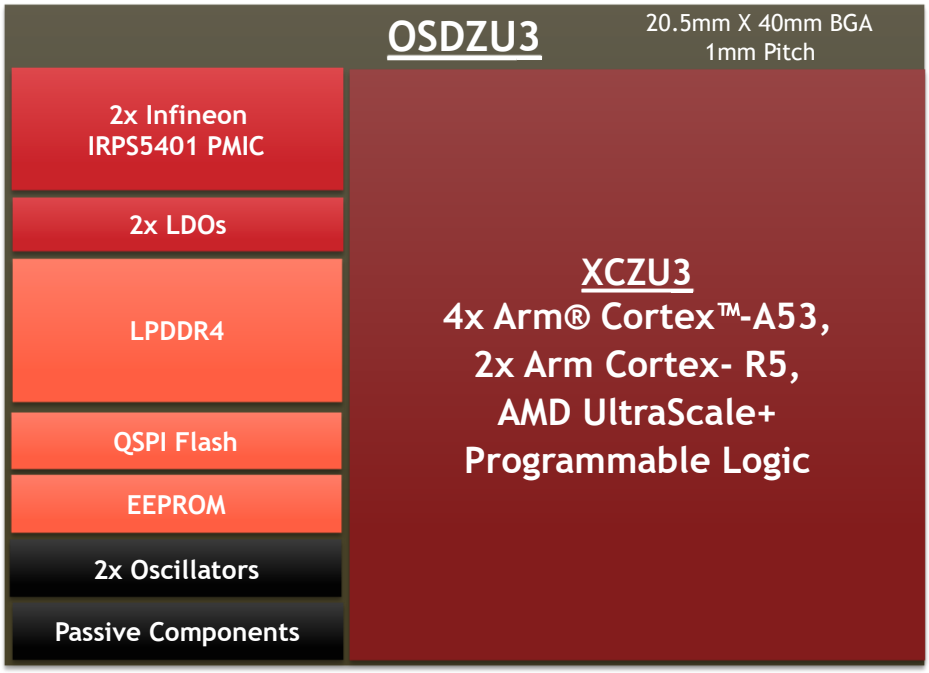


Figure 6-1 - OSDZU3 Internal Components

6.1 XCZU3 Processor

The heart of the OSDZU3 is the AMD Zynq® UltraScale+™ ZU3 MPSoC. It features a Quad-core Arm® Cortex®-A53 processor, a Dual-core Arm® Cortex®-R5 based real-time processing unit (RPU), a graphics accelerator and a Programmable Logic (PL) Array with 154,350 System Logic Cells, 141,120 CLB Flip-Flops, 70,560 CLB LUTs and 360 DSP Slices. Refer to Figure 4-1 and the references listed in Section 3 for more details. For detailed MPSoC specifications, refer to Table 3 in the Zynq UltraScale+ MPSoC Datasheet. The ZU3 MPSoC in the OSDZU3 is configured to perform identically to a ZU3 standalone device. Please refer to the User's Guide listed in the Reference Documents section for details on using the ZU3 processor.

6.2 LPDDR4 Memory

The OSDZU3 integrates LPDDR4 memory and handles all the connections needed between the ZU3 and the LPDDR4. All the required configuration has been completed for you in the Vivado Board Definition Files provided on the Octavo Systems website. A link can be found in Section 3 of this document.

If you wish to set them yourself, please refer to "Ch. 17: DDR Memory Controller" of "Zynq UltraScale+ Device Technical Reference Manual" listed in Section 3.

6.3 Oscillators

The OSDZU3 integrates a 33.333 MHz oscillator that is used as the main clock source. It also integrates a 32.768 kHz crystal as a real time clock (RTC) source.

This section outlines the key parameters for the oscillators that are integrated.

6.3.1 33.333 MHz Main Oscillator

The OSDZU3 integrates a 33.333 MHz oscillator and is used as the main clock source. The key parameters for the 33.333 MHz oscillator are outlined in Table 6-1.

Table 6-1 - 33 MHz MEMS Oscillator Parameters

Parameter	Min	Typ	Max	Units	Notes
Active Supply Current		3.5	5.0	mA	
Frequency Stability			±50	ppm	All temp ranges
Period Jitter, RMS			3	ps_{RMS}	
Frequency		33.333		MHz	

To disable the Oscillator the OSC_OE pin must be pulled low (VSS).

Note: The Oscillator has a 10K Ohm internal pull up on OSC_OE. This enables the oscillator by default. It is recommended that designs incorporate a test point for OSC_OE.

6.3.2 32.768 kHz Crystal for Real Time Clock

The OSDZU3 integrates a 32.768 kHz crystal to create a real time clock (RTC). To use the RTC a 10Mohm resistor must be added externally to the OSDZU3 between balls PS_PADI and PS_PADO.

The key parameters for the 32.768 kHz oscillator are outlined in Table 6-2.

Table 6-2 - 32 kHz Crystal Parameters

Parameter	Min	Typ	Max	Units	Notes
Frequency Stability			±20	ppm	@25C
Frequency		32.768		KHz	

6.4 EEPROM

The OSDZU3 contains a 32kb (4kB) EEPROM for non-volatile storage of configuration information. The EEPROM uses I2C to communicate with the ZU3. It is connected internally to the same I2C bus (PMIC_SCL and PMIC_SDA) as the 2 PMICs. The 7-bit I2C address is 0x50. This I2C bus needs to be connected to the ZU3 through OSDZU3 Ball Grid Array on the PCB.

6.4.1 EEPROM Contents

EEPROM address space 0x000 to 0xEFF is empty and can be used for board specific information or other configuration data. The final 256 bytes of the EEPROM (0xF00 to 0xFFF) are reserved for device specific information. The reserved space contents of the EEPROM can be found in Table 6-3.

Table 6-3 - EEPROM Contents Programmed by Octavo Systems

Name	Description	Size (bytes)	Start address	End address	Contents
RSVD	Reserved for Future Use	256	0xF00	0xFFF	All 0xFF

6.4.2 EEPROM Write Protection

By default, the EEPROM is write protected (i.e., the EEPROM_WP pin is pulled high to the +3V3_ON rail). To program values into the EEPROM, it is required to drive the EEPROM_WP pin to a logic low. See the OSDZU3 Layout Guide in the Reference Documents section for layout / manufacturing recommendations for the EEPROM_WP pin.

6.5 QSPI FLASH

The OSDZU3 may contain a QSPI Flash connected to MIO0 through MIO5. The internal QSPI is available for external programming using the MIO0 through MIO5 pins. See Table 5-5 for the specific pin mapping.

The QSPI is not dual voltage and will require either 3.3V or 1.8V. The OSDZU3 part number will specify the voltage level required by the QSPI. The voltage of VCCO_PSIO_500 must match the voltage required by the IO standard of the QSPI.

7 Power Management

The power management portion of the OSDZU3 consists of two Infineon IRPS5401 PMICs and two LDOs. The Power Management System provides the necessary power rails to the OSDZU3, LPDDR4s, EEPROM, QSPI and all the other internal components of the OSDZU3. It also provides power supply outputs that may be used to power circuitry external to the OSDZU3. This section describes how to power the OSDZU3 in a system and which output voltage rails may be used externally to the OSDZU3.

Note: For the PMICs to perform as described in this document you must add the resistors to the PMIC1_MTP and PMIC2_MTP pins as outlined in Table 5-8

7.1 IRPS5401 Configuration

The IRPS5401 PMICs have been preprogrammed to perform as described in this document. For details on the configuration of the IRPS5401 PMICs in the OSDZU3 refer to the OSDZU3 PMIC Configuration files linked in the Reference Documents section.

7.1.1 Switching Frequency

The switching frequency programmed into the IRPS5401 is dependent on the temperature designator for the OSDZU3 device. Table 7-1 outlines the default frequency settings for the different temperature grades.

Table 7-1 - Switching Frequency by Temperature Designator

	Temperature Designator			
Parameter	**B**	**I**	**H**	**Units**
Switching Frequency	923	923	1933	kHz

7.2 Power Block Diagram

Figure 7-1 shows the power connections to the various components (e.g., the ZU3, LPDDR4, etc.) within the OSDZU3. Some power inputs of the XCZU3 are not connected to power inputs within the OSDZU3 and must be connected externally on the PCB. Please see the Sections below on the power inputs and outputs for more details. Additionally, see Table 8-3 and Table 8-4 for information on the specifications for power outputs.

For further details on the power distribution for the XCZU3 refer to the Zynq UltraScale+ Device Technical Reference Manual. Refer to Table 3-1 of this data sheet for the link to this document and other useful documents.

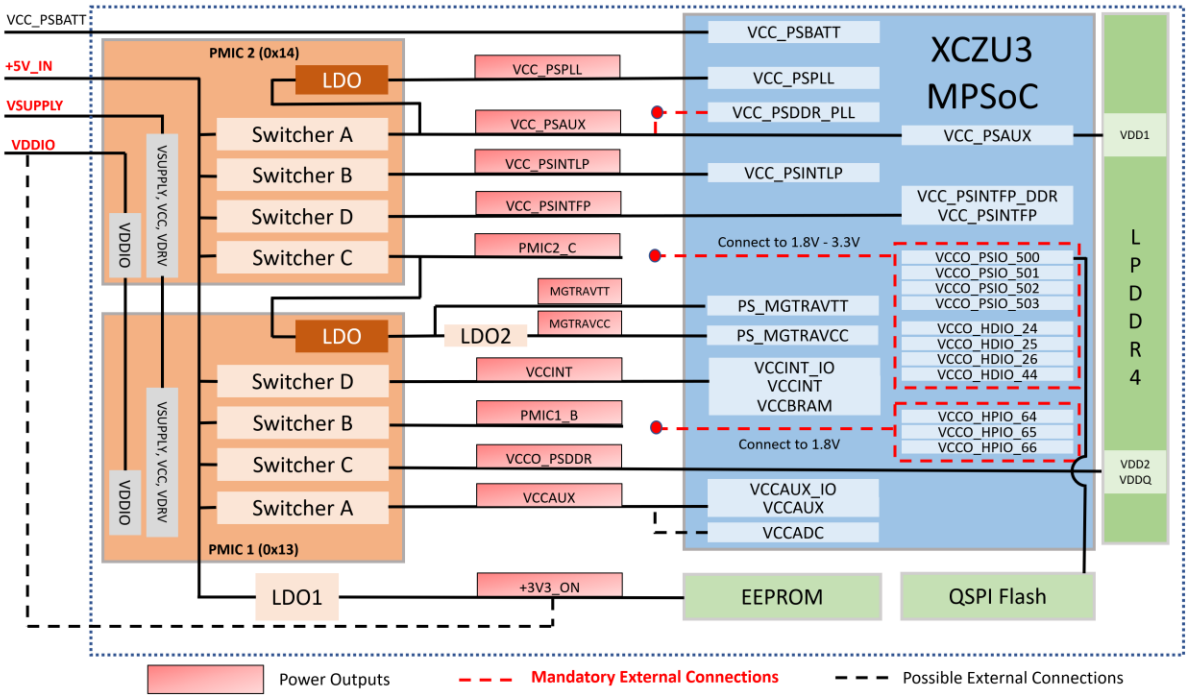


Figure 7-1 - OSDZU3 Power Usage Block Diagram.

Table 7-2 - PMIC voltage output requirements for OSDZU3

PMIC/LDO Voltage Out	XCZU3/OSDZU3 Power Rail Name	Voltage (V)	Availability for external use	ZU3 Power Domain
PMIC1_VOUT_A	VCCAUX, VCCAUX_IO(1)	1.8	Yes	PLPD
PMIC1_VOUT_B	PMIC1_B	1.8	Yes	
PMIC1_VOUT_C	VCCO_PSDDR	1.1	No	FPD
PMIC1_VOUT_D	VCCINT, VCCINT_IO(1), VCCBRAM(1)	0.85	No	PLPD
PMIC1_VO_LDO	+MGTRAVTT	1.8	No	FPD
LDO2	+MGTRAVCC	0.9	No	FPD
PMIC2_VOUT_A	VCC_PSAUX	1.8	Yes	LPD
PMIC2_VOUT_B	VCC_PSINTLP	0.85	No	LPD
PMIC2_VOUT_C	PMIC2_C	3.3	Yes	
PMIC2_VOUT_D	VCC_PSINTFP, VCC_PSINTFP_DDR(1)	0.9	No	FPD
PMIC2_VO_LDO	VCC_PSPLL	1.2	No	FPD, LPD
LDO1	+3V3_ON	3.3	No	

(1) Internal XCZU3 power input connected to OSDZU3 power rail

7.3 PMIC Control and Communication Signals

The PMICs and the processor interact through an I2C bus. Figure 7-2 shows the required interface between the ZU3 and the PMICs. Note that the two signals ***PMIC_SDA*** and ***PMIC SCL*** are connected to both PMICs and the EEPROM. They will need to be connected on the PCB via the Ball Grid Array to the ZU3 (e.g., MIO 72 and 73 balls). Both ***PMIC_SDA*** and ***PMIC_SCL*** are internally pulled high to VCCO_PSIO_503 through 10K ohm resistors.

Based on the respective ADDR_PROT resistors listed in Table 4-1 the 7-bit I2C addresses of PMIC1 and PMIC2 are 0x13 and 0x14 respectively.

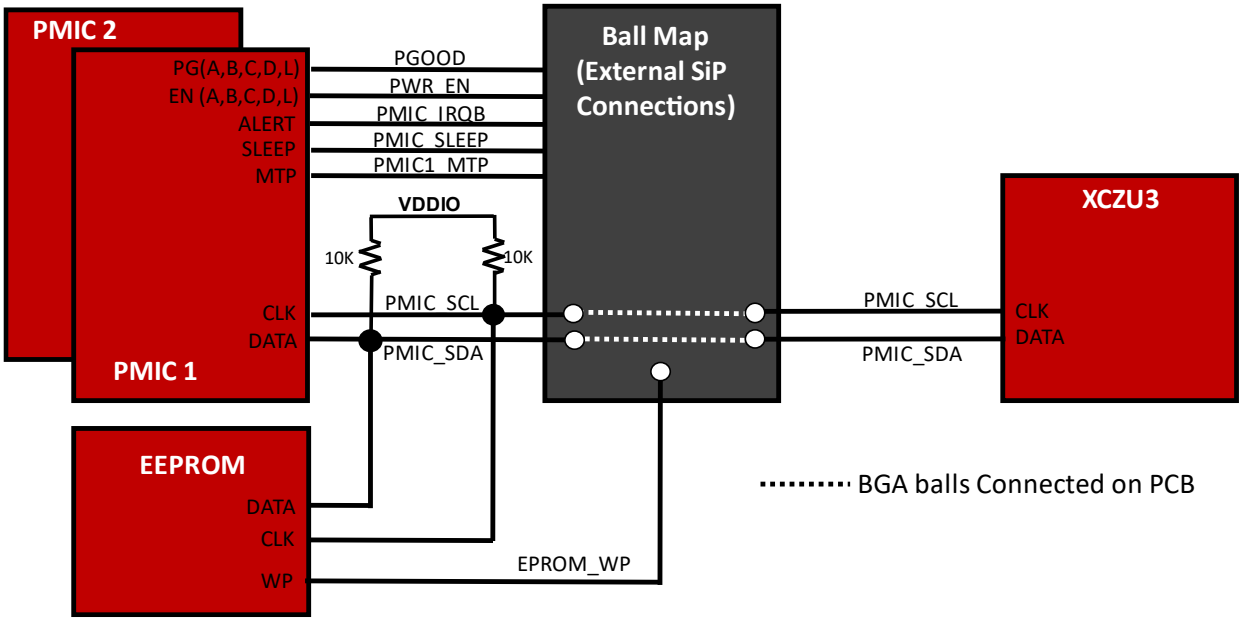


Figure 7-2 - OSDZU3 PMIC Interface Diagram

NOTE: The I2C bus used to connect the XCZU3 to the PMICs must have the same voltage level as VDDIO, 3.3V.

7.4 Main Power Input

OSDZU3 has five power inputs, +5V_IN, VSUPPLY, VCC_PSBATT, VDDIO, and VCC_PSDDR_PL. +5V_IN is the main power input for the devices, VSUPPLY is the power supply for the internal PMIC circuitry, VCC_PSBATT is the battery input used for low power modes, VDDIO provides power to the I/O of the PMICs and EEPROM, and VCC_PSDDDR_PLL provides power to the PLL Controller for the internal DDR. All rails except +5V_IN and VCC_PSBATT can be supplied with power outputs of OSDZU3.

7.4.1 +5V_IN Power Input

The OSDZU3 is powered by +5V_IN which is connected to the PMICs and LDO1. The OSDZU3 supports an input voltage range from 4.5V to 5.5V. All the DC-to-DC converters of PMIC1 and PMIC2 as well as LDO1 are powered by the +5V_IN Power input. LDOs of both PMICs are powered by switcher outputs of the PMICs. LDO2 is powered by the LDO output of PMIC1.

7.4.2 VSUPPLY Power Input

VSUPPLY is internally connected to VCC and VDRV of the PMICs and must be connected to a voltage source ranging from 4.5V to 5.5V. It can be tied to the main power input that powers +5V_IN.

7.4.3 VCC_PSBATT Power Input

VCC_PSBATT is connected to the VCC_PSBATT pin on the ZU3 (See Table 5-7). Its recommended voltage range is 1.2V to 1.5V. It is multiplexed with VCC_PSAUX as the power source to the Real Time Clock (RTC), Crystal, the RTC counters and BBRAM, the battery powered domain. In normal operation, VCC_PSAUX powers this domain. When VCC_PSAUX is powered down, VCC_PSBATT is used to power the battery powered domain of the ZU3.

7.4.4 VDDIO

VDDIO provides I/O power for the PMICs and EEPROM. It must be connected to a 3.3V source, preferably +3V3_ON.

7.4.5 VCC_PSDDR_PLL

VCC_PSDDR_PLL is a 1.8V nominal supply that provides power to the PLL used for the PS_DDR controller. The 1.8V power rail should be chosen based on the power mode requirements of the application.

Figure *7-3* shows an example of how the voltage rail VCC_PSDDR_PLL can be powered by VCC_PSAUX. Note that the ferrite bead and 10µF Capacitor must be connected external to the OSDZU3.

Further information can be found in Chapter 1 of the PCB Design User Guide from AMD listed in Table 3-1.

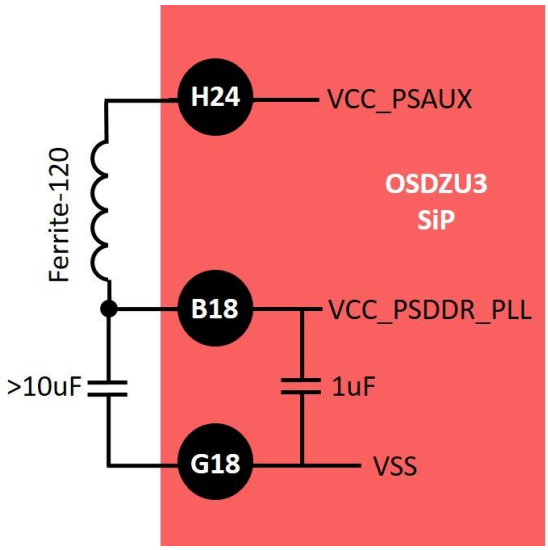


Figure 7-3.- Example of how to power VCC_PSDDR_PLL.

7.5 Power Output

The two PMICs and two LDOs integrated into the OSDZU3 produce the output power supplies described in this section. Each of the power supplies has a default output voltage. See Figure 7-1 and Table 7-2 for details on the default output voltages. For further information on how the PMICs have been programmed please refer to the PMIC data sheet listed in Table 3-1.

Two of the output power supplies (PMIC1_B and PMIC2_C) are for external use and are user adjustable. The other output power supplies should not be adjusted as doing so may cause the OSDZU3 device to not function correctly.

The power rails which may be used externally are listed in Table 7-2. Be careful when using them externally as using them out of specification may prevent the OSDZU3 from functioning properly. All the voltage rails have been connected to the OSDZU3 ball map and may be used for debugging / monitoring the system and as reference voltage outputs.

7.5.1 VCCAUX

VCCAUX is generated by DC-DC converter A in PMIC1. Its voltage is 1.8V. It is included in the Programmable Logic Power Domain (PLPD). VCCAUX may be used externally. It is also the source for ZU3 power input rail VCCAUX_IO. See Table 7-2 for additional configuration details for these voltage rails.

7.5.2 VCC_PSAUX

VCC_PSAUX is generated by the DC-DC converter A in PMIC2. Its voltage is 1.8V. VCC_PSAUX may be used externally. Please refer to Table 8-4 for current limitations of external use of this rail and Table 4-5 for recommended bulk capacitance needed for external use. See Table 7-2 for required PMIC configuration of this voltage rail.

7.5.3 User programmable Rails

Two of the DC-to-DC voltage rails, one from each PMIC is user programmable. One is PMIC1_B and the other is PMIC2_C.

7.5.3.1 PMIC1_B

PMIC1_B is produced by DC-DC converter B of PMIC1. The input of PMIC1_B is connected to the +5V_IN pins of the OSDZU3. The PMIC1_B voltage rail is a user programmable output with an output voltage range of 0.25 volts to 2.55 volts.

PMIC1_B has been factory programmed to be 1.8V. Please refer to the PMIC programming application note for details on how to properly program PMIC1_B to a different voltage.

7.5.3.2 PMIC2_C

PMIC2_C is produced by DC-DC converter C of PMIC2. The input of PMIC2_C is connected to the +5V_IN pins of the OSDZU3. The PMIC2_C voltage rail is a user programmable output with an output voltage range from 2.55 volts to 5.1 volts.

PMIC2_C has been factory programmed to be 3.3V. Please refer to the PMIC programming application note to program the PMIC2_C to a voltage other than 3.3V (2.55 to 5.1V).

7.5.4 External Power References

These rails are only to be used to power internal components in the SiP. They are provided for test points and monitoring. They should not be used to power external components.

7.5.4.1 VCCO_PSDDR

VCCO_PSDDR is generated by DC-DC converter C in PMIC1. It provides the power to the LPDDR4 memories (Bank 504). Its voltage is set to 1.1V. It is included in the Full Power Domain (FPD). See Table 7-2 for required PMIC configuration of this voltage rail. It is not available for external use and is only available as a test point.

7.5.4.2 VCCINT

VCCINT is generated by DC-DC converter D in PMIC1. Its voltage is 0.85V. VCCINT should not be used externally. It is also the source for two other internal voltage rails: VCCINT_IO and VCCBRAM. These three voltage rails are part of the Programable Logic Power Domain (PLPD). See Table 7-2 for required PMIC configuration of this voltage rail.

7.5.4.3 VCC_PSINTLP

VCC_PSINTLP is generated by DC-DC converter B in PMIC2. Its voltage is 0.85V. It is part of the low power domain (LPD). VCC_PSINTLP shall not be used externally. See Table 7-2 for required PMIC configuration of this voltage rail.

7.5.4.4 VCC_PSINTFP

VCC_PSINTFP is generated by the DC-DC converter D in PMIC2. Its voltage is 0.85V. It is part of the Full Power Domain (FPD). See Table 7-2 for required PMIC configuration of this voltage rail.

7.5.4.5 VCC_PSPLL

VCC_PSPLL is generated by the LDO in PMIC2. By default, its voltage is set to 1.2V. See Table 7-2 for required PMIC configuration of this voltage rail. It is not available for external use and is only available as a test point.

7.5.4.6 +3V3_ON

+3V3_ON is generated by LDO1. It is connected internally to the various components in the OSDZU3EG. By default, its voltage is 3.3V. +3V3_ON shall not be used externally. See Table 7-2 for required PMIC configuration of this voltage rail.

7.5.4.7 +MGTRAVTT

+MGTRAVTT is generated by the LDO in PMIC1. By default, its voltage is 1.8V. It is part of the Full Power Domain (FPD). It is also the input to LDO2 which generates the +MGTRAVCC voltage rail. See Table 7-2 for required PMIC configuration of this voltage rail. It powers the PS-GTR Bank (505), is not available for external use and is only available as a test point.

7.5.4.8 +MGTRAVCC

+MGTRAVCC is generated by LDO2. By default, its voltage is 0.9V. It is part of the FPD. See Table 7-2 for required PMIC configuration of this voltage rail. It powers the PS-GTR Bank (505), is not available for external use, and is only available as a test point.

7.6 Bank Power Inputs

The various banks of the ZU3 (HDIO, HPIO, and PSIO) must have their power rails connected external to the OSDZU3 SiP. This allows the user to either connect each bank to an internal voltage rail or external voltage rail. Refer to Figure 5-1 which shows the banks in the ZU3.

Please refer to the OSDZU3 Schematic Check List in the Reference Documents section for more details on the options available to power the banks.

To provide the most flexibility the power inputs for the banks of the ZU3 (see Figure 5-1, Figure 7-1, Table 8-2, and Table 5-8 through Table 5-19 for additional detail) have been brought out to balls in the OSDZU3 Ball Grid Array so they can be connected to a power source that meets the application's requirements. These sources can either be internal power rails brought out to the Ball Grid Array or external power sources. Figure 7-4 is an example of how the input voltages to the various Banks may be powered from external sources. There are three groups of these power inputs: 1) VCCO_HPIO, 2) VCCO_HDIO, and 3) VCCO_PSIO.

7.6.1 HP I/O Banks (VCCO_HPIO)

Each user HP I/O bank has a total of 52 I/Os where 48 can be used as differential (24 differential pairs) or single-ended I/Os. The remaining four function only as single-ended I/Os. The XCZU3 has three HP I/O banks (64, 65, 66) and are powered by VCCO_HPIO_64, VCCO_HPIO_65 and VCCO_HPIO_66, respectively.

If all I/O in a single bank are unused, then the VCCO_HPIO power input for that bank can be left floating.

7.6.2 HD I/O Banks (VCCO_HDIO)

The XCZU3 has four HD I/O Banks (24, 25, 26, 44) Each user HD I/O bank has a total of 24 I/Os that can be used as differential (12 differential pairs) or single-ended I/Os. They are powered by VCCO_HDIO_24, VCCO_HDIO_25, VCCO_HDIO_26 and VCCO_HDIO_44, respectively.

If all I/O in a single bank are unused, then the VCCO_HDIO power input for that bank can be left floating.

7.6.3 MIO Banks and Configuration Banks (VCCO_PSIO)

MIO pins are shared between banks 500, 501, and 502 and are powered by VCCO_PSIO_500, VCCO_PSIO_501 and VCCO_PSIO_502, respectively. Configuration pins are in bank 503 which is powered by VCCO_PSIO_503.

If all I/O in a single bank are unused, then the VCCO_PSIO power input for that bank can be left floating.

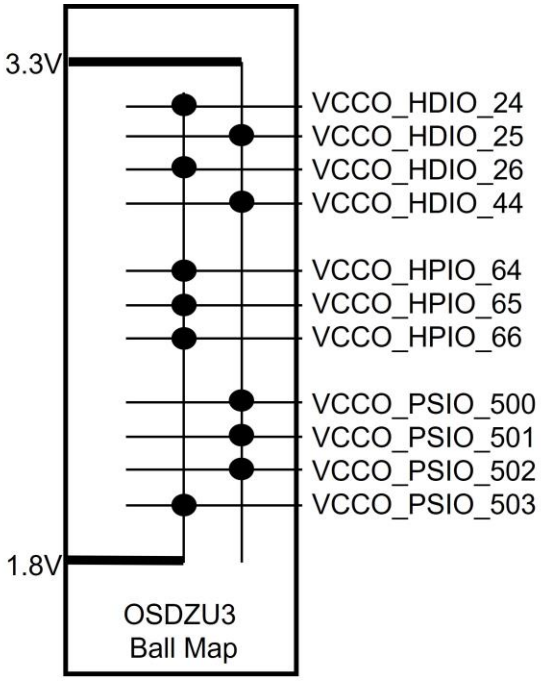


Figure 7-4 - OSDZU3 Example VCCO rails hooked up to 1.8V and 3.3V external sources.

7.6.3.1 VCCO_PSIO_500

The integrated QSPI Flash is connected to the XCZU3 through I/O on Bank 500 and thus determines the voltage that VCCO_PSIO_500 is connected to. VCCO_PSIO_500 must be connected to the same voltage of the QSPI as defined in Section 2 of this document.

Also note that the XCZU3 will not be able to boot from the eMMC interface if VCCO_PSIO_500 is connected to a 3.3V rail. eMMC boot is only supported when VCCO_PSIO_500 is connected to 1.8V and eMMC IOs are configured to operate at 1.8V.

7.7 Analog Power Inputs

To use the internal System Monitor capabilities of the XCZU3, the analog power inputs, VCCAUX and VCCADC should be connected.

7.7.1 VCCADC / GNDADC

VCCADC is the PL System Monitor power input. This voltage is relative to GNDADC and should nominally be 1.8V. There are no power sequencing requirements for VCCADC. We recommend connecting VCCADC to a 1.8V power output from the OSDZU3, for example VCCAUX, through a ferrite bead to reduce noise on the power input. Similarly, we recommend connecting GNDADC to GND through a ferrite bead to reduce noise on the ground connection. Additionally, we recommend placing a 0.1µF and 470nF capacitor between VDDADC and GNDADC.

VCCADC should never be tied to GND. If it is unused, it should be tied to VCCAUX.

GNDADC should always be connected to GND even if the System Monitor is not being used.

7.7.2 VCC_PSADC / GND_PSADC

VCC_PSADC is the PS System Monitor power input. This voltage is relative to GND_PSADC and should nominally be 1.8V. If this rail is used, it should be powered on at the same time as VCC_PSAUX. We recommend connecting VCC_PSADC to VCC_PSAUX through a ferrite bead to reduce noise on the power input. Similarly, we recommend connecting GND_PSADC to GND through a ferrite bead to reduce noise on the ground connection. Additionally, we recommend placing a 0.1µF and 470nF capacitor between VCC_PSADC and GND_PSADC.

VCC_PSADC should never be tied to GND. If it is unused, it should be tied to VCCAUX or VCC_PSAUX.

GND_PSADC should be always connected to GND even if the System Monitor is not being used.

7.7.3 VREFP/VREFN

VREFP is the externally supplied reference voltage input to the PL System Monitor. This voltage is relative to GNDADC and should nominally be 1.25V. There are no power sequencing requirements for VREFP. When using an external reference voltage, the regulated output should have a 0.1µF capacitor between VREFP and VREFN.

When using the on-chip reference voltage, VREFP should be connected to VREFN and connected to the analog ground, i.e. GNDADC.

7.8 PMIC I2C Interconnect

Both PMICs are managed by the XCZU3 through an I2C bus. **This I2C bus can be connected to any set of MIO pins that support either I2C0 or I2C1.** However, the OSDZU3's ball map has been laid out such that the required external interconnections can be simple to make. Figure 7-5 shows two examples on how this interconnection can be made. Either the two I2C pins, PMIC_SCL (P27) and PMIC_SDA (R27), can be connected to:

1) MIO72 (P26) and MIO73 (R26) respectively. This requires VCCO_PSIO_502 to be 3.3V.
2) MIO46 (T26) and MIO47 (U26) respectively. This requires VCCO_PSIO_501 to be 3.3V.

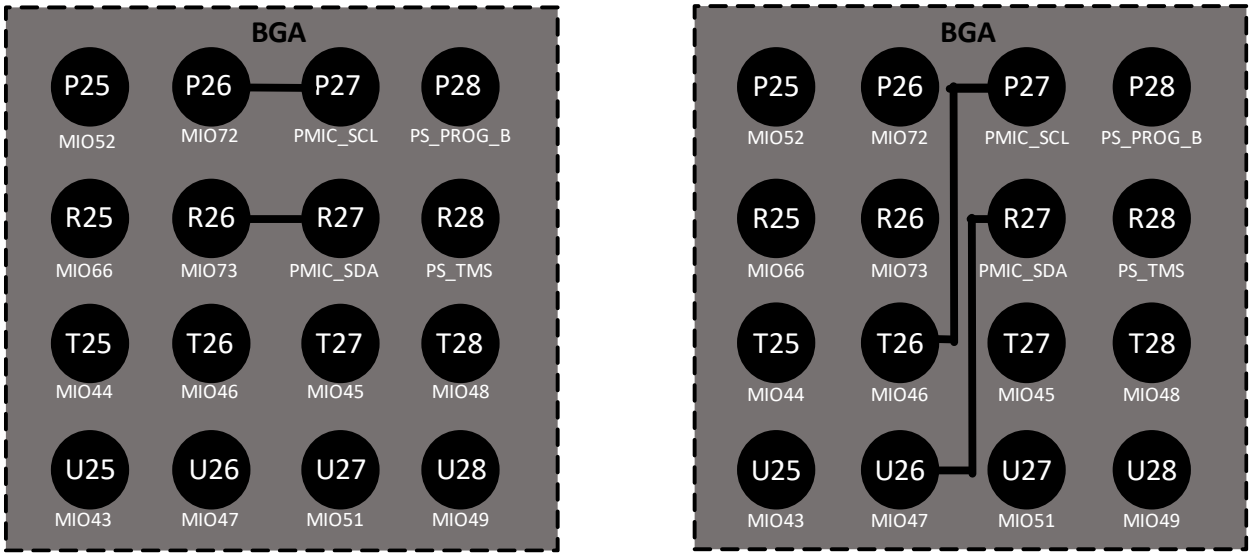


Figure 7-5 - Examples of two different ways to connect the PMIC I2C to the ZU3 processor.

7.9 Mode Selection

The XCZU3 has four pins which need to be connected to either VSS or VCCO_PSIO_503 to determine where the boot image is to be found. Table 7-3 lists the boot choices, and Figure 7-6 and Figure 7-7 show examples of how to properly connect the PS_MODE inputs to direct the ZU3 to a boot location.

Table 7-3 - List of Boot Modes based on Mode pin connections.

Boot Mode	Mode Pins (3:0)	Pin Location	CSU Mode	Description
PS JTAG	0000	JTAG	Slave	PSJTAG interface, PS dedicated pins.
Quad-SPI (24b)	0001	MIO (12:0)	Master	24-bit addressing (QSPI24).
Quad-SPI (32b)	0010	MIO (12:0)	Master	32-bit addressing (QSPI32).
SDO (2.0)	0011	MIO (25:21, 16:13)	Master	SD 2.0.
NAND	0100	MIO (25:09)	Master	Requires 8-bit data bus width.
SD1 (2.0)	0101	MIO (51:43)	Master	SD 2.0.
eMMC (1.8V)	0110	MIO (22:13)	Master	eMMC version 4.5 at 1.8V.
USB0 (2.0)	0111	MIO (52:63)	Slave	USB 2.0 only.
PJTAG (MIO #0)	1000	MIO (29:26)	Slave	PJTAG connection 0 option.
PJTAG (MIO #1)	1001	MIO (15:12)	Slave	PJTAG connection 1 option.
SD1 LS (3.0)	1110	MIO (51:39)	Master	SD 3.0 with a required SD 3.0 compliant voltage level shifter.

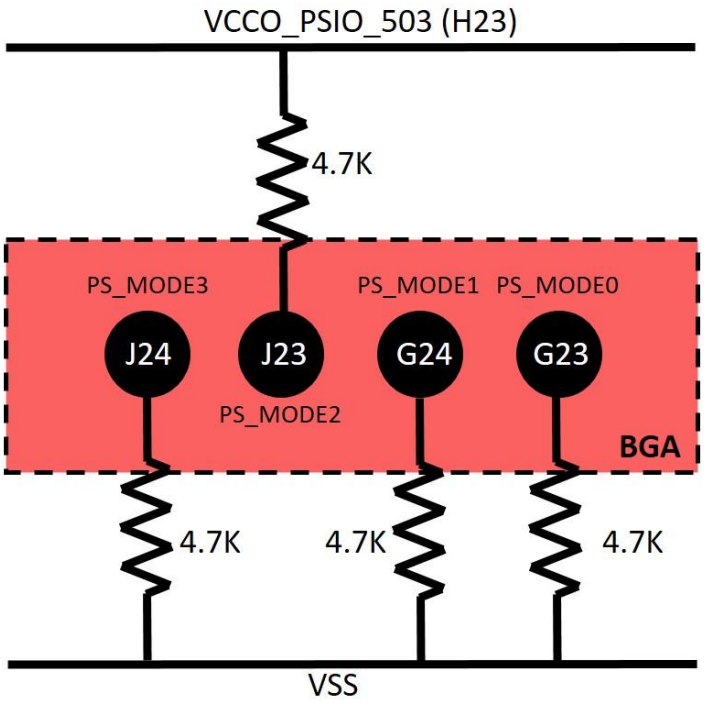


Figure 7-6 - Example of the pull up and down resistor configuration for the Mode Pins to indicate the boot code location to be the NAND.

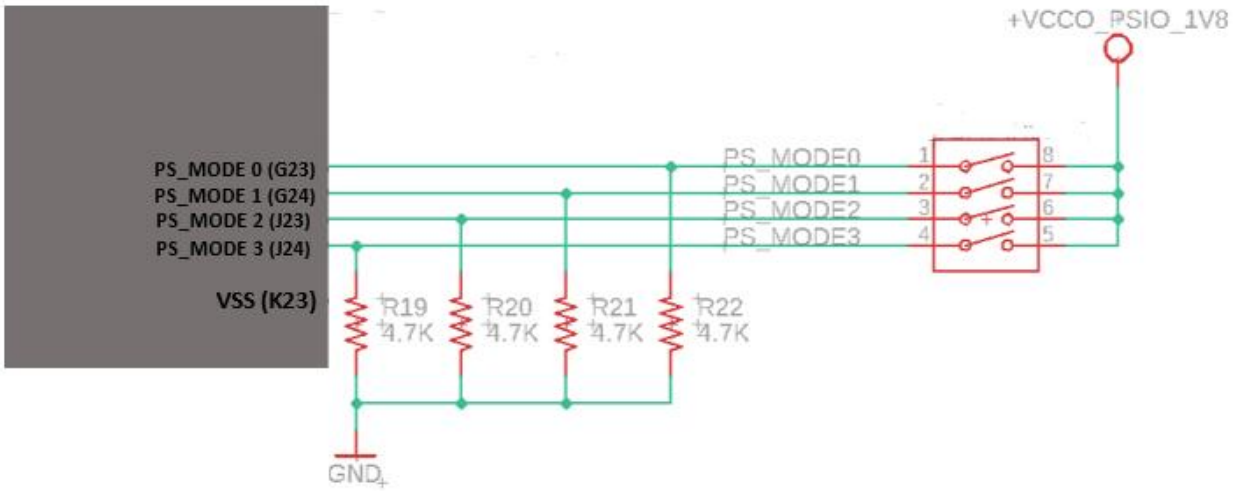


Figure 7-7 - Example of a configuration for the Mode Pins to indicate the boot code location. The switches are used to set the boot mode.

8 Electrical & Thermal Characteristics

Table 8-1 lists the absolute maximum voltage ratings for the OSDZU3 over its operating temperature range. The total current consumption of all power rails must not exceed the recommended input currents described in Table 8-2. This includes power consumption within the OSDZU3, including the memories, Oscillator, and other internal components as well as all external loads on the output power rails.

Table 7-2 lists the rails which may be used externally. Table 8-4 outlines the output specifications for power rails that can be used external to the OSDZU3. Finally, refer to Table 4-4 for the recommended external bulk capacitors.

The maximum current consumption of the internal power rails is outlined in Table 8-3.

Table 8-1 - OSDZU3EG Absolute Maximum Ratings(1) (2)

Description	Item	Value	Unit
Supply voltage range	+5V_IN	-0.3 to 6	V
Battery Input	VCC_PSBATT	-0.3 TO 2.0	V
VSUPPLY (VCC & VDRV) Input to the PMICs	VSUPPLY	-0.3 to 6	V
IO Voltage for the PMICs and EEPROM	VDDIO	-0.3 to 5.5	V
PS DDR PLL supply voltage	VCC_PSDDR_PL	-0.5 to 2	V
PL System Monitor supply relative to GNDADC	VCCADC	-0.5 to 2	V
PS SYSMON ADC supply voltage relative to GND_PSADC	VCC_PSADC	-0.5 to 2	V
PL System Monitor reference input relative to GNDADC	VREFP	-0.5 to 2	V
GND/AGND		-0.3 to 0.3	V
Tj (ZU3 Junction Temperature)	Commercial (B)	0 to 85	C
	Industrial (I)	-40 to 85	C
	Industrial Extended High (H)	-40 to 100	C

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to network ground terminal.

Table 8-2 - Recommended Operating Conditions (1) – Input Voltage Rails

Voltage Rail		Voltage				Current Limit	
	I/O	Min	Nom	Max	Unit	Max	Unit
Input supply voltage (+5V_IN)	I	4.5	5	5.5	V	3000	mA
VCC_PSBATT	I	1.2		1.5	V	500	mA
VSUPPLY	I	4.5		5.5	V	100	mA
VDDIO	I	1.71		3.465	V	500	mA
VCC_PSDDR_PLL	I	1.71	1.8	1.89	V	500	mA
VCCO_HDIO_24	I	1.14		3.4	V	500	mA
VCCO_HDIO_25	I	1.14		3.4	V	500	mA
VCCO_HDIO_26	I	1.14		3.4	V	500	mA
VCCO_HDIO_44	I	1.14		3.4	V	500	mA
VCCO_HPIO_64	I	0.95		1.9	V	500	mA
VCCO_HPIO_65	I	0.95		1.9	V	500	mA
VCCO_HPIO_66	I	0.95		1.9	V	500	mA
VCCO_PSIO_500	I	1.710		3.465	V	500	mA
VCCO_PSIO_501	I	1.710		3.465	V	500	mA
VCCO_PSIO_502	I	1.710		3.465	V	500	mA
VCCO_PSIO_503	I	1.710		3.465	V	500	mA
VCCADC	I	1.746	1.8	1.854	V	500	mA
VCC_PSADC	I	1.71	1.8	1.89	V	500	mA
VREFP	I	1.20	1.25	1.30	V	500	mA

(1) Over operating junction temperature range, unless otherwise noted.

Table 8-3 - Recommended Operating Conditions(1) – Output Voltage Rails – Internal Use

Voltage Rail		Voltage				Current output	
	I/O	Min	Nom	Max	Unit	Max	Unit
VCC_PSAUX(2)	O		1.8		V	1000	mA
VCCAUX(2)	O		1.8		V	1000	mA
VCCINT(2)	O		0.85		V	3750	mA
VCCO_PSDDR(2)	O		1.1		V	2000	mA
VCC_PSINTLP(2)	O		0.85		V	1000	mA
VCC_PSINTFP(2)	O		0.85		V	1500	mA
+3V3_ON(2)	O		3.3		V	250	mA

(1) Over operating junction temperature range, unless otherwise noted.
(2) Internal current limits. For use in XPE power modeling. See OSDZU3 Power Application Note.

Table 8-4 - Recommended Operating Conditions (1) – Output Voltage Rails – External Use

Voltage Rail		Voltage				Current output	
	I/O	Min	Nom	Max	Unit	Max	Unit
PMIC2_C(3)	O	2.55	3.3	5.1	V	1000	mA
PMIC1_B(3)	O	0.25	1.8	2.55	V	1000	mA
VCC_PSAUX(4)	O		1.8		V	1000	mA
VCCAUX(4)	O		1.8		V	1000	mA
VCCINT(2)	O		0.85		V	1	mA
VCCO_PSDDR(2)	O		1.1		V	1	mA
VCC_PSINTLP(2)	O		0.85		V	1	mA
VCC_PSINTFP(2)	O		0.85		V	1	mA
+3V3_ON(2)	O		3.3		V	1	mA

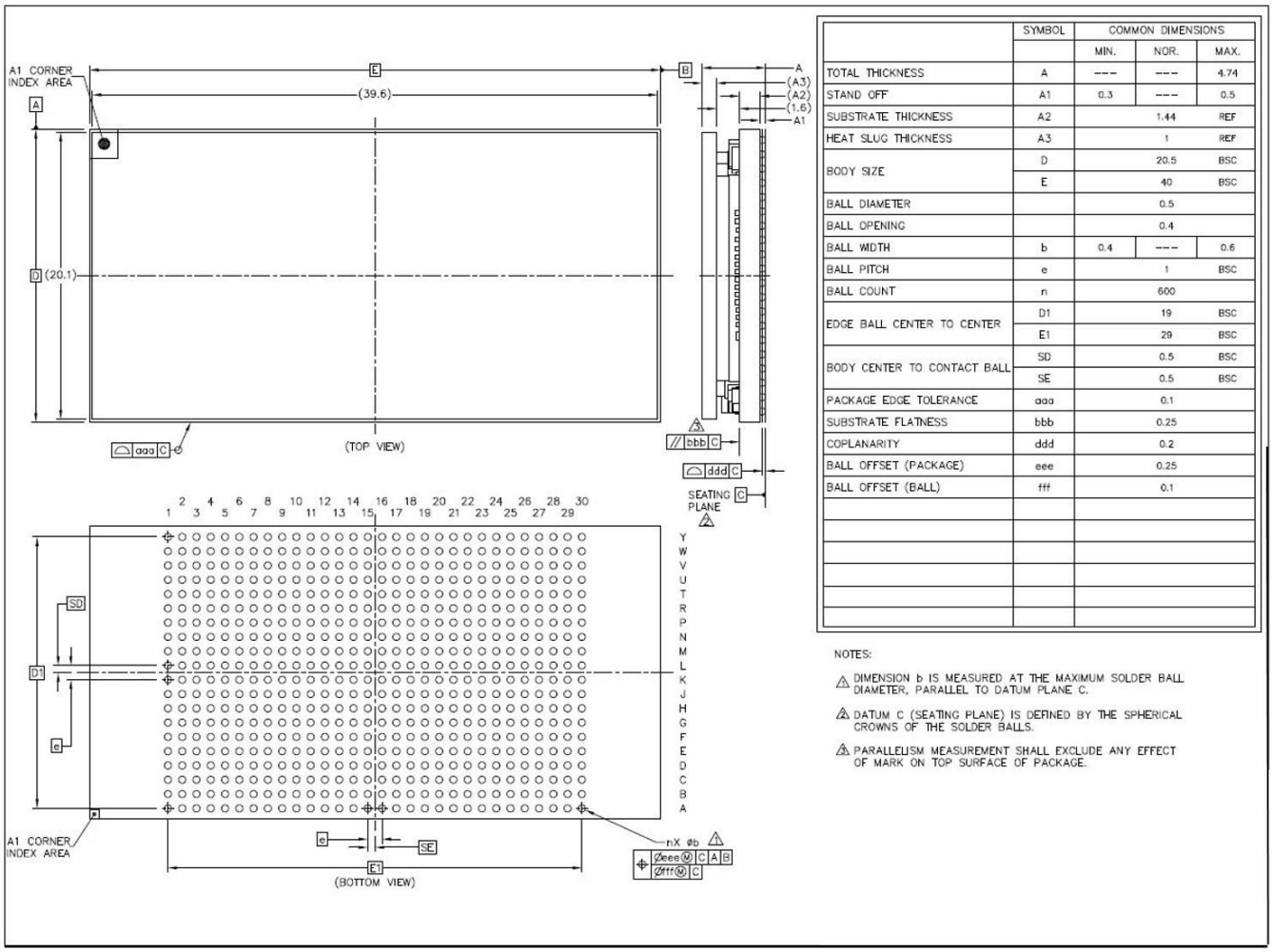
(1) Over operating junction temperature range, unless otherwise noted.
(2) Used internally. Can only be used as test point / voltage reference externally.
(3) User programmable / preprogrammed at factory to 3.3 (PMIC2_C) and 1.8V (PMIC1_B)
(4) Total Current, i.e., Internal + External current, should not exceed specified maximum current output

9 Packaging Information

The OSDZU3 is packaged in a 20.5mm X 40 mm BGA Package. It has a 20 x 30 Ball Grid Array in the center of the package consisting of 600 pins with 1 mm pitch. This section provides the specifics on this package.

9.1 Mechanical Dimensions

The mechanical drawings for the OSDZU3 are provided below. All measurements are in millimeters. Refer to the OSDZU3 Layout Guide for more details. A footprint and schematic symbol are available on the Octavo website.



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	4.74
STAND OFF	A1	0.3	---	0.5
SUBSTRATE THICKNESS	A2		1.44	REF
HEAT SLUG THICKNESS	A3		1	REF
BODY SIZE	D		20.5	BSC
	E		40	BSC
BALL DIAMETER			0.5	
BALL OPENING			0.4	
BALL WIDTH	b	0.4	---	0.6
BALL PITCH	e		1	BSC
BALL COUNT	n		600	
EDGE BALL CENTER TO CENTER	D1		19	BSC
	E1		29	BSC
BODY CENTER TO CONTACT BALL	SD		0.5	BSC
	SE		0.5	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
SUBSTRATE FLATNESS	bbb		0.25	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.25	
BALL OFFSET (BALL)	fff		0.1	

Figure 9-1 - OSDZU3 Mechanical drawing

9.1.1 Landing Pad Sizing

For the nominal ball diameter of 0.50mm, specification IPC-7351A states that for NSMD pads, the nominal land diameter is 0.40mm with a land variation of 0.45mm to 0.35mm. Footprints provided by Octavo Systems generally use the minimum land pad size to enable lower cost routing (see Layout Guide in the Reference Documents section for more information). However, some applications may require a larger land pad size to enable a more robust structural connection to the circuit board or for other manufacturing constraints. Check the requirements of the application and manufacturer to determine the appropriate land pad size.

9.2 Thermal Considerations

Power dissipation of the OSDZU3 SiP is highly dependent on the type of application. In most cases, an auxiliary heat sink will be required. Please see the Thermal Guide in the Reference Documents section for further information.

9.3 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

AMD provides a good overview of Handling & Process Recommendations in XAPP427 for this type of device. A link to the document can be found in the Reference Documents section of this document.

9.4 Storage Requirements

The OSDZU3 Family of devices are sensitive to moisture and need to be handled in specific ways to ensure they function properly during and after the manufacturing process. The OSDZU3 Family of devices are rated with a **Moisture Sensitivity Level (MSL) of 4**. This means that they are stored in a sealed Dry Pack with a desiccant bag and a Humidity Indicator Card (HIC). **If the HIC reads > 10% when read at 23 ± 5 C or the HIC is not present; the devices must be baked in per the directions in 9.4.3 before use.**

9.4.1 Floor Life

Once the sealed Dry Pack is opened the OSD335x-SM can be stored **for up to 72 hours in a room ≤ 30°C and ≤60% Relative Humidity (RH). If any of these conditions are not met the devices must be baked as outlined in section 9.4.3 before use.**

9.4.2 Shelf Life

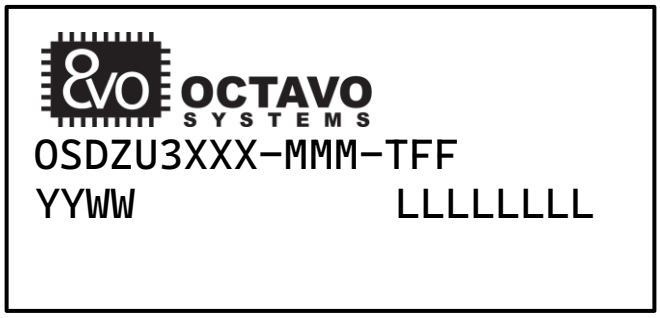
Octavo System devices are shipped in Moisture Barrier Bags (MBB) that have been partially vacuum-sealed with a desiccant bag. This combination supports a shelf life of the devices in an unopened factory bag for **24 Months from the seal date.** If this is exceeded, then the devices must be **baked per the directions in section 9.4.3 before use**.

9.4.3 Baking

The devices need to be baked if they have been exposed to environments outside of the guide lines outlined in sections 9.4.1 and 9.4.2, or if there is concern about the moisture content of the devices. The devices must be baked for **34hrs at 125°C with a RH of <5%.**

9.5 Part Marking

This section outlines the key markings that are found on the OSDZU3 device. There may be additional markings on the device that are not covered here.



9.5.1 Line 1: Part Number

- XXX – Processor Type and Speed Designator, Ex: EG1
- MMM – Memory Size Designator, Ex: 2G
- T – Temperature Designator, Ex: B, I, H
- FF – Option Designator, Ex : FA, FB

See Section 2 for more details.

9.5.2 Line 2: Date Code and Lot Number

- YY – Two Digit Year, Ex: 24
- WW – Two Digit Week of the Year, Ex: 16
- LLLLLLLL – Lot Number, Ex:PF282WVP0E