KNERON-KL630-007

KL630 SiP Series Specification

96board

1 INTRODUCTION

1.1 Overview

This document describes the functionalities of KL630 SiP SoC 96board. 96board has a dimension of (90mmx60mm) with 6-layer evaluation platform that enables users to evaluate and develop applications easily with KL630 SiP SoC. Figure 1-1 shows the snapshot of 96board.

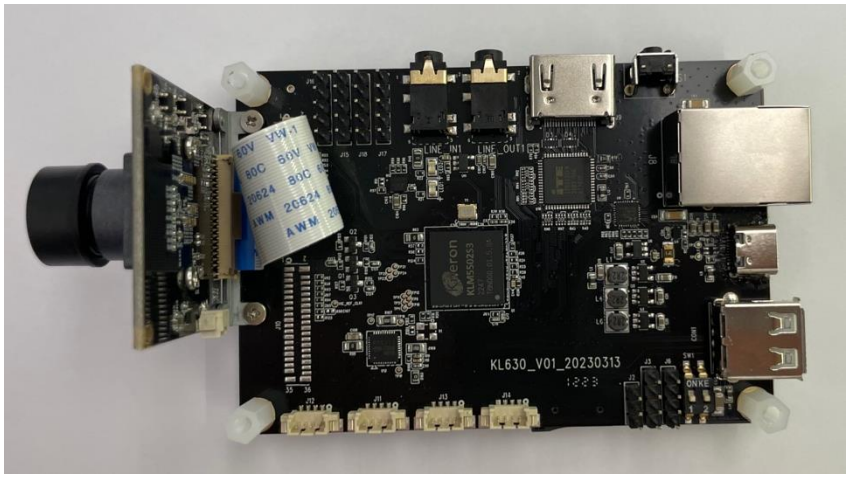

Figure 1-1 96board Snapshot

1.2 Features

KL630 96board is a stand-alone platform for emulating versatile IP-based camera. Essential peripherals of IP-based camera have been integrated in KL630 96board with some allocations reserved for optional devices. Figure 2 shows the functional block diagram of KL630 96board.

Block Diagram

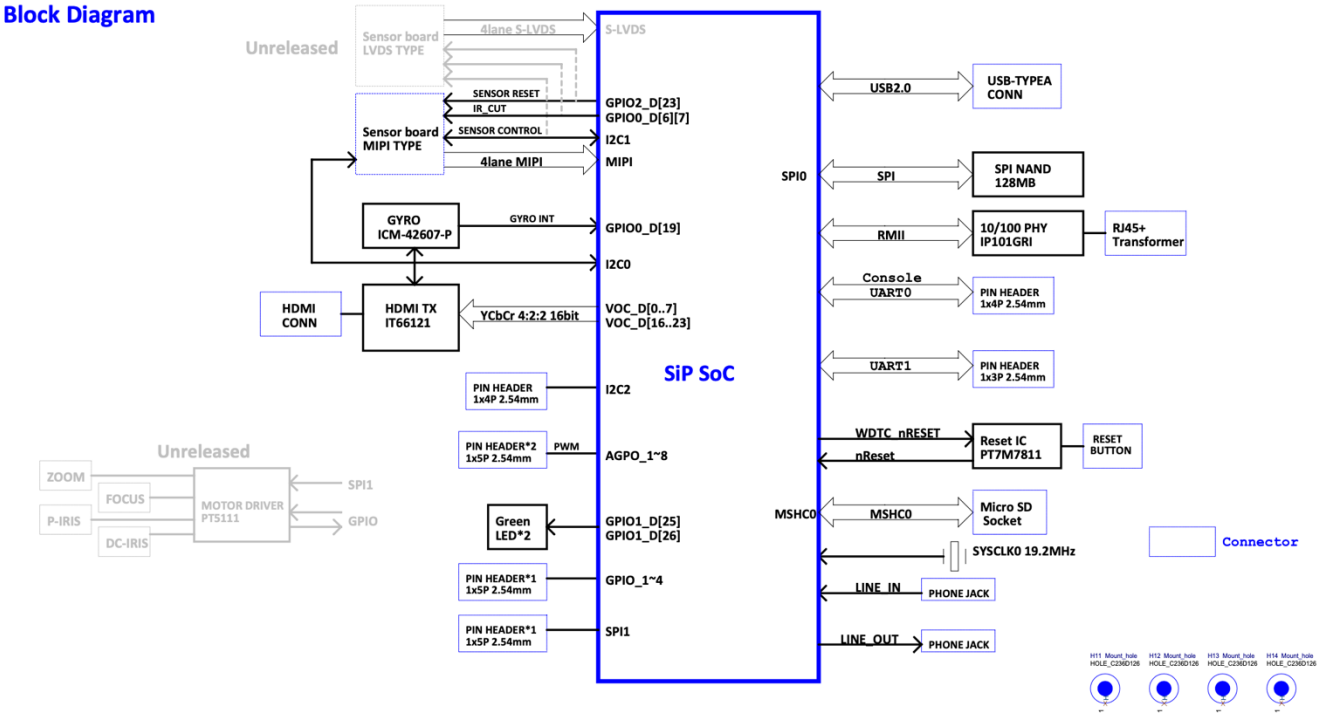

Figure 1-2 Block Diagram

The key components of KL630 96board include :

- One KLM5502S3 SiP SoC
- One 128MB SPI Flash
- One Gyro sensor
- One Micro SD card socket
- One 4-lane MIPI connector for MIPI CSI-2 CMOS sensor
- On board ethernet RJ45 connector
- On board line-in and line-out for audio recording and playback application
- One USB 2.0 connector
- One HDMI connector for video display
- Two pin headers for UART
- One pin header for GPIO
- Two pin headers for AGPO
- One pin header for I2C

- One pin header for SPI
- Single voltage power supply (5V DC)

Table 1-1 Board Specification

Items	Specification
SoC	KLM5502S3
CMOS sensor	Sony IMX662 2MP@30fps with HDR
Flash	128MB SPI NAND Flash
Network	RJ45 10/100 RMII
Console	4 pin UART interface
I/O	4 GPIO/ 8 AGPO
Video output	HDMI output
USB	USB 2.0 host/device
Audio	3.5mm Line in / Line out
SD Card	Micro SD
Power	USB type C 5V/2A
Working temperature	0 ~ 50°C

KL630 SoC is an ARM® based SoC which has embedded LPDDR2 or DDR3L SDRAM. KL630 SoC is embedded with video input controller (VIC) and video output controller (VOC) functions. To connect with LCD panels, a HDMI interface support the signal translation between KL630 SoC and the LCD panel.

The NPU core is the 3rd generation KDP series processor designed by Kneron® to accelerate major computing layers inside the convolutional neural network (CNN) and off-load the heavy computing from traditional CPU or GPU architecture. Its lego-like architecture services popular CNN models such as Yolo, Resnet, Mobilenet and Mobilenet-SSD and supports reconfigurable mechanism by INT8 or INT16 hybrid precisions. The inference AI model can be updated over the air (by OTA).

The built-in audio codec in KL630 SoC enables playback and recording functions on most applications. There are two microphone jacks (line-in and line-out) at the edge of the board. There is also a 10/100 Ethernet transceiver (IC Plus IP101GR) on EVM to support RMII Ethernet MAC protocol. Compressed video and audio data are streamed via Ethernet.

SPI NAND Flash and SD card can be used as boot device to boot up KL630 SoC. Boot code can be stored in any of the boot devices for executing the booting procedure.

1.3 Accessories

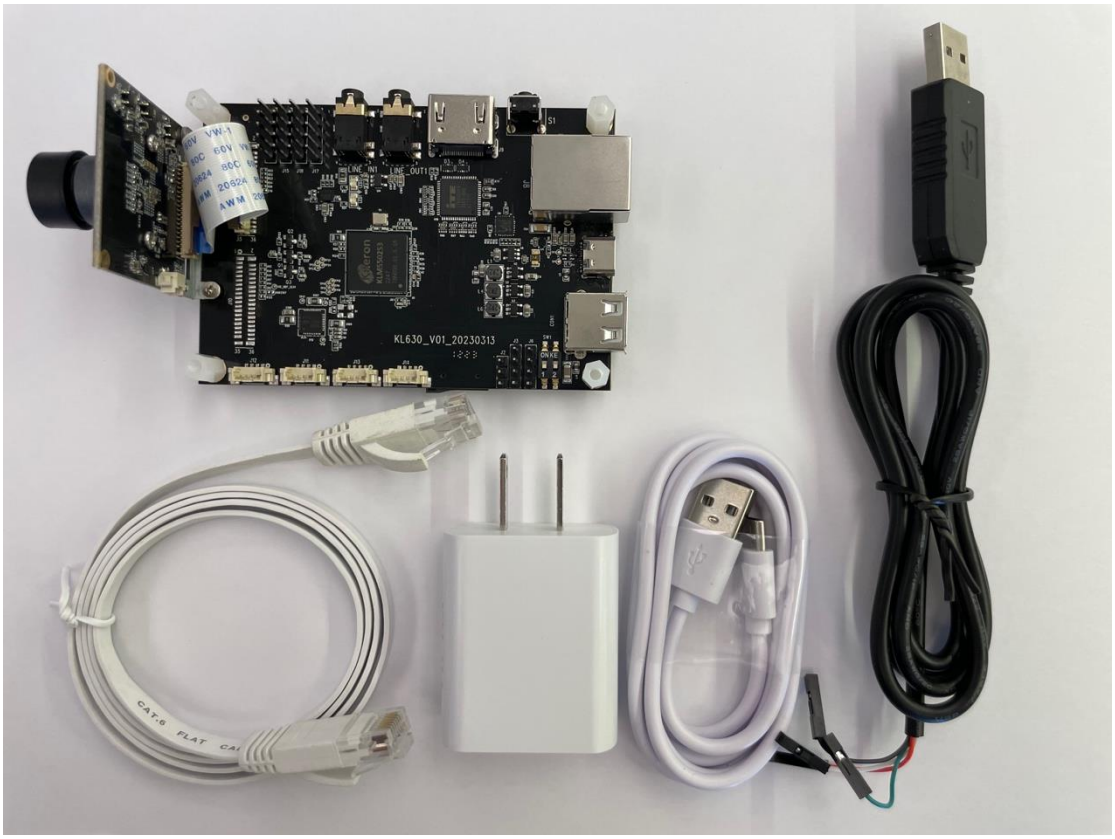

Figure 1-3 Bundled Accessories

Table 1-1 Bundled Accessories

Accessories	Qty
96board (with SoC)	1
Sony IMX662 CMOS Sensor Board	1
Lens & Holder (on CMOS Sensor Board)	1
Ethernet Cable	1
Power Adaptor	1
Power cable (USB type A to type C)	1
USB to UART console debug cable	1

1.4 I/O

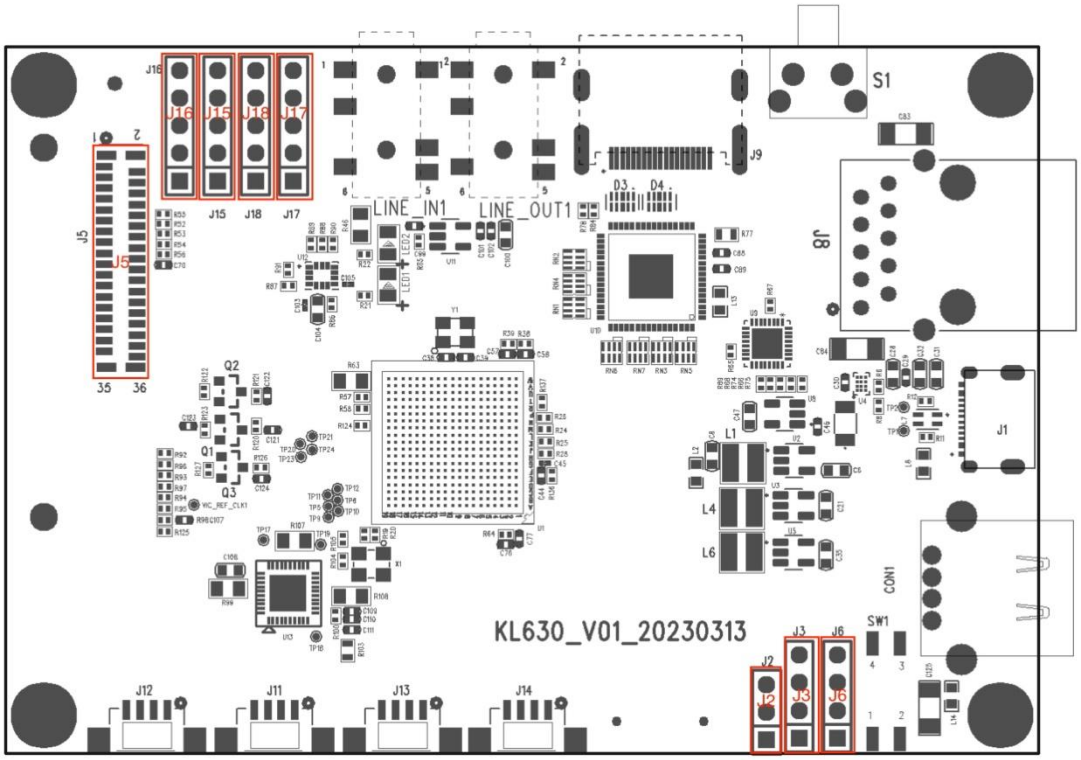

Figure 1-4 Top View

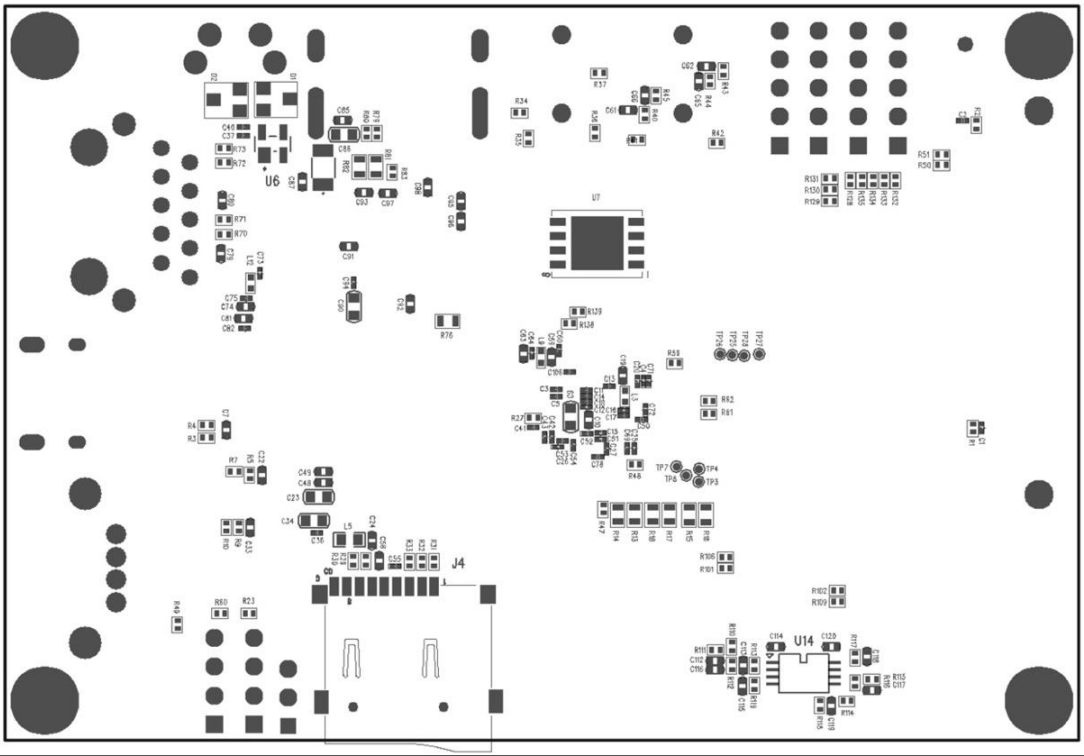

Figure 1-5 Rear View

Table 1-2 I/O Ports

Port No.	Description	Port No.	Description
J5	CMOS Sensor	J1	5V Power
LINE_IN1	Line in	CON1	USB
LINE_OUT1	Line out	J6	I2C
J9	HDMI output	J3	UART0
S1	Reset button	J2	UART1
J8	Ethernet	J15	GPIO
J4	Micro SD	J16	SPI
J17	AGPO	J18	AGPO
J11	Reserved	J12	Reserved
J13	Reserved	J14	Reserved

1.5 Pin Define

Table 1-3 J5 Pins

J5 MIPI CSI interface (Spec : FPC36p, 0.5mm)			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
PIN1	5V	PIN2	5V
PIN3	5V	PIN4	VIC0_VDDIO_SENSOR
PIN5	VIC0_VDDIO_SENSOR	PIN6	I2C0_SDA
PIN7	I2C0_SCL	PIN8	I2C1_SDA
PIN9	I2C1_SCL	PIN10	SENSOR_TEMP
PIN11	SEN_RST	PIN12	GND
PIN13	VIC_REF_CLK	PIN14	GND
PIN15	Reserved	PIN16	Reserved
PIN17	GND	PIN18	MIPI_CLK_P
PIN19	MIPI_CLK_N	PIN20	GND
PIN21	MIPI_DATA0_P	PIN22	MIPI_DATA0_N
PIN23	GND	PIN24	MIPI_DATA1_P
PIN25	MIPI_DATA1_N	PIN26	GND

J5 MIPI CSI interface (Spec : FPC36p, 0.5mm)			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
PIN27	MIPI_DATA2_P	PIN28	MIPI_DATA2_N
PIN29	GND	PIN30	MIPI_DATA3_P
PIN31	MIPI_DATA3_N	PIN32	GND
PIN33	IR_CUT_IN(+)	PIN34	IR_CUT_IN(-)
PIN35	GND	PIN36	3V3

Table 1-4 J2 Pins

J2			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
Pin 1	UART1_RXD	Pin 2	GND
Pin 3	UART1_TXD		

Table 1-5 J3 Pins

J3 Debug Console			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
Pin 1	UART0_RXD (Green)	Pin 2	GND (Black)
Pin 3	UART0_TXD (White)	Pin 4	3V3 (Red)

Table 1-6 J6 Pins

J6			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
Pin 1	I2C2_SCL	Pin 2	GND
Pin 3	I2C_SDA	Pin 4	3V3

Table 1-7 J15 Pins

J15			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
Pin 1	GPIO_1	Pin 2	GPIO_2
Pin 3	GPIO_3	Pin 4	GPIO_4
Pin 5	GND		

Table 1-8 J16 Pins

J16			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
Pin 1	SPI_1_CSn0	Pin 2	SPI_1_DO
Pin 3	SPI_1_CLK	Pin 4	Rreserved
Pin 5	GND		

Table 1-9 J17 Pins

J17			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
Pin 1	AGPO_0	Pin 2	AGPO_1
Pin 3	AGPO_2	Pin 4	AGPO_3
Pin 5	GND		

Table 1-10 J18 Pins

J18			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
Pin 1	AGPO_4	Pin 2	AGPO_5
Pin 3	AGPO_6	Pin 4	AGPO_7
Pin 5	GND		