Arm® Cortex®-M0 32-bit MCU + MATH coprocessor, 48 MHz, up to 200 KB flash/16 KB SRAM, real-time control

Features

- CPU and math: 32-bit Arm® Cortex®-M0 at 48 MHz (0.84 DMIPS/MHz), NVIC with 64 interrupt nodes, MATH coprocessor with 24-bit CORDIC and 32-bit divide
- On-chip memory: 8 KB ROM, 16 KB SRAM (parity), up to 200 KB flash (ECC)
- Power and reset: 1.8–5.5 V supply, power-on reset, brownout detector
- Clocking: on-chip clock monitor, external crystal support (32 kHz/4–20 MHz), internal slow and fast oscillators
- System control: window watchdog, real-time clock, pseudorandom number generator
- Communication: 2× USIC channels supporting UART, SPI, IIC, IIS, LIN, and CAN
- Analog: A/D converters (up to 12 inputs), comparators, temperature sensor
- Industrial control: 16-bit timers, POSIF (hall/quadrature encoders), BCCU (LED lighting)
- I/O ports: Up to 42 GPIOs, 1.8–5.5 V capable, high-current pads
- Debug: four breakpoints, two watchpoints, Arm® serial wire debug, single-pin debug
- Programming: single-pin bootloader, secure bootstrap loader (optional)
- Packages and tools: TSSOP-38, VQFN-40/48, LQFP-48; includes free ModusToolbox™ with low-level drivers and application support

Potential applications

- Motor control and automation: industrial drives, power tools, home appliances, and light electric vehicles
- Digital power conversion: switched-mode power supplies, LED lighting, EV charging, and renewable energy systems
- LED lighting system design: smart lighting systems, LED drivers, and lighting control applications

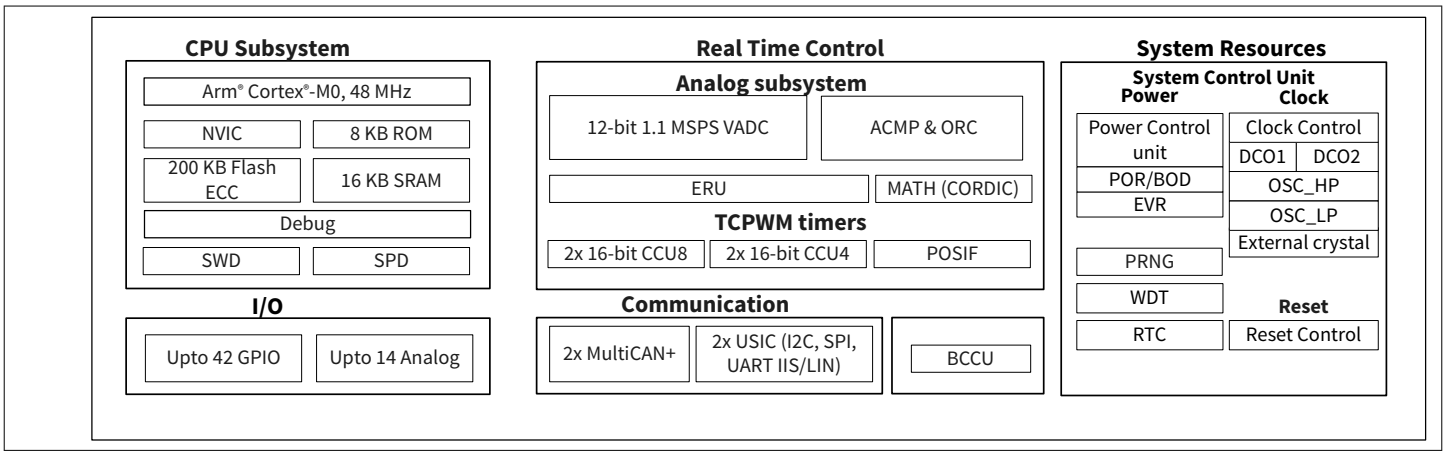
Green

Halogen-free

Lead-free

Description

The PSOC™ Control C1 (PSC1Mx) devices are based on a 32-bit Arm® Cortex®-M0 CPU running up to 48 MHz and are optimized for motor-control and power-conversion applications. In addition to the CPU subsystem, these devices integrate real-time control peripherals such as the VADC, ACMP/ORC comparators, CCU4 and CCU8 timer/PWM units, POSIF, ERU, and a MATH coprocessor (including DIV and CORDIC acceleration). For connectivity, the device provides two USIC modules for multi-protocol serial communication, and a MultiCAN+ interface with two CAN nodes.



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1 Introduction

The PSC1Mx devices are members of the PSOC™ Control family of microcontrollers. The PSC1Mx series addresses the real-time control needs of motor control and digital power conversion. It also features peripherals for LED lighting applications and human-machine interface (HMI).

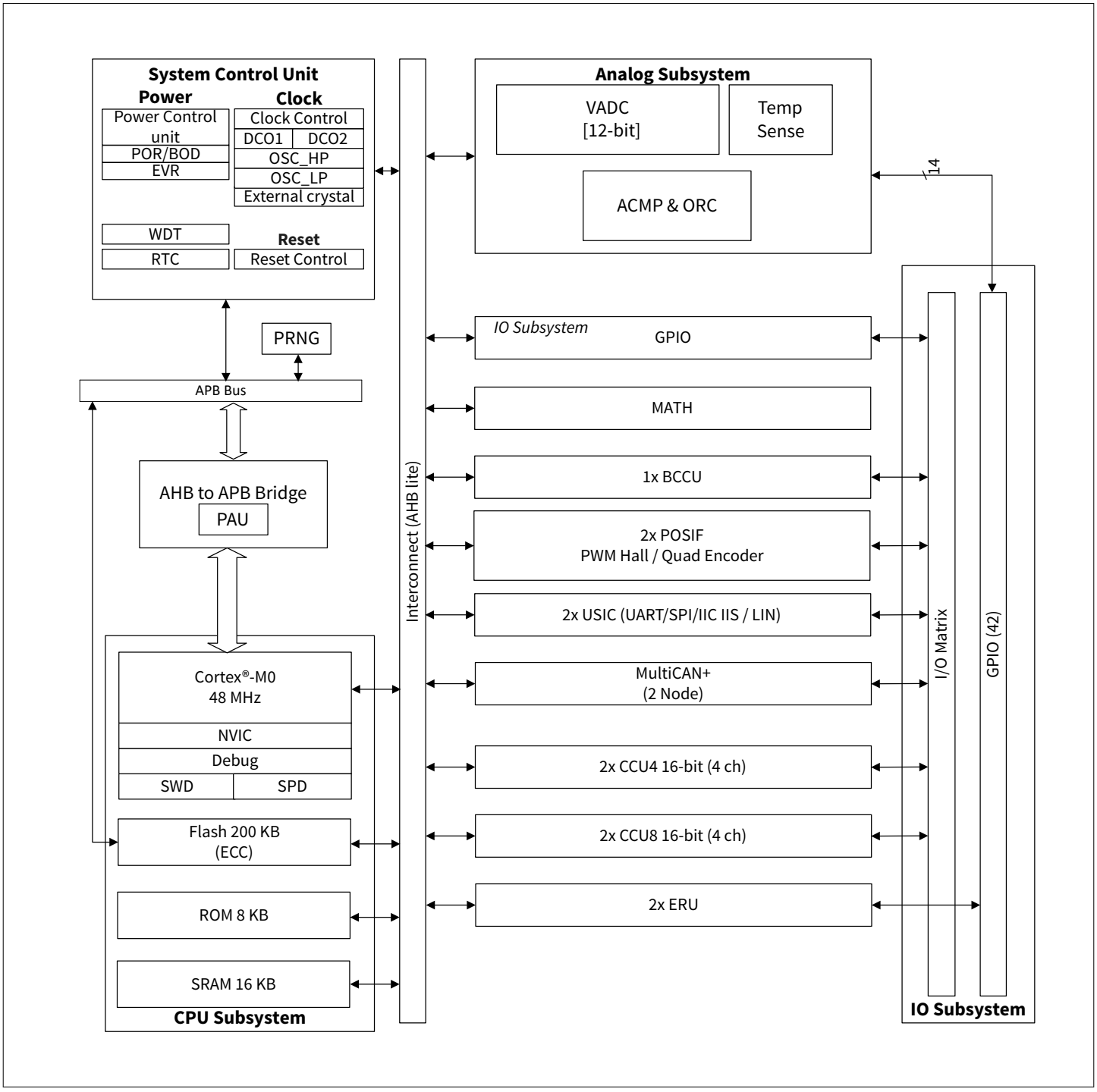


Figure 2 Block diagram

2 Detailed features

CPU subsystem

- 32-bit Arm® Cortex®-M0 CPU core
  - 0.84 DMIPS/MHz (Dhrystone 2.1) at 48 MHz
- Nested Vectored Interrupt Controller (NVIC)
- 64 interrupt nodes
- MATH coprocessor
  - 24-bit trigonometric calculation (CORDIC)
  - 32-bit divide operation
- 2 × 4 channels ERU for event interconnections

On-chip memories

- 8 KB ROM
- 16 KB SRAM (with parity)
- up to 200 KB flash (with ECC)

Supply, reset, and clock

- 1.8–5.5 V supply with power on reset and brownout detector
- On-chip clock monitor
- External crystal oscillator support (32 kHz and 4–20 MHz)
- Internal slow and fast oscillators without the need of PLL

System control

- Window watchdog
- Real-time clock module
- Pseudorandom number generator

Communication peripherals

- Two USIC channels, usable as:
  - UART (up to 12 Mb/s)
  - Single-SPI (up to 12 Mb/s)
  - Double-SPI (up to 2 × 12 Mb/s)
  - Quad-SPI (up to 4 × 12 Mb/s)
  - IIC (up to 400 Kb/s)
  - IIS (up to 12 Mb/s)
  - LIN interfaces (20 Kb/s)
- MultiCAN+, full-CAN/basic-CAN with two nodes, 32 message objects (up to 1 MBaud)

Analog front end peripherals

- A/D converters (up to 12 analog inputs)
  - Two sample-and-hold stages
  - Fast 12-bit ADC (up to 1.1 MS/s), adjustable gain
  - 0–5.5 V input range
- Up to eight channels out of range comparators
- Up to four fast analog comparators
- Temperature sensor (TSE)

Industrial control peripherals

- 2 × 4 16-bit 96 MHz CCU4 timers for signal monitoring and PWM
- 2 × 4 16-bit 96 MHz CCU8 timers for complex PWM, complementary high-/low-side switches and multi-phase control

- 2× POSIF for hall and quadrature encoders, motor positioning
- Nine channel BCCU (brightness and color control) for LED lighting applications

Up to 42 input/output ports

- 1.8–5.5 V capable
- Up to eight high-current pads (50 mA sink)

On-chip debug support

- Four breakpoints, two watchpoints
- Arm® serial wire debug, single-pin debug interfaces

Programming support

- Single-pin bootloader
- Secure bootstrap loader SBSL (optional)

Packages

- TSSOP-38 (9.7 × 6.4 mm^2)
- VQFN-40/48 (5 × 5/7 × 7/8 × 8 mm^2)
- LQFP-48 (7 × 7/12 × 12 mm^2)

Tools

- Free ModusToolbox™ toolchain with low-level drivers and applications

3 Block functional description

3.1 CPU

- Arm® Cortex®-M0 processor: A 32-bit processor core with a three-stage pipeline von Neumann architecture, designed for low power, and high performance
- A 32-bit hardware multiplier for fast arithmetic operations
- Math coprocessor (MATH): A module that supports the CPU in math-intensive computations, comprising of two independent sub-blocks:
  - Divider Unit (DIV): Performs signed and unsigned 32-bit division operations
  - CORDIC (COrdinate Rotation DIgital Computer) coprocessor: Computes trigonometric, linear, or hyperbolic functions, enabling efficient calculation of complex mathematical operations
- Nested Vectored Interrupt Controller (NVIC): An embedded interrupt controller with four interrupt priority levels, providing low latency interrupt processing and fast execution of interrupt service routines (ISRs)
- Sleep modes: Integrated sleep modes, including a deep sleep function, to optimize low power consumption and rapidly power down the device
- Debug solution: A complete hardware debug solution with single-pin debug (SPD) or 2-pin Serial Wire Debug (SWD), and extensive hardware breakpoint and watchpoint options
- Deterministic interrupt handling: High-performance interrupt handling with hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations, reducing interrupt latency and overhead

The CPU subsystem provides a highly efficient and flexible processing platform, with a range of features to support low power, high performance, and ease of use. The integrated NVIC and sleep modes enable fast and efficient interrupt handling and low power consumption, while the debug solution provides high system control and visibility.

3.2 Memory

The device features multiple nonvolatile and volatile memory types. The CPU and other bus masters can access any memory block. The number of wait states depends on the access path.

3.2.1 Flash

Up to 200 KB of on-chip flash memory store code or constant data. Dynamic error correction provides high read data security for all read accesses. Reading by word, writing by block, and erasing by page (256 b) or sector (4 KB). Up to 50,000 erase cycles per page.

3.2.2 BOOT ROM (BROM)

8 KB of ROM memory for boot code execution and exception vector table. The ROM contains system basic initialization sequence code and is executed immediately after reset release. The bootstrap loaders (BSL) and user routines are also stored in the ROM.

3.2.3 RAM

The device has 16 KB SRAM memory, with provision of retaining memory during Deep Sleep power mode. SRAM has ECC support for soft error detection and correction.

3.3 Clock system

The PSOC™ Control C1 clock system is responsible for providing clocks to all subsystems requiring clocks and switching between different clock sources without glitching. The clock system ensures that no metastable conditions occur and provides a range of clock sources, including:

- **DCO1**: A 48-MHz clock source with a frequency range of 188 kHz to 96 MHz
- **DCO2**: A 32-kHz clock source used as a standby clock and for the real-time clock (RTC)
- **OSC_HP**: A high-precision oscillator circuit that can drive an external crystal or accept an external clock source, with a frequency range of 4–48 MHz
- **OSC_LP**: A low-power oscillator circuit used for the RTC, with a frequency of 32.768 kHz
- **External clock**: An external clock source that can be used as an input to the clock system, with a maximum frequency of 48 MHz

The clock system also features:

- **Clock gating**: A feature that allows the clock to be gated on and off for individual peripherals, to reduce power consumption
- **Clock blanking**: A feature that freezes the clock input to the fractional divider to regulate the load change, to prevent a brown-out reset

The clock system generates a range of clock signals, including the main clock (MCLK), the fast peripheral clock (PCLK), and the slow peripheral clock (SPCLK), which are derived from the DCLK signal. The DCLK signal is generated by the clock doubler and can be selected from either the DCO1 clock source or the external clock source via the OSC_HP oscillator.

3.4 Watchdog timer (WDT)

The WDT is implemented as an independent window watchdog with a 32-bit counter. Servicing must be performed within a valid time window; otherwise, the module can first issue a pre-warning alarm and then request a watchdog reset if the fault is not recovered. The alarm path is routed through the system service request handling, while reset request is forwarded to reset control logic. WDT clocking is independent of the bus clock and supports standby-clock-based operation for low-power supervision use cases.

3.5 Real-time clock (RTC)

The RTC tracks time and calendar fields including seconds, minutes, hours, date, month, and year, with automatic leap year correction. It supports programmable alarm matching and periodic/time service request generation, enabling scheduled firmware activity and wake up from Sleep and Deep Sleep modes. RTC clock source selection is controlled through SCU clock control, and RTC programming is integrated through the SCU-side register model with mirrored RTC register access.

3.6 Reset

The device can be reset from various sources, including a software reset. Reset events are asynchronous and ensure reversion to a known state. The reset cause (WDT, POR/brownout, faults, debug, software, and clock) is recorded in a register, which is sticky through reset, and allows the software to determine the cause of the reset.

3.7 Analog subsystem

The PSOC™ Control C1 hosts a number of interfaces to connect to the analog world.

3.7.1 Analog-to-Digital Converter (VADC)

The Versatile Analog-to-Digital Converter () module consists of independent kernels which operate according to the successive approximation principle (SAR). The resolution is programmable from 8-12 bit. The kernel provides a versatile state machine allowing complex measurement sequences. The kernels can be synchronized and conversions may run completely in background. Multiple trigger events can be prioritized and allow the exact measurement of time critical signals. The result buffering and handling avoids data loss and ensures consistency. Self-test mechanisms can be used for plausibility checks. The basic structure supports a clean software architecture where tasks may only read valid results and do not need to care for starting conversions.

3.7.2 Analog Comparator (ACMP) and Out of Range Comparator (ORC)

The Analog Comparator is used to compare the voltage of two analog inputs and a digital output indicating which input voltage is higher. One of the inputs can either be the internal reference voltage or from external pin. A low power mode is available to help to reduce the total power consumption. A number of out-of-range on-chip comparators serve the purpose of overvoltage monitoring for analog input pins of the VADC.

3.7.3 Temperature Sensor

The Temperature Sensor generates a measurement result that indicates directly the die temperature. It is also capable of generating interrupt requests when the temperature measurement crosses the selectable upper/lower threshold value.

3.8 Fixed function digital

Core components needed for motion and motor control, power conversion and other time based applications.

3.8.1 Capture/Compare Unit 4 (CCU4)

The CCU4 peripheral is a major component for systems that need general purpose timers for signal monitoring/ conditioning and pulse width modulation (PWM) signal generation. Power electronic control systems like switched mode power supplies or uninterruptible power supplies can easily be implemented with the functions inside the CCU4 peripheral. The internal modularity of CCU4 translates into a software friendly system for fast code development and portability between applications.

3.8.2 Capture/Compare Unit 8 (CCU8)

The CCU8 peripheral functions play a major role in applications that need complex PWM signal generation, with complementary high side and low-side switches, multi-phase control, or output parity checking. The CCU8 is optimized for state of the art motor control, multi-phase and multi-level power electronics systems. The internal modularity of CCU8 translates into a software friendly system for fast code development and portability between applications.

3.8.3 Position Interface Unit (POSIF)

The POSIF unit is a flexible and powerful component for motor control systems that use rotary encoders or hall sensors as feedback loop. The configuration schemes of the module target a very large number of motor control application requirements. This enables the build of simple and complex control feedback loops for industrial and automotive motor applications, targeting high performance motion and position monitoring.

3.8.4 Brightness and Color Control Unit (BCCU)

The BCCU is a dimming control peripheral for LED lighting applications that is capable of controlling multiple LED channels. A one-bit sigma-delta bit stream is provided for every channel that determines the brightness. The brightness can be changed gradually along an exponential curve to appear natural to the human eye by using dedicated dimming engines. The module supports color control by adjusting the relative intensity of selected channels using a linear walk scheme for smooth color changes, and it also supports high-power multi-channel LED lamps by optionally “packing” the bitstream to provide a defined ON-time at the output.

3.8.5 Universal Serial Interface Channel (USIC)

The USIC is a flexible interface module covering several serial communication protocols such as ASC, LIN, SSC, I2C, and I2S. A USIC module contains two independent communication channels which can be used in parallel. A FIFO allows transmit and result buffering for relaxing real-time conditions. Multiple chip select signals are available for communication with multiple devices on the same channel.

3.8.6 Controller Area Network Controller (MultiCAN+)

The MultiCAN+ module contains two independently operating CAN nodes with Full-CAN functionality that are able to exchange data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification ISO11898-1. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Both CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

3.9 Event Request Unit (ERU)

PSOC™ Control C1 uses the Event Request Unit (ERU) to support the programmable interconnection for the processing of service requests. There are 2 instances of ERU in PSOC™ Control C1 – ERU0 and ERU1. The ERU supports flexible processing of external and internal service requests, programming for edge and/or level triggering, multiple inputs per channel, triggers combinable from multiple inputs, and input and output gating.

3.10 Coordinate Rotation Digital Computer (CORDIC)

The PSOC™ Control C1 implements CORDIC inside the MATH coprocessor. CORDIC is used to compute transforms required for motor speed/position estimation and reference-frame transforms used in field-oriented control (FOC). It performs trigonometric and related operations in hardware to offload processing from the CPU and improve deterministic control-loop execution.

The CORDIC function supports circular, linear, and hyperbolic operating classes and accelerates algorithm families commonly used in control firmware, including sine/cosine, arctan, and phase- or magnitude-oriented vector operations. The hardware executes up to 27 CORDIC iterations per calculation and provides calculation-complete and error event signaling for firmware handling. CORDIC data paths are controlled through memory-mapped MATH registers, and DIV-to-CORDIC result chaining is supported through the integrated MATH datapath, which also includes signed/unsigned hardware division support.

3.11 General-purpose input/output (GPIO) ports

The PSOC™ Control C1 provides up to 42 package-dependent digital GPIO lines. The pins are organized in logical entities called ports. Each port pin is implemented as a configurable port slice with GPIO control, alternate-function routing to on-chip peripherals, and pad-control configuration.

The GPIO/PORT block has the following features:

- Generic per-pin register interface for GPIO and alternate functions
- Up to nine alternate output paths selectable per pin, with direct peripheral input connectivity
- Push-pull/open-drain driver configuration, pull-up/pull-down, input inverter, and pad hysteresis control
- Digital input disable support on shared analog-capable inputs
- Atomic set/clear/toggle output update through output modification registers
- Hardware-controlled I/O and per-pin Deep Sleep power-save configuration support

GPIO data paths are controlled through memory-mapped PORT registers. After pin and routing configuration, pins can operate as software GPIO or alternate-function peripheral I/O. The pin state remains readable through the input path independent of output configuration.

3.12 Device firmware update (DFU)

Port functions can be overruled by the boot mode selected. The type of boot mode is selected via BMI. Table 1 shows the port pins used for the various boot modes.

Table 1 Port pin for boot modes

Pin	Boot	Boot description
P0.13	CS(O)	SSC BSL mode
P0.14	SWDIO_0	Debug mode (SWD)
	SPD_0	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
	SCLK(O)	SSC BSL mode
P0.15	SWDCLK_0	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
	DATA(I/O)	SSC BSL mode
P1.2	SWDCLK_1	Debug mode (SWD)
	TX	ASC BSL full-duplex mode
	TX	CAN BSL mode
P1.3	SWDIO_1	Debug mode (SWD)
	SPD_1	Debug mode (SPD)
	RX/TX	ASC BSL half-duplex mode
	RX	ASC BSL full-duplex mode
	RX	CAN BSL mode
P4.6	HWCON0	Boot pins
P4.7	HWCON1	(Boot from pins mode must be selected)

3.13 Debug system

The on-chip debug system based on the Arm® Cortex®-M0 debug system provides a broad range of debug and emulation features built into the PSOC™ Control C1. The user software running on the PSOC™ Control C1 can so be debugged within the target system environment.

The Debug unit is controlled by an external debugging tool via the debug interface. The debugger controls the Debug unit via a set of dedicated registers accessible via the debug interface. Additionally, the Debug unit can be controlled by the CPU, for example by a monitor program.

Multiple breakpoints can be triggered by on-chip hardware or by software. Single stepping is supported as well as the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU-halt, a monitor call or a data transfer.

The data transferred at a watchpoint can be obtained via the debug interface for increased performance.

4 Pins

The following general building block is used to describe each pin:

Table 2 Package pin mapping description

Function	Package A	Package B	...	Pad type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad type” indicates the employed pad type:

- STD_INOUT(standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- STD_INOUT/clock (standard bi-directional pads with oscillator function)
- High Current (high-current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical specifications chapter.

Table 3 Package pin mapping

Function	LQFP-48	VQFN-48	VQFN-40	TSSOP-38	Pad type	Notes
VSS	20	17	13	9	Power	Supply GND, ADC reference GND
VDD	21	18	14	10	Power	Supply VDD, ADC reference voltage/ORC reference voltage
VDDP	28	19	15	10	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.
VDDP	-	27	–	–	Power	I/O port supply
VDDP	38	38	32	26	Power	I/O port supply
VSSP	37	37	31	25	Power	I/O port ground
VSSP	-	Exp. Pad	Exp. Pad	–	Power	Exposed die pad. The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, see Package information.
P0.0	30	29	23	17	STD_INOUT	

(table continues...)

Table 3 (continued) Package pin mapping

Function	LQFP-48	VQFN-48	VQFN-40	TSSOP-38	Pad type	Notes
P0.1	31	30	24	18	STD_INOUT	
P0.2	32	31	25	19	STD_INOUT	
P0.3	33	32	26	20	STD_INOUT	
P0.4	34	33	27	21	STD_INOUT	
P0.5	35	34	28	22	STD_INOUT	
P0.6	36	35	29	23	STD_INOUT	
P0.7	-	36	30	24	STD_INOUT	
P0.8/ RTC_ XTAL1	39	39	33	27	STD_INOUT/ clock_IN	
P0.9/ RTC_ XTAL2	40	40	34	28	STD_INOUT/ clock_O	
P0.10/XTAL1	41	41	35	29	STD_INOUT/ clock_IN	
P0.11/XTAL2	42	42	36	30	STD_INOUT/ clock_O	
P0.12	43	43	37	31	STD_INOUT	
P0.13	44	44	38	32	STD_INOUT	
P0.14	45	45	39	33	STD_INOUT	
P0.15	46	46	40	34	STD_INOUT	
P1.0	27	26	22	16	High Current	
P1.1	26	25	21	15	High Current	
P1.2	25	24	20	14	High Current	
P1.3	24	23	19	13	High Current	
P1.4	23	22	18	12	High Current	
P1.5	22	21	17	11	High Current	
P1.6	-	20	16	–	High Current	
P2.0	6	3	1	35	STD_INOUT/ AN	
P2.1	7	4	2	36	STD_INOUT/ AN	
P2.2	8	5	3	37	STD_IN/AN	
P2.3	9	6	4	38	STD_IN/AN	
P2.4	10	7	5	1	STD_IN/AN	

(table continues...)

Table 3 (continued) Package pin mapping

Function	LQFP-48	VQFN-48	VQFN-40	TSSOP-38	Pad type	Notes
P2.5	11	8	6	2	STD_IN/AN	
P2.6	12	9	7	3	STD_IN/AN	
P2.7	13	10	8	4	STD_IN/AN	
P2.8	14	11	9	5	STD_IN/AN	
P2.9	15	12	10	6	STD_IN/AN	
P2.10	16	13	11	7	STD_INOUT/AN	
P2.11	17	14	12	8	STD_INOUT/AN	
P2.12	18	15	–	–	STD_INOUT/AN	
P2.13	19	16	–	–	STD_INOUT/AN	
P3.0	29	28	–	–	STD_INOUT	
P4.1	47	–	–	–	STD_INOUT	
P4.2	48	–	–	–	STD_INOUT	
P4.3	1	–	–	–	STD_INOUT	
P4.4	-	47	–	–	STD_INOUT	
P4.5	-	48	–	–	STD_INOUT	
P4.6	2	1	–	–	STD_INOUT	
P4.7	3	2	–	–	STD_INOUT	
P4.8	4	–	–	–	STD_INOUT	
P4.9	5	–	–	–	STD_INOUT	

The following figures summarize all pins, showing their locations on the different packages.

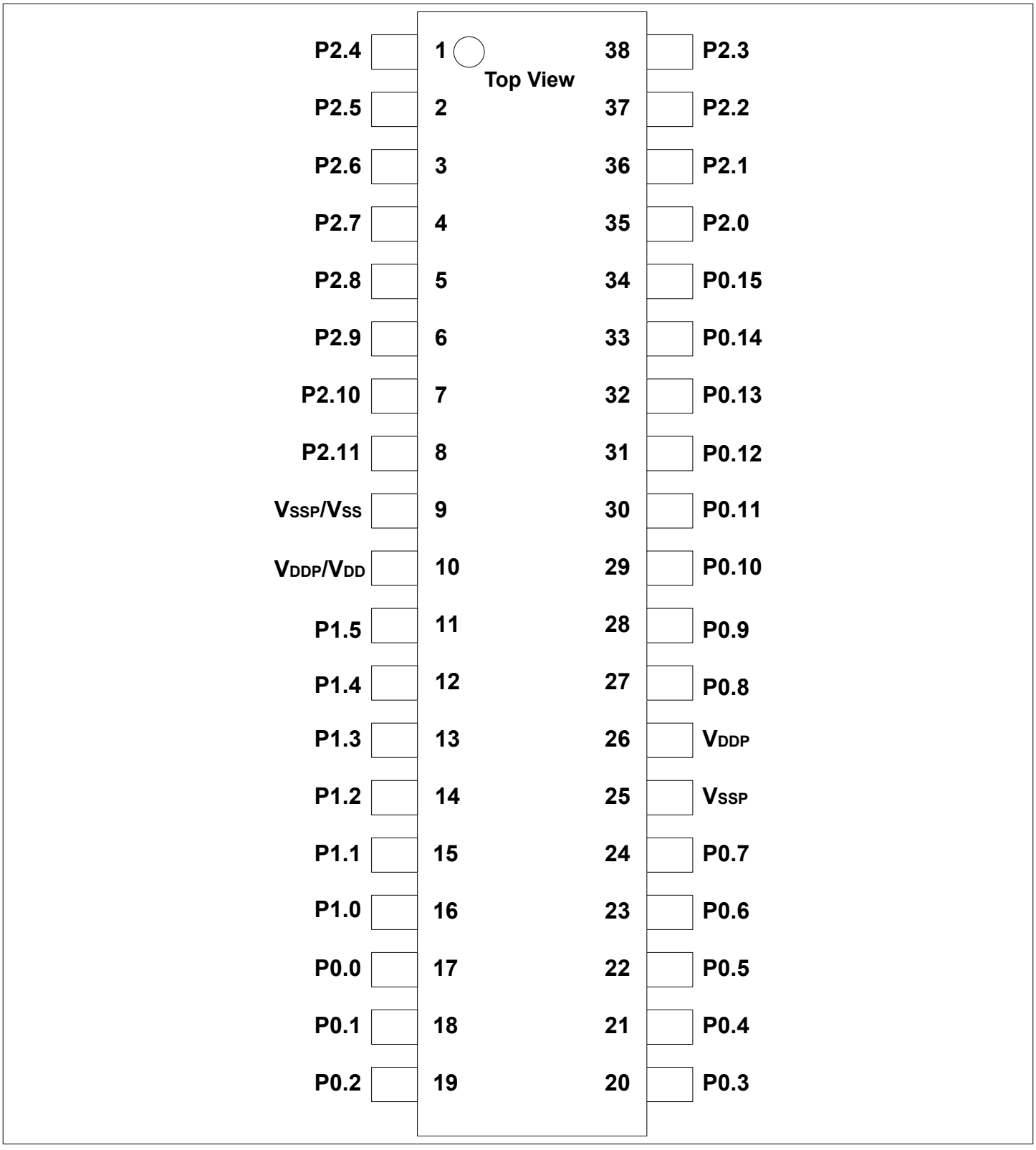


Figure 3 PSC1M2, PSC1M3 PG-TSSOP-38-9 pin configuration (top view)

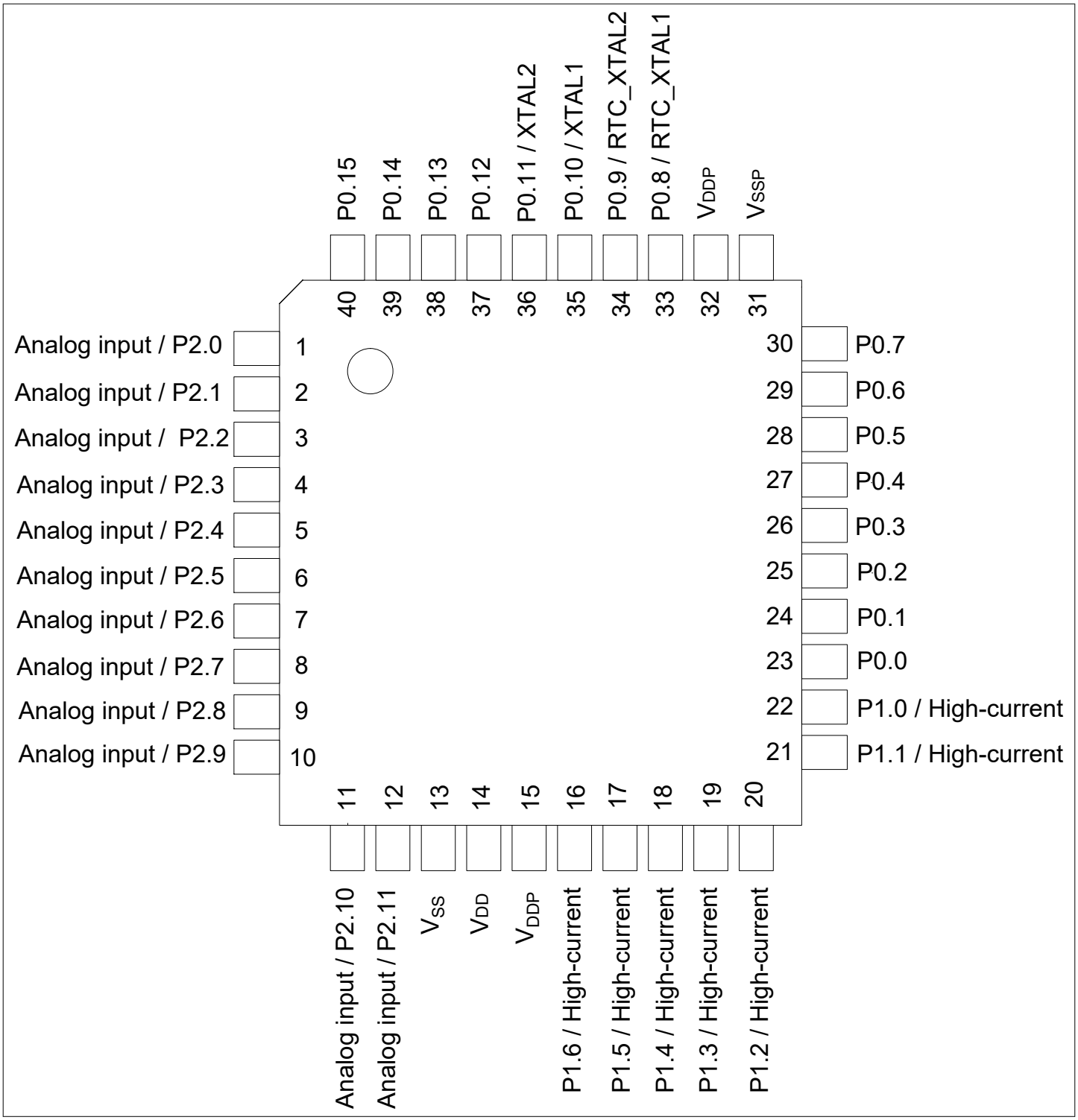


Figure 4 PSC1M2, PSC1M3 PG-VQFN-40-17 pin configuration (top view)

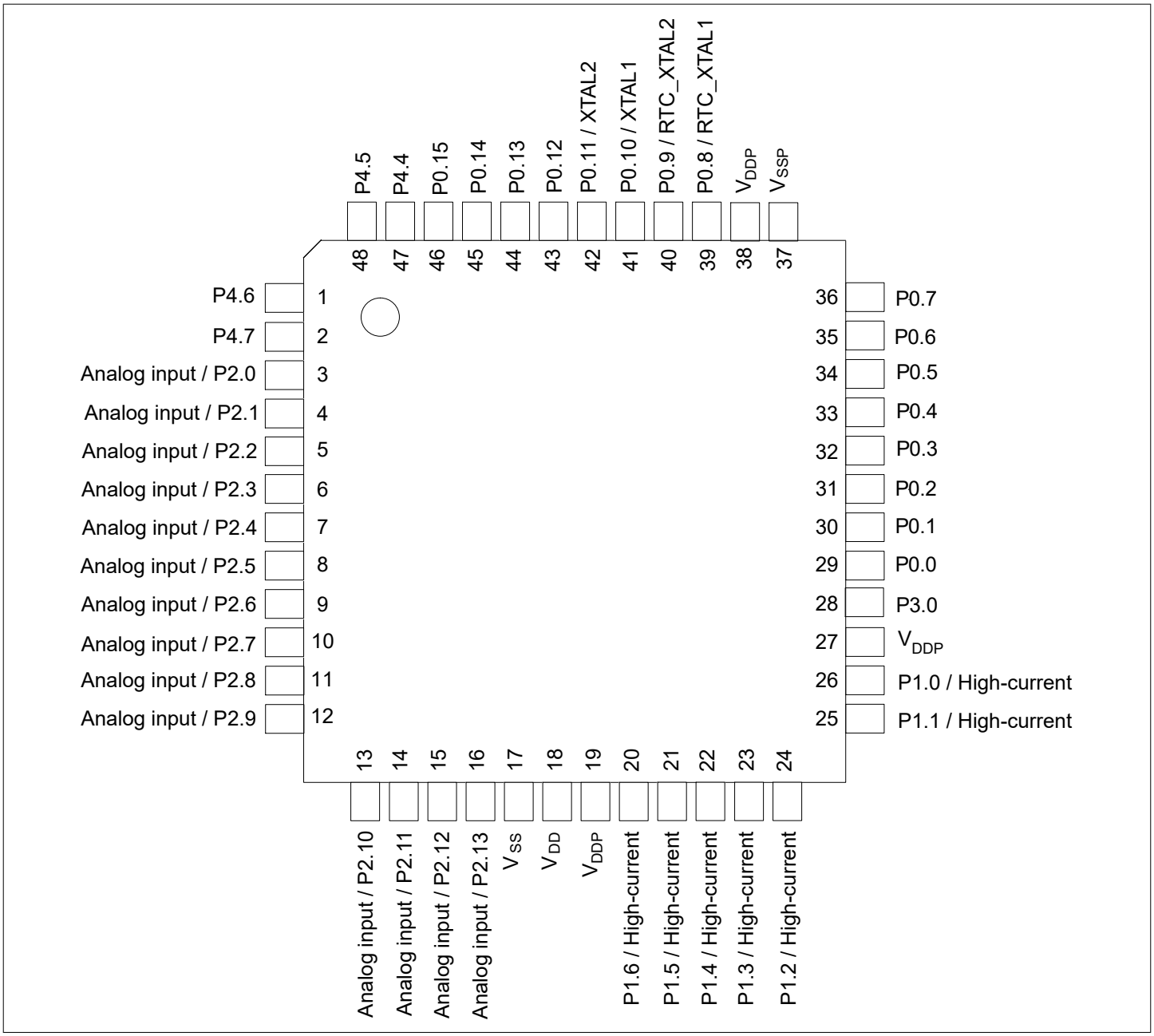


Figure 5 PSC1M2, PSC1M3 PG-VQFN-48-73 pin configuration (top view)

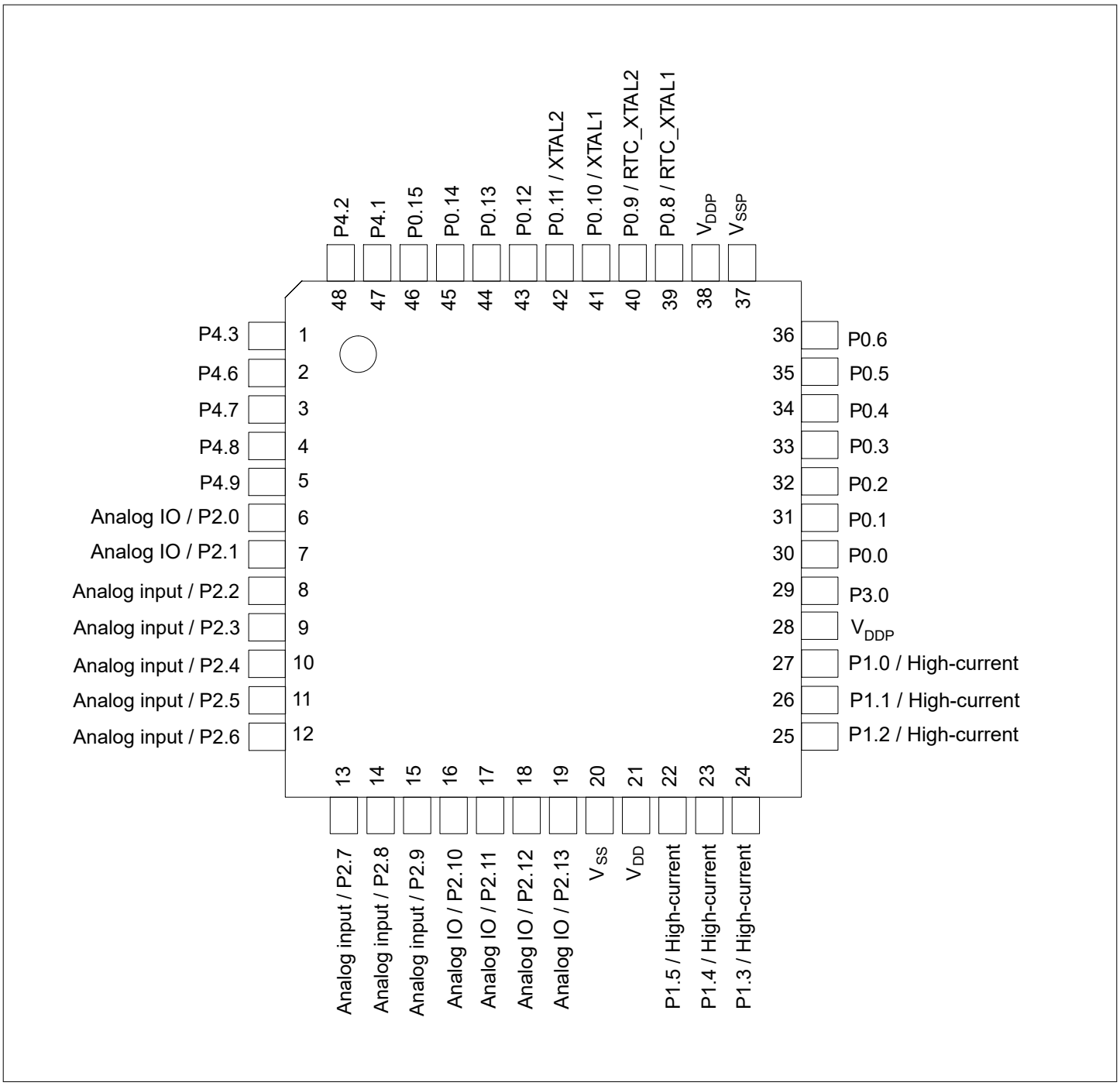


Figure 6 PSC1M2, PSC1M3 PG-LQFP-48-10 pin configuration (top view)

5 GPIO alternate functions tables

Table 4 GPIO alternate functions

GPIO	Alternate functions and I/O routes			
P0.0	ERU0.PDOUT0	ALT1	ERU0.GOUT0	ALT3
	CCU40.OUT0	ALT4	CCU80.OUT00	ALT5
	USIC0_CH0.SELO0	ALT6	USIC0_CH1.SELO0	ALT7
	CCU81.OUT00	ALT8	USIC1_CH1.DOUT0	ALT9
	BCCU0.TRAPINB	Input	CCU40.IN0AC	Input
	USIC1_CH1.DX0A	Input	USIC0_CH0.DX2A	Input
	USIC0_CH1.DX2A	Input		
P0.1	ERU0.PDOUT1	ALT1	ERU0.GOUT1	ALT3
	CCU40.OUT1	ALT4	CCU80.OUT01	ALT5
	BCCU0.OUT8	ALT6	SCU.VDROP	ALT7
	USIC1_CH1.SCLKOUT	ALT8	USIC1_CH1.DOUT0	ALT9
	CCU40.IN1AC	Input	USIC1_CH1.DX0B	Input
	USIC1_CH1.DX1A	Input		
P0.2	ERU0.PDOUT2	ALT1	ERU0.GOUT2	ALT3
	CCU40.OUT2	ALT4	CCU80.OUT02	ALT5
	VADC0.EMUX02	ALT6	CCU80.OUT10	ALT7
	USIC1_CH0.SCLKOUT	ALT8	USIC1_CH0.DOUT0	ALT9
	CCU40.IN2AC	Input	USIC1_CH0.DX0A	Input
	USIC1_CH0.DX1A	Input		
P0.3	ERU0.PDOUT3	ALT1	ERU0.GOUT3	ALT3
	CCU40.OUT3	ALT4	CCU80.OUT03	ALT5
	VADC0.EMUX01	ALT6	CCU80.OUT11	ALT7
	USIC1_CH1.SCLKOUT	ALT8	USIC1_CH0.DOUT0	ALT9
	CCU40.IN3AC	Input	USIC1_CH0.DX0B	Input
P0.4	BCCU0.OUT0	ALT1	CCU40.OUT1	ALT4
	CCU80.OUT13	ALT5	VADC0.EMUX00	ALT6
	WWDT.SERVICE_OUT	ALT7	USIC1_CH1.SELO0	ALT8
	CAN.N0_TXD	ALT9	CCU41.IN0AB	Input
	CCU80.IN0AB	Input	CAN.N0_RXDA	Input
P0.5	BCCU0.OUT1	ALT1	CCU40.OUT0	ALT4
	CCU80.OUT12	ALT5	ACMP2.OUT	ALT6
	CCU80.OUT01	ALT7	VADC0.EMUX10	ALT8

(table continues...)

Table 4 (continued) GPIO alternate functions

	CAN.N0_TXD	ALT9	CCU41.IN1AB	Input
	CCU80.IN1AB	Input	CAN.N0_RXDB	Input
P0.6	BCCU0.OUT2	ALT1	CCU40.OUT0	ALT4
	CCU80.OUT11	ALT5	USIC0_CH1.MCLKOUT	ALT6
	USIC0_CH1.DOUT0	ALT7	VADC0.EMUX11	ALT8
	CCU41.OUT0	ALT9	CCU40.IN0AB	Input
	CCU41.IN2AB	Input	USIC0_CH1.DX0C	Input
P0.7	BCCU0.OUT3	ALT1	CCU40.OUT1	ALT4
	CCU80.OUT10	ALT5	USIC0_CH0.SCLKOUT	ALT6
	USIC0_CH1.DOUT0	ALT7	VADC0.EMUX12	ALT8
	CCU41.OUT1	ALT9	CCU40.IN1AB	Input
	CCU41.IN3AB	Input	USIC0_CH0.DX1C	Input
	USIC0_CH1.DX0D	Input	USIC0_CH1.DX1C	Input
P0.8/RTC_XTAL1	BCCU0.OUT4	ALT1	CCU40.OUT2	ALT4
	CCU80.OUT20	ALT5	USIC0_CH0.SCLKOUT	ALT6
	USIC0_CH1.SCLKOUT	ALT7	CCU81.OUT20	ALT8
	CCU41.OUT2	ALT9	CCU40.IN2AB	Input
	USIC0_CH0.DX1B	Input	USIC0_CH1.DX1B	Input
P0.9/RTC_XTAL2	BCCU0.OUT5	ALT1	CCU40.OUT3	ALT4
	CCU80.OUT21	ALT5	USIC0_CH0.SELO0	ALT6
	USIC0_CH1.SELO0	ALT7	CCU81.OUT21	ALT8
	CCU41.OUT3	ALT9	CCU40.IN3AB	Input
	USIC0_CH0.DX2B	Input	USIC0_CH1.DX2B	Input
P0.10/XTAL1	BCCU0.OUT6	ALT1	ACMP0.OUT	ALT4
	CCU80.OUT22	ALT5	USIC0_CH0.SELO1	ALT6
	USIC0_CH1.SELO1	ALT7	CCU81.OUT22	ALT8
	CCU80.IN2AB	Input	CCU81.IN2AB	Input
	USIC0_CH0.DX2C	Input	USIC0_CH1.DX2C	Input
P0.11/XTAL2	BCCU0.OUT7	ALT1	USIC0_CH0.MCLKOUT	ALT4
	CCU80.OUT23	ALT5	USIC0_CH0.SELO2	ALT6
	USIC0_CH1.SELO2	ALT7	CCU81.OUT23	ALT8
	USIC0_CH0.DX2D	Input	USIC0_CH1.DX2D	Input
P0.12	BCCU0.OUT6	ALT1	CCU80.OUT33	ALT5
	USIC0_CH0.SELO3	ALT6	CCU80.OUT20	ALT7

(table continues...)

Table 4 (continued) GPIO alternate functions

	CAN.N1_TXD	ALT9	BCCU0.TRAPINA	Input
	CCU40.IN0AA	Input	CCU40.IN1AA	Input
	CCU40.IN2AA	Input	CCU81.IN0AU	Input
	CCU40.IN3AA	Input	CCU80.IN0AA	Input
	USIC0_CH0.DX2E	Input	CCU80.IN1AA	Input
	CCU80.IN2AA	Input	CAN.N1_RXDA	Input
	CCU80.IN3AA	Input		
P0.13	WWDT.SERVICE_OUT	ALT1	CCU80.OUT32	ALT5
	USIC0_CH0.SELO4	ALT6	CCU80.OUT21	ALT7
	CAN.N1_TXD	ALT9	CCU80.IN3AB	Input
	CCU81.IN1AU	Input	POSIF0.IN0B	Input
	USIC0_CH0.DX2F	Input	CAN.N1_RXDB	Input
P0.14	BCCU0.OUT7	ALT1	CCU80.OUT31	ALT5
	USIC0_CH0.DOUT0	ALT6	USIC0_CH0.SCLKOUT	ALT7
	CAN.N0_TXD	ALT9	CCU81.IN2AU	Input
	POSIF0.IN1B	Input	USIC0_CH0.DX0A	Input
	USIC0_CH0.DX1A	Input	USIC1_CH1.DX5B	Input
	CAN.N0_RXDC	Input		
P0.15	BCCU0.OUT8	ALT1	CCU80.OUT30	ALT5
	USIC0_CH0.DOUT0	ALT6	USIC0_CH1.MCLKOUT	ALT7
	CAN.N0_TXD	ALT9	CCU81.IN3AU	Input
	POSIF0.IN2B	Input	USIC0_CH0.DX0B	Input
	USIC1_CH1.DX3B	Input	USIC1_CH1.DX4B	Input
	CAN.N0_RXDD	Input		
P1.0	BCCU0.OUT0	ALT1	CCU40.OUT0	ALT2
	CCU80.OUT00	ALT5	ACMP1.OUT	ALT6
	USIC0_CH0.DOUT0	ALT7	CCU81.OUT00	ALT8
	CAN.N0_TXD	ALT9	POSIF0.IN2A	Input
	USIC0_CH0.DX0C	Input	CAN.N0_RXDG	Input
P1.1	ERU1.PDOUT1	ALT1	CCU40.OUT1	ALT2
	CCU80.OUT01	ALT5	USIC0_CH0.DOUT0	ALT6
	USIC0_CH1.SELO0	ALT7	CCU81.OUT01	ALT8
	CAN.N0_TXD	ALT9	POSIF0.IN1A	Input
	USIC0_CH0.DX0D	Input	USIC0_CH0.DX1D	Input

(table continues...)

Table 4 (continued) GPIO alternate functions

	USIC0_CH1.DX2E	Input	CAN.N0_RXDH	Input
P1.2	ERU1.PDOUT2	ALT1	CCU40.OUT2	ALT2
	CCU80.OUT10	ALT5	ACMP2.OUT	ALT6
	USIC0_CH1.DOUT0	ALT7	CCU81.OUT10	ALT8
	CAN.N1_TXD	ALT9	POSIF0.IN0A	Input
	USIC0_CH1.DX0B	Input	CAN.N1_RXDG	Input
P1.3	ERU1.PDOUT3	ALT1	CCU40.OUT3	ALT2
	CCU80.OUT11	ALT5	USIC0_CH1.SCLKOUT	ALT6
	USIC0_CH1.DOUT0	ALT7	CCU81.OUT11	ALT8
	CAN.N1_TXD	ALT9	USIC0_CH1.DX0A	Input
	USIC0_CH1.DX1A	Input	CAN.N1_RXDH	Input
P1.4	ERU1.PDOUT0	ALT1	USIC0_CH1.SCLKOUT	ALT2
	CCU80.OUT20	ALT5	USIC0_CH0.SELO0	ALT6
	USIC0_CH1.SELO1	ALT7	CCU81.OUT20	ALT8
	CCU41.OUT0	ALT9	USIC0_CH0.DX5E	Input
	USIC0_CH1.DX5E	Input		
P1.5	ERU1.PDOUT1	ALT1	USIC0_CH0.DOUT0	ALT2
	BCCU0.OUT1	ALT4	CCU80.OUT21	ALT5
	USIC0_CH0.SELO1	ALT6	USIC0_CH1.SELO2	ALT7
	CCU81.OUT21	ALT8	CCU41.OUT1	ALT9
	USIC0_CH1.DX5F	Input		
P1.6	ERU1.PDOUT2	ALT1	USIC0_CH1.DOUT0	ALT2
	USIC0_CH0.SCLKOUT	ALT4	BCCU0.OUT2	ALT5
	USIC0_CH0.SELO2	ALT6	USIC0_CH1.SELO3	ALT7
	CCU81.OUT30	ALT8	CCU41.OUT2	ALT9
	POSIF1.IN2A	Input	USIC0_CH0.DX5F	Input
P2.0	ERU0.PDOUT3	ALT1	CCU40.OUT0	ALT2
	ERU0.GOUT3	ALT3	CCU80.OUT20	ALT5
	USIC0_CH0.DOUT0	ALT6	USIC0_CH0.SCLKOUT	ALT7
	CCU81.OUT20	ALT8	CAN.N0_TXD	ALT9
	VADC0.G0CH5	Input	USIC0_CH0.DX0E	Input
	USIC0_CH0.DX1E	Input	USIC0_CH1.DX2F	Input
	CAN.N0_RXDE	Input	ERU0.0B0	Input
P2.1	ERU0.PDOUT2	ALT1	CCU40.OUT1	ALT2

(table continues...)

Table 4 (continued) GPIO alternate functions

	ERU0.GOUT2	ALT3	CCU80.OUT21	ALT5
	USIC0_CH0.DOUT0	ALT6	USIC0_CH1.SCLKOUT	ALT7
	CCU81.OUT21	ALT8	CAN.N0_TXD	ALT9
	ACMP2.INP	Input	VADC0.G0CH6	Input
	USIC0_CH0.DX0F	Input	USIC0_CH1.DX3A	Input
	USIC0_CH1.DX4A	Input	CAN.N0_RXDF	Input
	ERU0.1B0	Input		
P2.2	ACMP2.INN	Input	VADC0.G0CH7	Input
	ORC0.AIN	Input	USIC1_CH0.DX5E	Input
	USIC0_CH0.DX3A	Input	USIC0_CH0.DX4A	Input
	USIC0_CH1.DX5A	Input	ERU0.0B1	Input
P2.3	VADC0.G1CH5	Input	ORC1.AIN	Input
	USIC1_CH0.DX3E	Input	USIC1_CH0.DX4E	Input
	USIC1_CH1.DX5C	Input	USIC0_CH0.DX5B	Input
	USIC0_CH1.DX3C	Input	USIC0_CH1.DX4C	Input
	ERU0.1B1	Input		
P2.4	VADC0.G1CH6	Input	ORC2.AIN	Input
	USIC1_CH1.DX3C	Input	USIC1_CH1.DX4C	Input
	USIC0_CH0.DX3B	Input	USIC0_CH0.DX4B	Input
	USIC1_CH0.DX5F	Input	USIC0_CH1.DX5B	Input
	ERU0.0A1	Input		
P2.5	VADC0.G1CH7	Input	ORC3.AIN	Input
	USIC1_CH1.DX5D	Input	USIC0_CH0.DX5D	Input
	USIC0_CH1.DX3E	Input	USIC0_CH1.DX4E	Input
	ERU0.1A1	Input		
P2.6	ACMP1.INN	Input	VADC0.G0CH0	Input
	ORC4.AIN	Input	USIC1_CH1.DX3E	Input
	USIC1_CH1.DX4E	Input	USIC0_CH0.DX3E	Input
	USIC0_CH0.DX4E	Input	USIC0_CH1.DX5D	Input
	ERU0.2A1	Input		
P2.7	ACMP1.INP	Input	VADC0.G1CH1	Input
	ORC5.AIN	Input	USIC1_CH1.DX5E	Input
	USIC0_CH0.DX5C	Input	USIC0_CH1.DX3D	Input
	USIC0_CH1.DX4D	Input	ERU0.3A1	Input

(table continues...)

Table 4 (continued) GPIO alternate functions

P2.8	ACMP0.INN	Input	VADC0.G0CH1	Input
	VADC0.G1CH0	Input	ORC6.AIN	Input
	USIC0_CH0.DX3D	Input	USIC0_CH0.DX4D	Input
	USIC0_CH1.DX5C	Input	ERU0.3B1	Input
P2.9	ACMP0.INP	Input	VADC0.G0CH2	Input
	VADC0.G1CH4	Input	ORC7.AIN	Input
	USIC0_CH0.DX5A	Input	USIC0_CH1.DX3B	Input
	USIC0_CH1.DX4B	Input	ERU0.3B0	Input
P2.10	ERU0.PDOUT1	ALT1	CCU40.OUT2	ALT2
	ERU0.GOUT1	ALT3	CCU80.OUT30	ALT5
	ACMP0.OUT	ALT6	USIC0_CH1.DOUT0	ALT7
	CAN.N1_TXD	ALT9	VADC0.G0CH3	Input
	VADC0.G1CH2	Input	USIC0_CH0.DX3C	Input
	USIC0_CH0.DX4C	Input	USIC0_CH1.DX0F	Input
	CAN.N1_RXDE	Input	ERU0.2B0	Input
P2.11	ERU0.PDOUT0	ALT1	CCU40.OUT3	ALT2
	ERU0.GOUT0	ALT3	CCU80.OUT31	ALT5
	USIC0_CH1.SCLKOUT	ALT6	USIC0_CH1.DOUT0	ALT7
	CAN.N1_TXD	ALT9	ACMP.REF	Input
	VADC0.G0CH4	Input	VADC0.G1CH3	Input
	USIC0_CH1.DX0E	Input	USIC0_CH1.DX1E	Input
	CAN.N1_RXDF	Input	ERU0.2B1	Input
P2.12	BCCU0.OUT3	ALT1	VADC0.EMUX00	ALT2
	USIC1_CH0.SCLKOUT	ALT3	USIC1_CH1.SCLKOUT	ALT4
	ACMP2.OUT	ALT6	USIC1_CH1.DOUT0	ALT7
	ACMP3.INN	Input	USIC1_CH0.DX3A	Input
	USIC1_CH0.DX4A	Input	USIC1_CH1.DX0C	Input
	USIC1_CH1.DX1B	Input	ERU1.3A2	Input
P2.13	BCCU0.OUT4	ALT1	CCU40.OUT3	ALT2
	USIC1_CH0.MCLKOUT	ALT3	CCU81.OUT31	ALT4
	VADC0.EMUX01	ALT6	USIC1_CH1.DOUT0	ALT7
	CCU81.OUT33	ALT8	CCU41.OUT3	ALT9
	ACMP3.INP	Input	USIC1_CH0.DX5A	Input
	USIC1_CH1.DX0D	Input	ERU1.3A3	Input

(table continues...)

Table 4 (continued) GPIO alternate functions

P3.0	BCCU0.OUT0	ALT1	USIC1_CH1.DOUT0	ALT2
	USIC1_CH1.SCLKOUT	ALT3	CCU80.OUT21	ALT5
	ACMP1.OUT	ALT6	USIC1_CH0.SELO1	ALT7
	CCU81.OUT21	ALT8	CCU41.OUT0	ALT9
	BCCU0.TRAPINC	Input	CCU41.IN0AA	Input
	CCU41.IN1AA	Input	CCU41.IN2AA	Input
	CCU41.IN3AA	Input	CCU81.IN0AA	Input
	CCU81.IN1AA	Input	CCU81.IN2AA	Input
	USIC1_CH1.DX0E	Input	USIC1_CH1.DX1D	Input
	CCU81.IN3AA	Input	ERU1.0A1	Input
P4.1	BCCU0.OUT8	ALT1	ERU1.PDOUT1	ALT2
	ERU1.GOUT1	ALT4	CCU40.OUT1	ALT5
	ACMP3.OUT	ALT6	USIC1_CH1.SELO2	ALT7
	CCU81.OUT11	ALT8	CCU41.OUT1	ALT9
	CCU40.IN1BA	Input	CCU41.IN1AC	Input
	CCU80.IN1AU	Input	POSIF1.IN0B	Input
	USIC1_CH0.DX5C	Input		
P4.2	BCCU0.OUT4	ALT1	ERU1.PDOUT2	ALT2
	CCU81.OUT20	ALT3	ERU1.GOUT2	ALT4
	CCU40.OUT2	ALT5	ACMP2.OUT	ALT6
	USIC1_CH1.SELO3	ALT7	CCU81.OUT12	ALT8
	CCU41.OUT2	ALT9	CCU40.IN2BA	Input
	CCU41.IN2AC	Input	CCU80.IN2AU	Input
	CCU81.IN1AB	Input	POSIF1.IN1B	Input
	USIC1_CH0.DX5D	Input		
P4.3	BCCU0.OUT5	ALT1	ERU1.PDOUT3	ALT2
	CCU81.OUT21	ALT3	ERU1.GOUT3	ALT4
	CCU40.OUT3	ALT5	ACMP0.OUT	ALT6
	USIC1_CH0.SCLKOUT	ALT7	CCU81.OUT13	ALT8
	CCU41.OUT3	ALT9	CCU40.IN3BA	Input
	CCU41.IN3AC	Input	CCU80.IN3AU	Input
	POSIF1.IN2B	Input	USIC1_CH0.DX1B	Input
P4.4	BCCU0.OUT0	ALT1	CCU80.OUT00	ALT5
	USIC1_CH0.DOUT0	ALT6	CCU81.OUT00	ALT8

(table continues...)

Table 4 (continued) GPIO alternate functions

	CCU41.OUT0	ALT9	CCU41.IN0AV	Input
	USIC1_CH0.DX0C	Input	USIC1_CH1.DX5F	Input
	ERU1.0A2	Input		
P4.5	BCCU0.OUT8	ALT1	CCU80.OUT01	ALT5
	USIC1_CH0.DOUT0	ALT6	USIC1_CH0.SCLKOUT	ALT7
	CCU81.OUT01	ALT8	CCU41.OUT1	ALT9
	CCU41.IN1AV	Input	USIC1_CH0.DX0D	Input
	USIC1_CH0.DX1C	Input	ERU1.1A2	Input
P4.6	BCCU0.OUT2	ALT1	CCU81.OUT10	ALT3
	CCU80.OUT10	ALT5	USIC1_CH0.SCLKOUT	ALT7
	CCU81.OUT02	ALT8	CCU41.OUT2	ALT9
	CCU41.IN2AV	Input	CCU81.IN0AB	Input
	USIC1_CH0.DX1D	Input	ERU1.2A2	Input
P4.7	BCCU0.OUT5	ALT1	CCU81.OUT11	ALT3
	CCU80.OUT11	ALT5	USIC1_CH0.SELO0	ALT7
	CCU81.OUT03	ALT8	CCU41.OUT3	ALT9
	CCU41.IN3AV	Input	USIC1_CH0.DX2A	Input
	ERU1.0A3	Input		
P4.8	BCCU0.OUT7	ALT1	CCU80.OUT30	ALT5
	CCU40.OUT0	ALT6	USIC1_CH0.SELO1	ALT7
	CCU81.OUT30	ALT8	CAN.N1_TXD	ALT9
	CCU40.IN0AV	Input	CCU41.IN0BA	Input
	USIC1_CH0.DX2B	Input	CAN.N1_RXDC	Input
P4.9	BCCU0.OUT3	ALT1	CCU80.OUT31	ALT5
	CCU40.OUT1	ALT6	USIC1_CH0.SELO2	ALT7
	CCU81.OUT31	ALT8	CAN.N1_TXD	ALT9
	CCU40.IN1AV	Input	CCU41.IN1BA	Input
	USIC1_CH0.DX2C	Input	CAN.N1_RXDD	Input

Table 5 GPIO alternate functions

Function	GPIO	Function	GPIO	Function	GPIO
ACMP.REF	P2.11	ACMP0.INN	P2.8	ACMP0.INP	P2.9
ACMP0.OUT	P0.10/XTAL1, P2.10, P4.3	ACMP1.INN	P2.6	ACMP1.INP	P2.7
ACMP1.OUT	P1.0, P3.0	ACMP2.INN	P2.2	ACMP2.INP	P2.1

(table continues...)

Table 5 (continued) GPIO alternate functions

ACMP2.OUT	P0.5, P1.2, P2.12, P4.2	ACMP3.INN	P2.12	ACMP3.INP	P2.13
ACMP3.OUT	P4.1	BCCU0.OUT0	P0.4, P1.0, P3.0, P4.4	BCCU0.OUT1	P0.5, P1.5
BCCU0.OUT2	P0.6, P1.6, P4.6	BCCU0.OUT3	P0.7, P2.12, P4.9	BCCU0.OUT4	P0.8/RTC_XTAL1, P2.13, P4.2
BCCU0.OUT5	P0.9/RTC_XTAL2, P4.3, P4.7	BCCU0.OUT6	P0.10/XTAL1, P0.12	BCCU0.OUT7	P0.11/XTAL2, P0.14, P4.8
BCCU0.OUT8	P0.1, P0.15, P4.1, P4.5	BCCU0.TRAPINA	P0.12	BCCU0.TRAPINB	P0.0
BCCU0.TRAPINC	P3.0	CAN.N0_RXDA	P0.4	CAN.N0_RXDB	P0.5
CAN.N0_RXDC	P0.14	CAN.N0_RXDD	P0.15	CAN.N0_RXDE	P2.0
CAN.N0_RXDF	P2.1	CAN.N0_RXDG	P1.0	CAN.N0_RXDH	P1.1
CAN.N0_TXD	P0.4, P0.5, P0.14, P0.15, P1.0, P1.1, P2.0, P2.1	CAN.N1_RXDA	P0.12	CAN.N1_RXDB	P0.13
CAN.N1_RXDC	P4.8	CAN.N1_RXDD	P4.9	CAN.N1_RXDE	P2.10
CAN.N1_RXDF	P2.11	CAN.N1_RXDG	P1.2	CAN.N1_RXDH	P1.3
CAN.N1_TXD	P0.12, P0.13, P1.2, P1.3, P2.10, P2.11, P4.8, P4.9	CCU40.IN0AA	P0.12	CCU40.IN0AB	P0.6
CCU40.IN0AC	P0.0	CCU40.IN0AV	P4.8	CCU40.IN1AA	P0.12
CCU40.IN1AB	P0.7	CCU40.IN1AC	P0.1	CCU40.IN1AV	P4.9
CCU40.IN1BA	P4.1	CCU40.IN2AA	P0.12	CCU40.IN2AB	P0.8/RTC_XTAL1
CCU40.IN2AC	P0.2	CCU40.IN2BA	P4.2	CCU40.IN3AA	P0.12
CCU40.IN3AB	P0.9/RTC_XTAL2	CCU40.IN3AC	P0.3	CCU40.IN3BA	P4.3
CCU40.OUT0	P0.0, P0.5, P0.6, P1.0, P2.0, P4.8	CCU40.OUT1	P0.1, P0.4, P0.7, P1.1, P2.1, P4.1, P4.9	CCU40.OUT2	P0.2, P0.8/ RTC_XTAL1, P1.2, P2.10, P4.2
CCU40.OUT3	P0.3, P0.9/ RTC_XTAL2, P1.3, P2.11, P2.13, P4.3	CCU41.IN0AA	P3.0	CCU41.IN0AB	P0.4
CCU41.IN0AV	P4.4	CCU41.IN0BA	P4.8	CCU41.IN1AA	P3.0
CCU41.IN1AB	P0.5	CCU41.IN1AC	P4.1	CCU41.IN1AV	P4.5
CCU41.IN1BA	P4.9	CCU41.IN2AA	P3.0	CCU41.IN2AB	P0.6
CCU41.IN2AC	P4.2	CCU41.IN2AV	P4.6	CCU41.IN3AA	P3.0
CCU41.IN3AB	P0.7	CCU41.IN3AC	P4.3	CCU41.IN3AV	P4.7
CCU41.OUT0	P0.6, P1.4, P3.0, P4.4	CCU41.OUT1	P0.7, P1.5, P4.1, P4.5	CCU41.OUT2	P0.8/RTC_XTAL1, P1.6, P4.2, P4.6

(table continues...)

Table 5 (continued) GPIO alternate functions

CCU41.OUT3	P0.9/RTC_XTAL2, P2.13, P4.3, P4.7	CCU80.IN0AA	P0.12	CCU80.IN0AB	P0.4
CCU80.IN1AA	P0.12	CCU80.IN1AB	P0.5	CCU80.IN1AU	P4.1
CCU80.IN2AA	P0.12	CCU80.IN2AB	P0.10/XTAL1	CCU80.IN2AU	P4.2
CCU80.IN3AA	P0.12	CCU80.IN3AB	P0.13	CCU80.IN3AU	P4.3
CCU80.OUT00	P0.0, P1.0, P4.4	CCU80.OUT01	P0.1, P0.5, P1.1, P4.5	CCU80.OUT02	P0.2
CCU80.OUT03	P0.3	CCU80.OUT10	P0.2, P0.7, P1.2, P4.6	CCU80.OUT11	P0.3, P0.6, P1.3, P4.7
CCU80.OUT12	P0.5	CCU80.OUT13	P0.4	CCU80.OUT20	P0.8/RTC_XTAL1, P0.12, P1.4, P2.0
CCU80.OUT21	P0.9/RTC_XTAL2, P0.13, P1.5, P2.1, P3.0	CCU80.OUT22	P0.10/XTAL1	CCU80.OUT23	P0.11/XTAL2
CCU80.OUT30	P0.15, P2.10, P4.8	CCU80.OUT31	P0.14, P2.11, P4.9	CCU80.OUT32	P0.13
CCU80.OUT33	P0.12	CCU81.IN0AA	P3.0	CCU81.IN0AB	P4.6
CCU81.IN0AU	P0.12	CCU81.IN1AA	P3.0	CCU81.IN1AB	P4.2
CCU81.IN1AU	P0.13	CCU81.IN2AA	P3.0	CCU81.IN2AB	P0.10/XTAL1
CCU81.IN2AU	P0.14	CCU81.IN3AA	P3.0	CCU81.IN3AU	P0.15
CCU81.OUT00	P0.0, P1.0, P4.4	CCU81.OUT01	P1.1, P4.5	CCU81.OUT02	P4.6
CCU81.OUT03	P4.7	CCU81.OUT10	P1.2, P4.6	CCU81.OUT11	P1.3, P4.1, P4.7
CCU81.OUT12	P4.2	CCU81.OUT13	P4.3	CCU81.OUT20	P0.8/RTC_XTAL1, P1.4, P2.0, P4.2
CCU81.OUT21	P0.9/RTC_XTAL2, P1.5, P2.1, P3.0, P4.3	CCU81.OUT22	P0.10/XTAL1	CCU81.OUT23	P0.11/XTAL2
CCU81.OUT30	P1.6, P4.8	CCU81.OUT31	P2.13, P4.9	CCU81.OUT33	P2.13
ERU0.0A1	P2.4	ERU0.0B0	P2.0	ERU0.0B1	P2.2
ERU0.1A1	P2.5	ERU0.1B0	P2.1	ERU0.1B1	P2.3
ERU0.2A1	P2.6	ERU0.2B0	P2.10	ERU0.2B1	P2.11
ERU0.3A1	P2.7	ERU0.3B0	P2.9	ERU0.3B1	P2.8
ERU0.GOUT0	P0.0, P2.11	ERU0.GOUT1	P0.1, P2.10	ERU0.GOUT2	P0.2, P2.1
ERU0.GOUT3	P0.3, P2.0	ERU0.PDOUT0	P0.0, P2.11	ERU0.PDOUT1	P0.1, P2.10
ERU0.PDOUT2	P0.2, P2.1	ERU0.PDOUT3	P0.3, P2.0	ERU1.0A1	P3.0
ERU1.0A2	P4.4	ERU1.0A3	P4.7	ERU1.1A2	P4.5
ERU1.2A2	P4.6	ERU1.3A2	P2.12	ERU1.3A3	P2.13
ERU1.GOUT1	P4.1	ERU1.GOUT2	P4.2	ERU1.GOUT3	P4.3

(table continues...)

Table 5 (continued) GPIO alternate functions

ERU1.PDOUT0	P1.4	ERU1.PDOUT1	P1.1, P1.5, P4.1	ERU1.PDOUT2	P1.2, P1.6, P4.2
ERU1.PDOUT3	P1.3, P4.3	ORC0.AIN	P2.2	ORC1.AIN	P2.3
ORC2.AIN	P2.4	ORC3.AIN	P2.5	ORC4.AIN	P2.6
ORC5.AIN	P2.7	ORC6.AIN	P2.8	ORC7.AIN	P2.9
POSIF0.IN0A	P1.2	POSIF0.IN0B	P0.13	POSIF0.IN1A	P1.1
POSIF0.IN1B	P0.14	POSIF0.IN2A	P1.0	POSIF0.IN2B	P0.15
POSIF1.IN0B	P4.1	POSIF1.IN1B	P4.2	POSIF1.IN2A	P1.6
POSIF1.IN2B	P4.3	SCU.VDROP	P0.1	USIC0_CH0.DOUT0	P0.14, P0.15, P1.0, P1.1, P1.5, P2.0, P2.1
USIC0_CH0.DX0A	P0.14	USIC0_CH0.DX0B	P0.15	USIC0_CH0.DX0C	P1.0
USIC0_CH0.DX0D	P1.1	USIC0_CH0.DX0E	P2.0	USIC0_CH0.DX0F	P2.1
USIC0_CH0.DX1A	P0.14	USIC0_CH0.DX1B	P0.8/RTC_XTAL1	USIC0_CH0.DX1C	P0.7
USIC0_CH0.DX1D	P1.1	USIC0_CH0.DX1E	P2.0	USIC0_CH0.DX2A	P0.0
USIC0_CH0.DX2B	P0.9/RTC_XTAL2	USIC0_CH0.DX2C	P0.10/XTAL1	USIC0_CH0.DX2D	P0.11/XTAL2
USIC0_CH0.DX2E	P0.12	USIC0_CH0.DX2F	P0.13	USIC0_CH0.DX3A	P2.2
USIC0_CH0.DX3B	P2.4	USIC0_CH0.DX3C	P2.10	USIC0_CH0.DX3D	P2.8
USIC0_CH0.DX3E	P2.6	USIC0_CH0.DX4A	P2.2	USIC0_CH0.DX4B	P2.4
USIC0_CH0.DX4C	P2.10	USIC0_CH0.DX4D	P2.8	USIC0_CH0.DX4E	P2.6
USIC0_CH0.DX5A	P2.9	USIC0_CH0.DX5B	P2.3	USIC0_CH0.DX5C	P2.7
USIC0_CH0.DX5D	P2.5	USIC0_CH0.DX5E	P1.4	USIC0_CH0.DX5F	P1.6
USIC0_CH0.MCLKOUT	P0.11/XTAL2	USIC0_CH0.SCLKOUT	P0.7, P0.8/RTC_XTAL1, P0.14, P1.6, P2.0	USIC0_CH0.SELO0	P0.0, P0.9/RTC_XTAL2, P1.4
USIC0_CH0.SELO1	P0.10/XTAL1, P1.5	USIC0_CH0.SELO2	P0.11/XTAL2, P1.6	USIC0_CH0.SELO3	P0.12
USIC0_CH0.SELO4	P0.13	USIC0_CH1.DOUT0	P0.6, P0.7, P1.2, P1.3, P1.6, P2.10, P2.11	USIC0_CH1.DX0A	P1.3
USIC0_CH1.DX0B	P1.2	USIC0_CH1.DX0C	P0.6	USIC0_CH1.DX0D	P0.7
USIC0_CH1.DX0E	P2.11	USIC0_CH1.DX0F	P2.10	USIC0_CH1.DX1A	P1.3
USIC0_CH1.DX1B	P0.8/RTC_XTAL1	USIC0_CH1.DX1C	P0.7	USIC0_CH1.DX1E	P2.11
USIC0_CH1.DX2A	P0.0	USIC0_CH1.DX2B	P0.9/RTC_XTAL2	USIC0_CH1.DX2C	P0.10/XTAL1
USIC0_CH1.DX2D	P0.11/XTAL2	USIC0_CH1.DX2E	P1.1	USIC0_CH1.DX2F	P2.0
USIC0_CH1.DX3A	P2.1	USIC0_CH1.DX3B	P2.9	USIC0_CH1.DX3C	P2.3
USIC0_CH1.DX3D	P2.7	USIC0_CH1.DX3E	P2.5	USIC0_CH1.DX4A	P2.1
USIC0_CH1.DX4B	P2.9	USIC0_CH1.DX4C	P2.3	USIC0_CH1.DX4D	P2.7

(table continues...)

Table 5 (continued) GPIO alternate functions

USIC0_CH1.DX4E	P2.5	USIC0_CH1.DX5A	P2.2	USIC0_CH1.DX5B	P2.4
USIC0_CH1.DX5C	P2.8	USIC0_CH1.DX5D	P2.6	USIC0_CH1.DX5E	P1.4
USIC0_CH1.DX5F	P1.5	USIC0_CH1.MCLKOUT	P0.6, P0.15	USIC0_CH1.SCLKOUT	P0.8/RTC_XTAL1, P1.3, P1.4, P2.1, P2.11
USIC0_CH1.SELO0	P0.0, P0.9/RTC_XTAL2, P1.1	USIC0_CH1.SELO1	P0.10/XTAL1, P1.4	USIC0_CH1.SELO2	P0.11/XTAL2, P1.5
USIC0_CH1.SELO3	P1.6	USIC1_CH0.DOUT0	P0.2, P0.3, P4.4, P4.5	USIC1_CH0.DX0A	P0.2
USIC1_CH0.DX0B	P0.3	USIC1_CH0.DX0C	P4.4	USIC1_CH0.DX0D	P4.5
USIC1_CH0.DX1A	P0.2	USIC1_CH0.DX1B	P4.3	USIC1_CH0.DX1C	P4.5
USIC1_CH0.DX1D	P4.6	USIC1_CH0.DX2A	P4.7	USIC1_CH0.DX2B	P4.8
USIC1_CH0.DX2C	P4.9	USIC1_CH0.DX3A	P2.12	USIC1_CH0.DX3E	P2.3
USIC1_CH0.DX4A	P2.12	USIC1_CH0.DX4E	P2.3	USIC1_CH0.DX5A	P2.13
USIC1_CH0.DX5C	P4.1	USIC1_CH0.DX5D	P4.2	USIC1_CH0.DX5E	P2.2
USIC1_CH0.DX5F	P2.4	USIC1_CH0.MCLKOUT	P2.13	USIC1_CH0.SCLKOUT	P0.2, P2.12, P4.3, P4.5, P4.6
USIC1_CH0.SELO0	P4.7	USIC1_CH0.SELO1	P3.0, P4.8	USIC1_CH0.SELO2	P4.9
USIC1_CH1.DOUT0	P0.0, P0.1, P2.12, P2.13, P3.0	USIC1_CH1.DX0A	P0.0	USIC1_CH1.DX0B	P0.1
USIC1_CH1.DX0C	P2.12	USIC1_CH1.DX0D	P2.13	USIC1_CH1.DX0E	P3.0
USIC1_CH1.DX1A	P0.1	USIC1_CH1.DX1B	P2.12	USIC1_CH1.DX1D	P3.0
USIC1_CH1.DX3B	P0.15	USIC1_CH1.DX3C	P2.4	USIC1_CH1.DX3E	P2.6
USIC1_CH1.DX4B	P0.15	USIC1_CH1.DX4C	P2.4	USIC1_CH1.DX4E	P2.6
USIC1_CH1.DX5B	P0.14	USIC1_CH1.DX5C	P2.3	USIC1_CH1.DX5D	P2.5
USIC1_CH1.DX5E	P2.7	USIC1_CH1.DX5F	P4.4	USIC1_CH1.SCLKOUT	P0.1, P0.3, P2.12, P3.0
USIC1_CH1.SELO0	P0.4	USIC1_CH1.SELO2	P4.1	USIC1_CH1.SELO3	P4.2
VADC0.EMUX00	P0.4, P2.12	VADC0.EMUX01	P0.3, P2.13	VADC0.EMUX02	P0.2
VADC0.EMUX10	P0.5	VADC0.EMUX11	P0.6	VADC0.EMUX12	P0.7
VADC0.G0CH0	P2.6	VADC0.G0CH1	P2.8	VADC0.G0CH2	P2.9
VADC0.G0CH3	P2.10	VADC0.G0CH4	P2.11	VADC0.G0CH5	P2.0
VADC0.G0CH6	P2.1	VADC0.G0CH7	P2.2	VADC0.G1CH0	P2.8
VADC0.G1CH1	P2.7	VADC0.G1CH2	P2.10	VADC0.G1CH3	P2.11
VADC0.G1CH4	P2.9	VADC0.G1CH5	P2.3	VADC0.G1CH6	P2.4

(table continues...)

Table 5 (continued) GPIO alternate functions

VADC0.G1CH7	P2.5	WWDT.SERVICE_OUT	P0.4, P0.13		

6 Electrical specifications

This section provides the electrical parameters which are implementation-specific for the PSOC™ Control C1.

6.1 General parameters

6.1.1 Absolute maximum ratings

Stresses above the values listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 6 Absolute maximum rating parameters

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Junction temperature	T_J	-40	–	115	°C	–
Storage temperature	T_{ST}	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	-0.3	–	6	V	–
Voltage on digital pins with respect to V_{SSP} [1]	V_{IN}	-0.5	–	V_{DDP} + 0.5 or max. 6	V	Whichever is lower
Voltage on P2 pins with respect to V_{SSP} [2]	V_{INP2}	-0.3	–	V_{DDP} + 0.3	V	–
Voltage on analog input pins with respect to V_{SSP}	V_{AIN} V_{AREF}	-0.5	–	V_{DDP} + 0.5 or max. 6	V	Whichever is lower
Input current on any pin during overload condition	I_{IN}	-10	–	10	mA	–
Absolute maximum sum of all input currents during overload condition	ΣI_{IN}	-50	–	+50	mA	–

1) Excluding port pins P2.[1,2,6,7,8,9,11].
2) Applicable to port pins P2.[1,2,6,7,8,9,11].

6.1.2 Pin reliability in overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 7 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- Operating conditions are met for:
  - pad supply levels (V_{DDP})
  - temperature

If a pin current is outside of the Operating conditions but within the overload conditions, then the parameters of this pin as stated in the operating conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

***Note**: An overload condition on one or more pins does not require a reset.*

***Note**: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.*

Table 7 Overload parameters

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Input current on any port pin during overload condition	I_{OV}	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS}	–	–	25	mA	

Figure 7shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

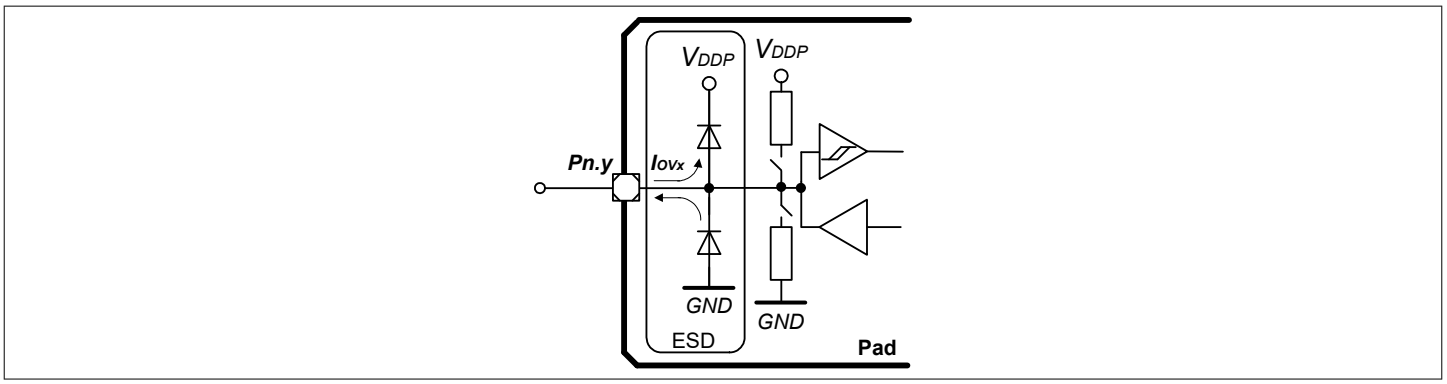


Figure 7 Input overload current via ESD structures

Table 8 and Table 9 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the Absolute maximum ratings must not be exceeded during overload.

Table 8 PN-junction characteristics for positive overload

Pad type	I_{OV} = 5 mA
Standard, high-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5$ V $V_{AIN} = V_{DDP} + 0.5$ V $V_{AREF} = V_{DDP} + 0.5$ V
P2.[1,2,6:9,11]	$V_{INP2} = V_{DDP} + 0.3$ V

Table 9 PN-junction characteristics for negative overload

Pad type	I_{OV} = 5 mA
Standard, high-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5$ V $V_{AIN} = V_{SS} - 0.5$ V $V_{AREF} = V_{SS} - 0.5$ V
P2.[1,2,6:9,11]	$V_{INP2} = V_{SS} - 0.3$ V

6.1.3 Operating conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the PSOC™ Control C1. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 10 Operating conditions parameters

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Ambient temperature	T_A	-40	–	85	°C	Temperature range F
		-40	–	105	°C	Temperature range X
Digital supply voltage[1)]	V_{DDP}	1.8	–	5.5	V	
Short-circuit current of digital outputs	I_{SC}	-5	–	5	mA	
Absolute sum of short-circuit currents of the device	ΣI_{SC_D}	–	–	25	mA	

1) See also the supply monitoring thresholds, Power-up and supply threshold characteristics.

6.2 DC parameters

6.2.1 Input/output characteristics

Table 11 provides the characteristics of the input/output pins of the PSOC™ Control C1.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Note: *Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.*

Table 11 Input/output characteristics (operating conditions apply)

Parameter	Symbol	Limit values		Unit	Note/test condition
		Min	Max		
Output low voltage on port pins (with standard pads)	V_{OLP}	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
		–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on high-current pads	V_{OLP1}	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
		–	0.32	V	I_{OL}= 10 mA (5 V)
		–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = –7 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = –4.5 mA (5 V) I_{OH} = –2.5 mA (3.3 V)
Output high voltage on high current pads	V_{OHP1}	V_{DDP} - 0.32	–	V	I_{OH} = –6 mA (5 V)
		V_{DDP} - 1.0	–	V	I_{OH} = –8 mA (3.3 V)
		V_{DDP} - 0.4	–	V	I_{OH} = –4 mA (3.3 V)
Input low voltage on port pins (standard hysteresis)	V_{ILPS}	–	0.19 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V, and 2.2 V)
Input high voltage on port pins (standard hysteresis)	V_{IHPS}	0.7 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V, and 2.2 V)
Input low voltage on port pins (large hysteresis)	V_{ILPL}	–	0.08 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V, and 2.2 V)
Input high voltage on port pins (large hysteresis)	V_{IHPL}	0.85 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V, and 2.2 V)
Rise/fall time on high-current pad[1)]	t_{HCPR}, t_{HCPF}	–	9	ns	50 pF at 5 V[2)]
		–	12	ns	50 pF at 3.3 V[3)]
		–	25	ns	50 pF at 1.8 V[4)]
Rise/fall time on standard pad Input/output characteristics	t_R, t_F	–	12	ns	50 pF at 5 V[5)]
		–	15	ns	50 pF at 3.3 V[6)]
		–	31	ns	50 pF at 1.8 V[7)]
Input hysteresis on port pin except P2.3 - P2.9[8)]	*HYS*	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), standard hysteresis

(table continues...)

Table 11 (continued) Input/output characteristics (operating conditions apply)

Parameter	Symbol	Limit values		Unit	Note/test condition
		Min	Max		
		0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), standard hysteresis
		0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), standard hysteresis
		0.5 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode (5 V), large hysteresis
		0.4 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode (3.3 V), large hysteresis
		0.2 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode (2.2 V), large hysteresis
Input Hysteresis on port pin P2.3 - P2.9 Input/output characteristics	*HYS*_P2	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), standard hysteresis
		0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), standard hysteresis
		0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), standard hysteresis
		0.35 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode (5 V), large hysteresis
		0.25 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode (3.3 V), large hysteresis
		0.15 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode (2.2 V), large hysteresis
Pin capacitance (digital inputs/ outputs)	C_{IO}	–	10	pF	
Pull-up current on port pins	I_{PUP}	–	-80	µA	$V_{IH,min}$ (5 V)
		-95	–	µA	$V_{IL,max}$ (5 V)
		–	-50	µA	$V_{IH,min}$ (3.3 V)
		-65	–	µA	$V_{IL,max}$ (3.3 V)
Pull-down current on port pins	I_{PDP}	–	40	µA	$V_{IL,max}$ (5 V)
		95	–	µA	$V_{IH,min}$ (5 V)
		–	30	µA	$V_{IL,max}$ (3.3 V)
		60	–	µA	$V_{IH,min}$ (3.3 V)
Input leakage current except P0.11[9]	I_{OZP}	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105°C$

(table continues...)

Table 11 (continued) Input/output characteristics (operating conditions apply)

Parameter	Symbol	Limit values		Unit	Note/test condition
		Min	Max		
Input leakage current for P0.11Input/output characteristics	I_{OZP1}	-10	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105°C$
Voltage on any pin during V_{DDP} power off	V_{PO}	–	0.3	V	*10)*
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	-10	11	mA	–
Maximum current per high current pins	I_{MP1A}	-10	50	mA	–
Maximum current into V_{DDP} (VQFN64, LQFP64)	I_{MVDD1}	–	520	mA	
Maximum current into V_{DDP} (VQFN48)	I_{MVDD2}	–	390	mA	
Maximum current into V_{DDP} (VQFN40)	I_{MVDD3}	–	260	mA	
Maximum current out of V_{SS} (VQFN64, LQFP64)	I_{MVSS1}	–	390	mA	
Maximum current out of V_{SS} (VQFN48)	I_{MVSS2}	–	260	mA	
Maximum current out of V_{SS} (VQFN40)	I_{MVSS3}	–	260	mA	

1) Rise/fall time parameters are taken with 10% - 90% of supply.
2) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF at 0.150 ns/pF at 5 V supply voltage.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF at 0.205 ns/pF at 3.3 V supply voltage.
4) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF at 0.445 ns/pF at 1.8 V supply voltage.
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF at 0.225 ns/pF at 5 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF at 0.288 ns/pF at 3.3 V supply voltage.
7) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF at 0.588 ns/pF at 1.8 V supply voltage.
8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

6.2.2 Analog-to-digital converters (ADC)

Table 12 shows the analog-to-digital converter (ADC) characteristics.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 12 ADC characteristics (operating conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Supply voltage range (internal reference)	V_{DD_int}	2.0	–	3.0	V	SHSCFG.AREF = 11_B; CALCTR.CALGNSTC = $0C_H$ for f_{SH} = 32 MHz, 12_H for f_{SH} = 48 MHz
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext}	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN}	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground[2)]	V_{REFGND}	V_{SSP} - 0.05	–	1.0	V	G0CH0
		V_{SSP} - 0.05	–	0.2	V	G1CH0
Internal reference voltage (full scale value)	V_{REFINT}	5			V	
Switched capacitance of an analog input	C_{AINS}	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT}	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT}	–	–	10	pF	
Gain settings	G_{IN}	1			–	GNCTRxz.GAINy = 00_B (unity gain)
		3			–	GNCTRxz.GAINy = 01_B (gain g1)
		6			–	GNCTRxz.GAINy = 10_B (gain g2)
		12			–	GNCTRxz.GAINy = 11_B (gain g3)
Sample time	t_{sample}	5	–	–	$1/f_{ADC}$	V_{DD} = 5.0 V, f_{ADCI} = 48 MHz

(table continues...)

Table 12 (continued) ADC characteristics (operating conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
		3	–	–	$1/f_{ADC}$	V_{DD} = 5.0 V, f_{ADCI} = 32 MHz
		3	–	–	$1/f_{ADC}$	V_{DD} = 3.3 V, f_{ADCI} = 32 MHz
		30	–	–	$1/f_{ADC}$	V_{DD} = 2.0 V, f_{ADCI} = 32 MHz
Conversion time in fast compare mode	t_{CF}	9			$1/f_{ADC}$	[3)]
Conversion time in 12-bit mode	t_{C12}	20			$1/f_{ADC}$	
Maximum sample rate in 12-bit mode[4)]	f_{C12}	–	–	$f_{ADC}/42.5$	–	1 sample pending
		–	–	$f_{ADC}/62.5$	–	2 samples pending
Conversion time in 10-bit mode	t_{C10}	18			$1/f_{ADC}$	
Maximum sample rate in 10-bit mode Analog-to-digital converters (ADC)	f_{C10}	–	–	$f_{ADC}/40.5$	–	1 sample pending
		–	–	$f_{ADC}/58.5$	–	2 samples pending
Conversion time in 8-bit mode	t_{C8}	16			$1/f_{ADC}$	
Maximum sample rate in 8-bit mode Analog-to-digital converters (ADC)	f_{C8}	–	–	$f_{ADC}/38.5$	–	1 sample pending
		–	–	$f_{ADC}/54.5$	–	2 samples pending
RMS noise[5)]	EN_{RMS}	–	1.5	–	LSB12	DC input, SHSCFG.AREF = 00_B, GNCTRxz.GAINy = 00_B (unity gain), V_{DD} = 5.0 V, V_{AIN} = 2.5 V, 25°C
DNL error	EA_{DNL}	–	±2.0	–	LSB12	
INL error	EA_{INL}	–	±4.0	–	LSB12	
Gain error with external reference	EA_{GAIN}	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference [6)]	EA_{GAIN}	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 110°C

(table continues...)

Table 12 (continued) ADC characteristics (operating conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF}	–	±8.0	–	mV	Calibrated, V_{DD} = 5.0 V

1) The parameters are defined for ADC clock frequencies f_{SH} = 32 MHz for the full supply range, and f_{SH} = 48 MHz at V_{DD_int}, V_{DD_ext} = 5 V. Usage of any other frequencies may affect the ADC performance.
2) The alternate reference ground connection is separate for each converter. This mode, therefore, provides the lowest noise impact.
3) No pending samples assumed, excluding sampling time and calibration.
4) Includes synchronization and calibration (average of gain and offset calibration).
5) This parameter can also be defined as an SNR value: SNR[dB] = 20 × log(A_{MAXeff}/N_{RMS}).
With $A_{MAXeff} = 2^N/2$, SNR[dB] = 20 × log(2048/N_{RMS}) [N = 12].
N_{RMS} = 1.5 LSB12, therefore, equals SNR = 20 × log(2048/1.5) = 62.7 dB.
6) Includes error from the reference voltage.

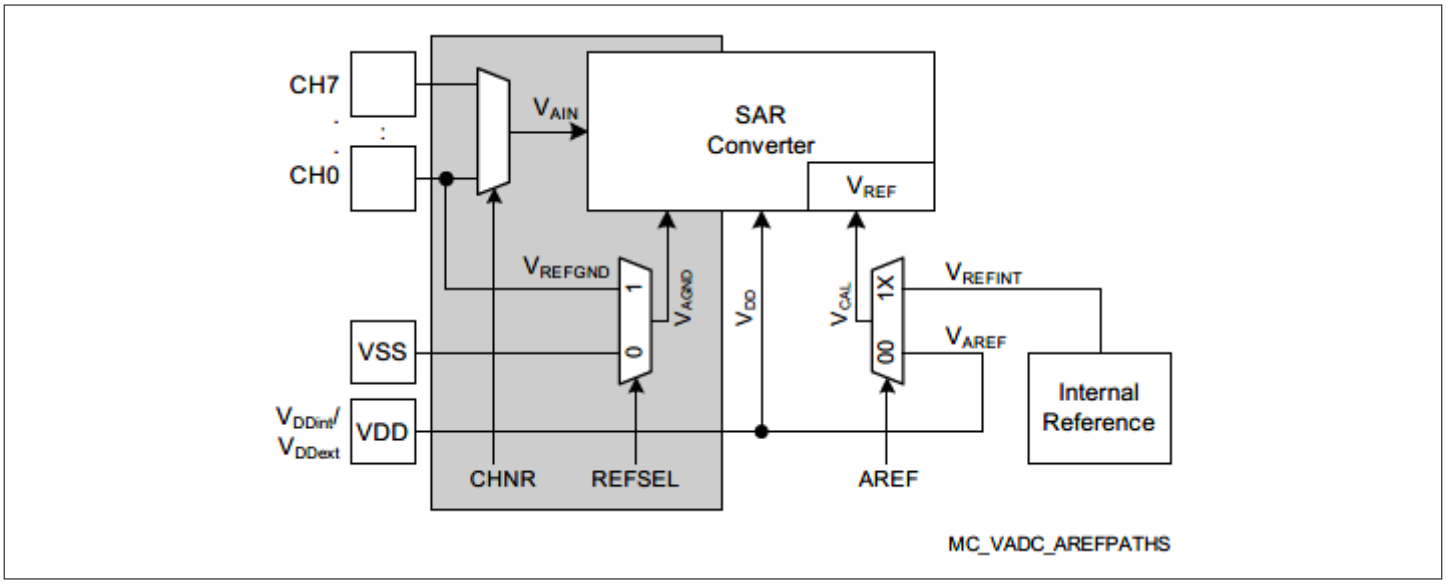


Figure 8 ADC voltage supply

6.2.3 Out-of-range comparator (ORC) characteristics

The out-of-range comparator (ORC) triggers on analog input voltages (V_{AIN}) above V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 13 Out-of-range comparator (ORC) characteristics (operating conditions apply; V_{DDP} = 3.0 V - 5.5 V; C_L = 0.25 pF)

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
DC switching level	V_{ODC}	–	–	180	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	15	–	54	mV	

(table continues...)

Table 13 (continued) Out-of-range comparator (ORC) characteristics (operating conditions apply; V_{DDP} = 3.0 V - 5.5 V; C_L = 0.25 pF)

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Always detected overvoltage pulse	t_{OPDD}	103	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
		88	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Never detected overvoltage pulse	t_{OPDN}	–	–	21	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
		–	–	11	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Detection delay	t_{ODD}	39	–	132	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
		31	–	121	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Release delay	t_{ORD}	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 5 V
		57	–	340	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 3.3 V
Enable delay	t_{OED}	–	–	300	ns	ORCCTRL.ENORCx = 1

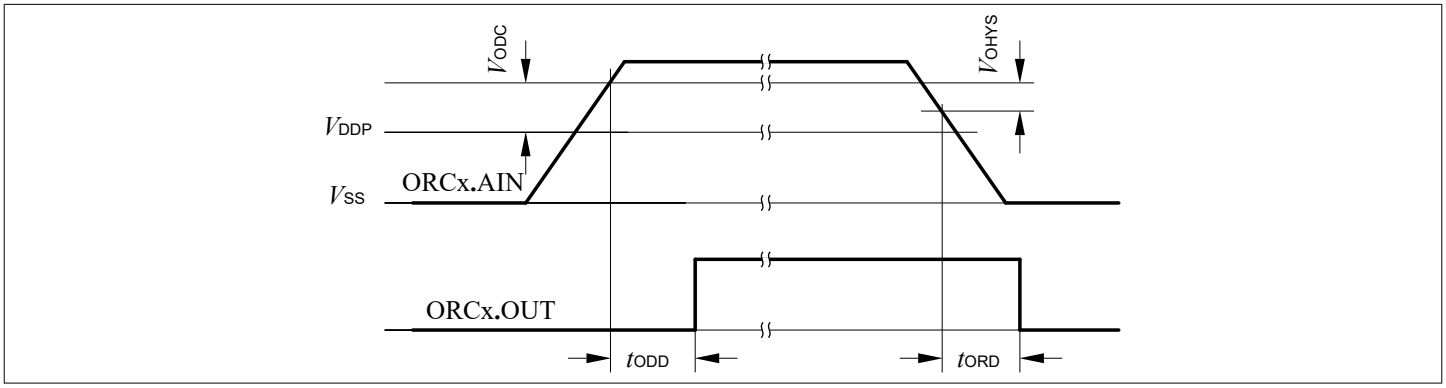


Figure 9 ORCx.OUT trigger generation

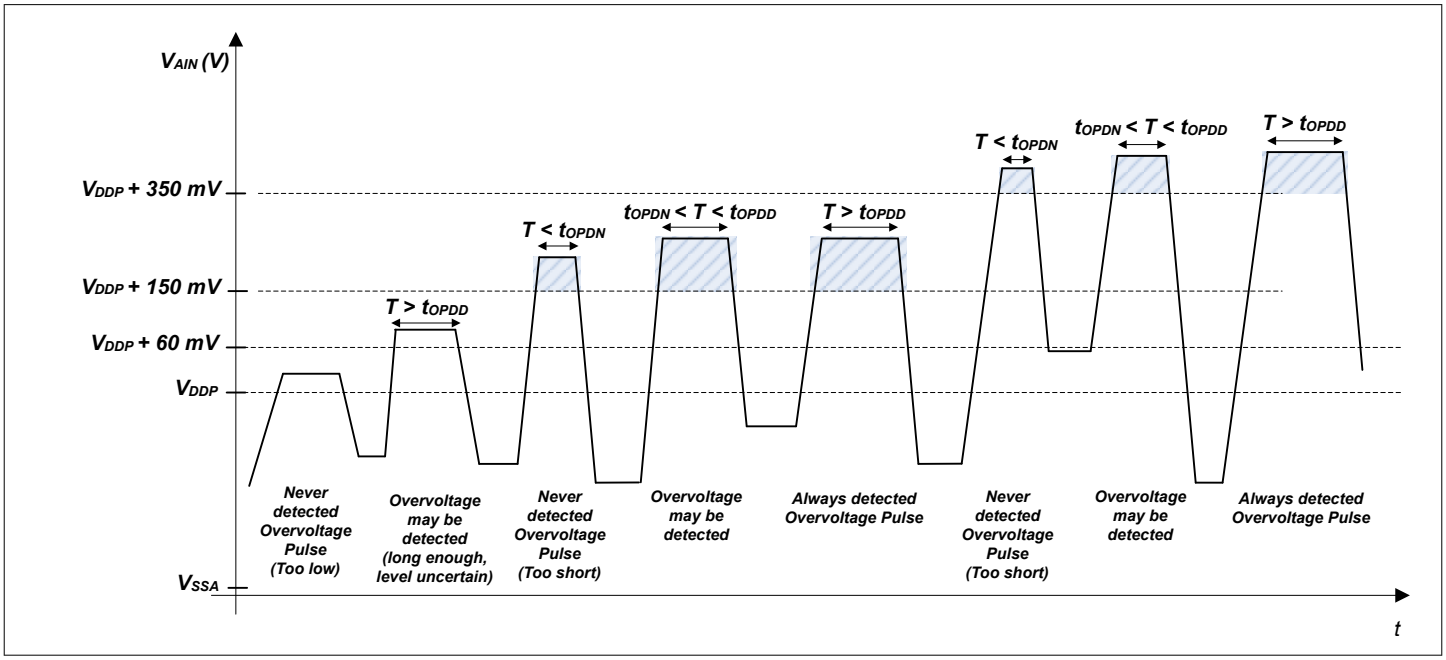


Figure 10 ORC detection ranges

6.2.4 Analog comparator characteristics

Table 14 shows the analog comparator characteristics.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 14 Analog comparator characteristics (operating conditions apply)

Parameter	Symbol	Limit values			Unit	Note/test condition
		Min	Typ	Max		
Input voltage	V_{CMP}	-0.05	–	V_{DDP} + 0.05	V	
Input offset	V_{CMPOFF}	–	±3	–	mV	High power mode ΔV_{CMP} < 200 mV
Propagation delay[1)]	t_{PDELAY}	–	25	–	ns	High power mode, ΔV_{CMP} = 100 mV
		–	80	–	ns	High power mode, ΔV_{CMP} = 25 mV
		–	250	–	ns	Low power mode, ΔV_{CMP} = 100 mV
		–	700	–	ns	Low power mode, ΔV_{CMP} = 25 mV
Current consumption	I_{ACMP}	–	100	–	µA	First active ACMP in high power mode, ΔV_{CMP} > 30 mV
		–	66	–	µA	Each additional ACMP in high power mode, ΔV_{CMP} > 30 mV
		–	10	–	µA	First active ACMP in low power mode
		–	6	–	µA	Each additional ACMP in low power mode
Input hysteresis	V_{HYS}	–	±15	–	mV	
Filter delay	t_{FDELAY}	–	5	–	ns	

1) Total analog comparator delay is the sum of propagation delay and filter delay.

6.2.5 Temperature sensor characteristics

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 15 Temperature sensor characteristics

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Measurement time	t_M	–	–	10	ms	

(table continues...)

Table 15 (continued) Temperature sensor characteristics

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Temperature sensor range	T_{SR}	-40	–	115	°C	
Sensor accuracy[1)]	T_{TSAL}	-6	–	6	°C	$T_J > 20°C$
		-10	–	10	°C	$0°C \le T_J \le 20°C$
		–	-/+8	–	°C	$T_J < 0°C$
Start-up time	t_{TSST}	–	–	15	µs	

1) The temperature sensor accuracy is independent of the supply voltage.

6.2.6 Oscillator pins

***Note**: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

The oscillator pins can be operated with an external crystal/resonator (see Figure 11) or in direct input mode (see Figure 12).

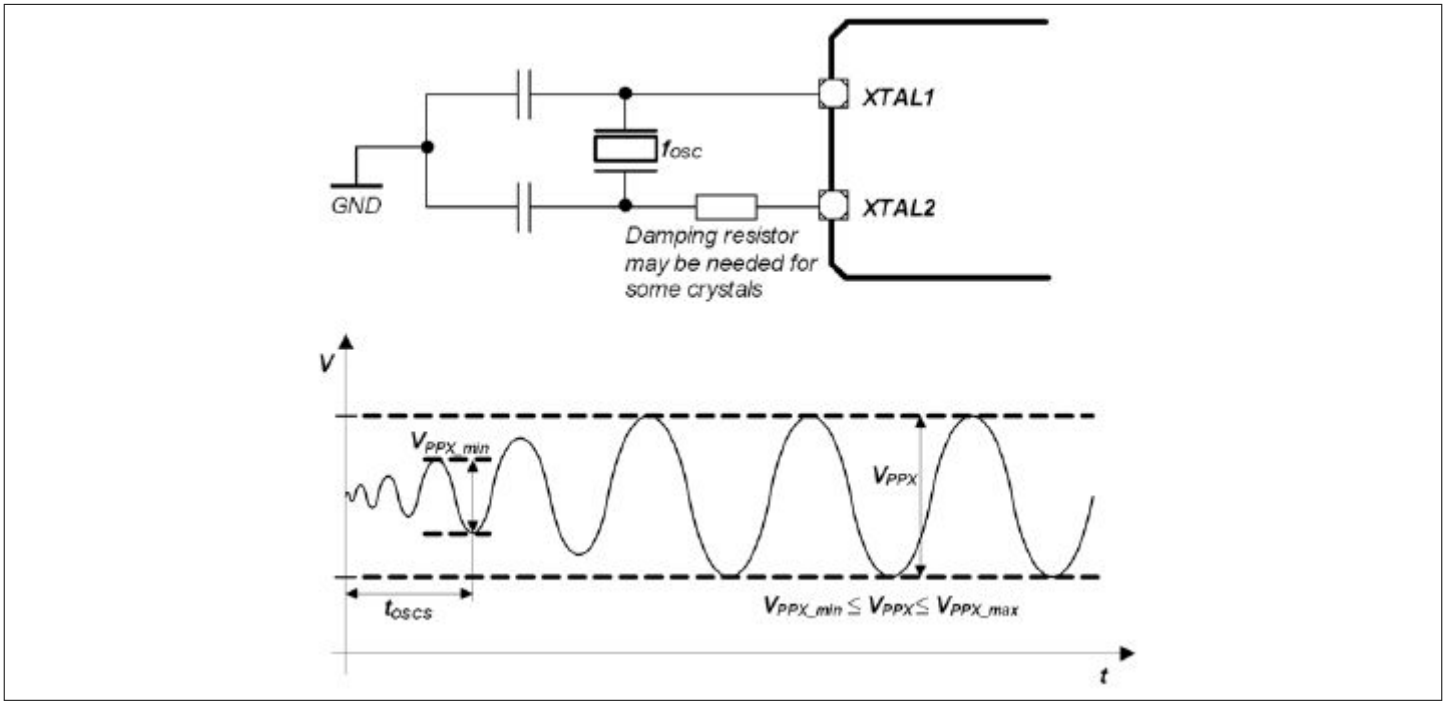


Figure 11 Oscillator in crystal mode

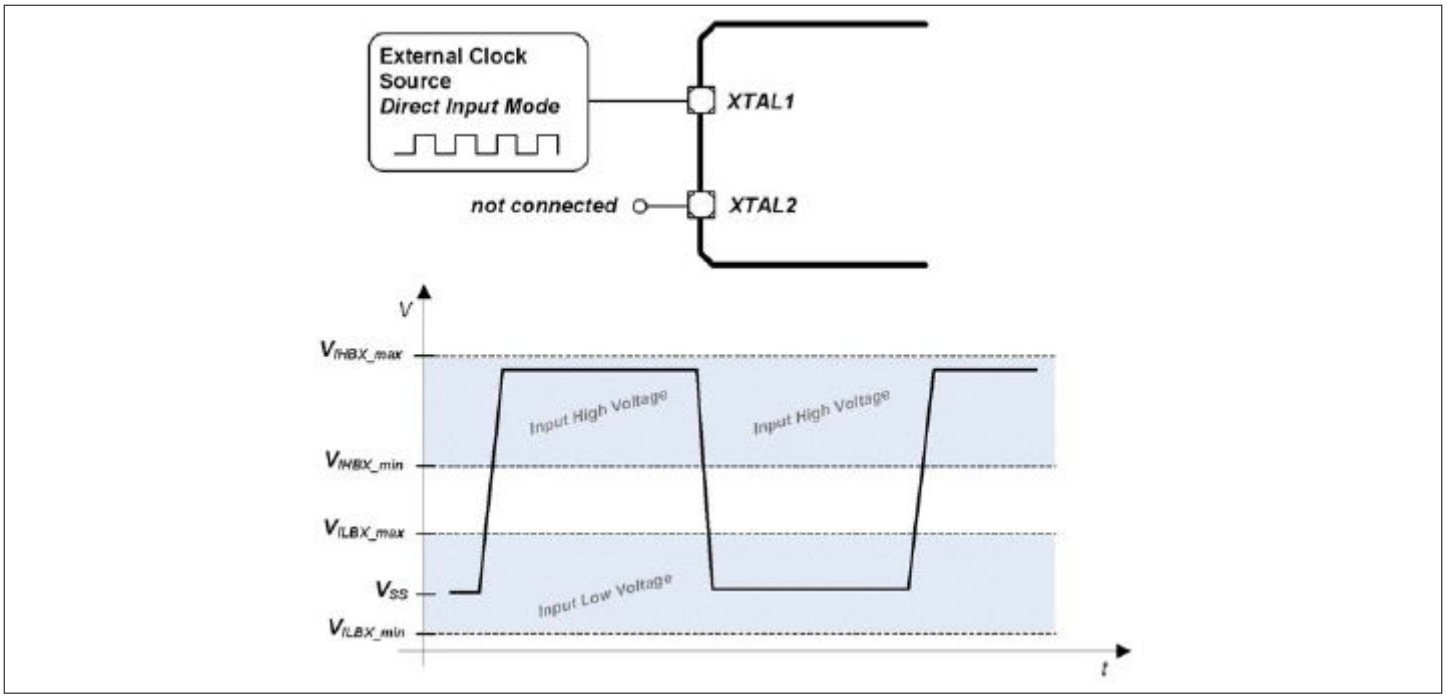


Figure 12 Oscillator in direct input mode

Table 16 OSC_XTAL parameters

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Input frequency	f_{OSC}	4	–	48	MHz	Direct Input Mode
		4	–	20	MHz	External Crystal Mode
Oscillator start-up time[1) 2)]	t_{OSCS}	–	–	10	ms	
Input voltage at XTAL1	V_{IX}	-0.3	–	1.5	V	External Crystal Mode
		-0.3	–	5.5	V	Direct Input Mode
Input amplitude (peak- to-peak) at XTAL1[3)]	V_{PPX}	0.6	–	1.7	V	External Crystal Mode

1) t_{OSCS} is defined from the moment the oscillator is enabled with SCU_ANAOSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of 0.9 * V_{PPX}.
2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
3) If the shaper unit is enabled and not bypassed.

Table 17 RTC_XTAL parameters

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Input frequency	f_{OSC}	–	32.768	–	kHz	
Oscillator start-up time[1) 2)]	t_{OSCS}	–	–	5	s	

(table continues...)

Table 17 (continued) RTC_XTAL parameters

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Input voltage at RTC_XTAL1	V_{IX}	-0.3	–	1.5	V	
Input amplitude (peak- to-peak) at RTC_XTAL1[3]	V_{PPX}	0.2	–	1.2	V	

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_ANAOSCLPCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 0.9 * V_{PPX}.
2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
3) If the shaper unit is enabled and not bypassed.

6.2.7 Power supply current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (for example, thermal connection or used application configurations).

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 18 Power supply parameter table; V_{DDP} = 5 V

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ[1]	Max		
Active mode current Peripherals enabled f_{MCLK}/f_{PCLK} in MHz[2]	I_{DDPAE}	–	14.1	20	mA	48/96
		–	9.8	–	mA	24/48
		–	7.8	–	mA	16/32
		–	6.4	–	mA	8/16
		–	4.4	–	mA	1/1
Active mode current Peripherals disabled f_{MCLK}/f_{PCLK} in MHz[3]	I_{DDPAD}	–	6.2	–	mA	48/96
		–	4.6	–	mA	24/48
		–	3.6	–	mA	16/32
		–	3.1	–	mA	8/16
		–	1.8	–	mA	1/1
Active mode current Code execution from RAM flash is powered down f_{MCLK}/f_{PCLK} in MHz	I_{DDPAR}	–	9.6	–	mA	48/96
Sleep mode current Peripherals clock enabled f_{MCLK}/f_{PCLK} in MHz[4]	I_{DDPSE}	–	11.0	–	mA	48/96
		–	7.6	–	mA	24/48
		–	6.4	–	mA	16/32

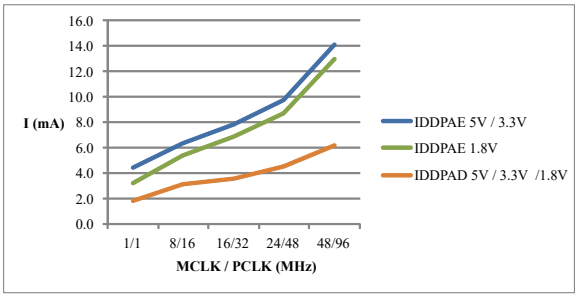
(table continues...)

Table 18 (continued) Power supply parameter table; V_{DDP} = 5 V

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ[1]	Max		
		–	5.3	–	mA	8/16
		–	4.2	–	mA	1/1
Sleep mode current Peripherals clock disabled Flash active f_{MCLK}/f_{PCLK} in MHz[5]	I_{DDPSD}	–	2.8	–	mA	48/96
		–	2.2	–	mA	24/48
		–	2.0	–	mA	16/32
		–	1.9	–	mA	8/16
		–	1.7	–	mA	1/1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK}/f_{PCLK} in MHz[6]	I_{DDPSR}	–	2.2	–	mA	48/96
		–	1.7	–	mA	24/48
		–	1.4	–	mA	16/32
		–	1.2	–	mA	8/16
		–	1.1	–	mA	1/1
Deep Sleep mode current[7]	I_{DDPDS}	–	0.27	–	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA}	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA}	–	290	–	µsec	

1) The typical values are measured at T_A = + 25°C and V_{DDP} = 5 V.
2) CPU and all peripherals clock enabled, flash is in Active mode.
3) CPU enabled, all peripherals clock disabled, flash is in Active mode.
4) CPU in sleep, all peripherals clock enabled and flash is in Active mode.
5) CPU in sleep, flash is in Active mode.
6) CPU in sleep, flash is powered down and code executed from RAM after wake up.
7) CPU in sleep, peripherals clock disabled, flash is powered down and code executed from RAM after wake up.
8) CPU in sleep, flash is in Active mode during Sleep mode.
9) CPU in sleep, flash is in powered down mode during Deep Sleep mode.

Figure 13 shows typical graphs for active mode supply current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 13 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

Figure 14 shows typical graphs for sleep mode current for V_{DDP} = 5 V, V_{DDP} = 3.3 V, V_{DDP} = 1.8 V across different clock frequencies.

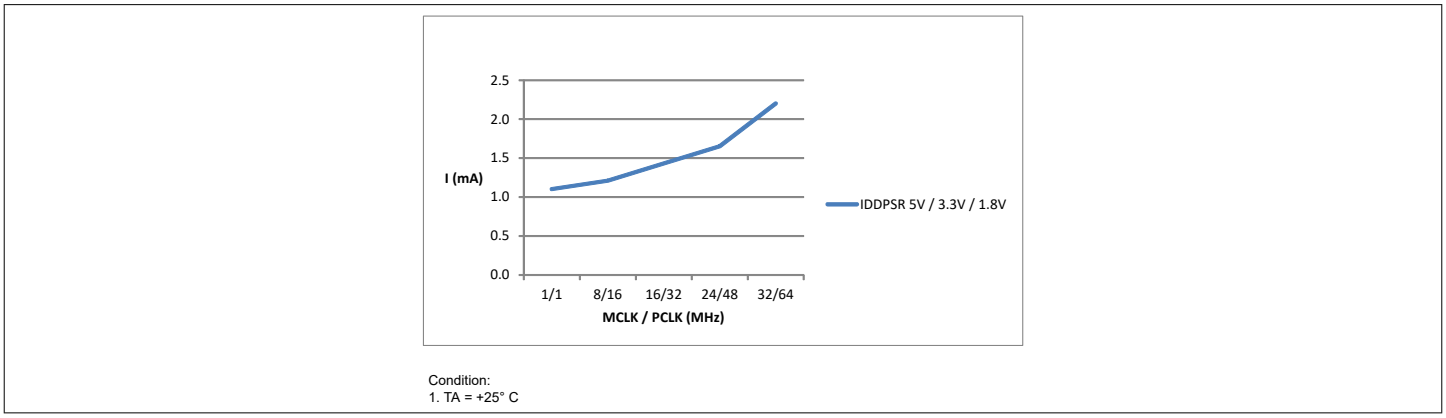


Figure 14 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSD} over-supply voltage V_{DDP} for different clock frequencies

Table 19 provides the active current consumption of some modules operating at 5 V power supply at 25°C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 19 Typical active current parameter table

Active current consumption	Symbol	Limit values	Unit	Note/test condition
		Typ		
Baseload current	I_{CPUDDC}	4.14	mA	Modules including Core, SCU, PORT, memories, ANATOP[1)]
VADC and SHS	I_{ADCDDC}	3.73	mA	Set CGATCLR0.VADC to 1[2)]
USICx	$I_{USIC0DDC}$	1.35	mA	Set CGATCLR0.USIC0 to 1[3)]
CCU4x	$I_{CCU40DDC}$	0.99	mA	Set CGATCLR0.CCU40 to 1[4)]
CCU8x	$I_{CCU80DDC}$	1.00	mA	Set CGATCLR0.CCU80 to 1[5)]
POSIFx	$I_{PIF0DDC}$	1.05	mA	Set CGATCLR0.POSIF0 to 1[6)]
BCCU0	$I_{BCCU0DDC}$	0.29	mA	Set CGATCLR0.BCCU0 to 1[7)]
MATH	$I_{MATHDDC}$	0.50	mA	Set CGATCLR0.MATH to 1[8)]
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1[9)]
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1[10)]
MultiCAN	$I_{MCANDDC}$	1.38	mA	Set CGATCLR0.MCAN0 to 1[11)]

1) Baseload current is measured with device running in user mode, MCLK=PCLK=48 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.
2) Active current is measured with: module enabled, MCLK=48 MHz, running in auto-scan conversion mode.
3) Active current is measured with: module enabled, each of the 2 USIC channels sending alternate messages at 57.6 kbaud every 200 ms.
4) Active current is measured with: module enabled, MCLK=PCLK=48 MHz, 1 CCU4 slice for PWM switching at 20 kHz with duty cycle varying at 10%-90%, 1 CCU4 slice in capture mode for reading period and duty cycle.
5) Active current is measured with: module enabled, MCLK=PCLK=48 MHz, 3 CCU8 slices with PWM frequency at 20 kHz and a period match interrupt used to toggle duty cycle between 10% and 90%.
6) Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, hall sensor mode.
7) Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, FCLK=0.8 MHz, Normal mode (BCCU clock = FCLK/4), 4 BCCU Channels with packers enabled and 1 Dimming Engine, change color or dim every 1 s.
8) Active current is measured with: module enabled, MCLK=48 MHz, PCLK=96 MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11.
9) Active current is measured with: module enabled, MCLK=48 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1 s.

10) Active current is measured with: module enabled, MCLK=48 MHz, Periodic interrupt enabled.
11) Active current is measured with: module enabled, MCLK=48 MHz, running at 20 MHz baud rate generator, 1 node activated, 1 transmit and 1 receive object active.

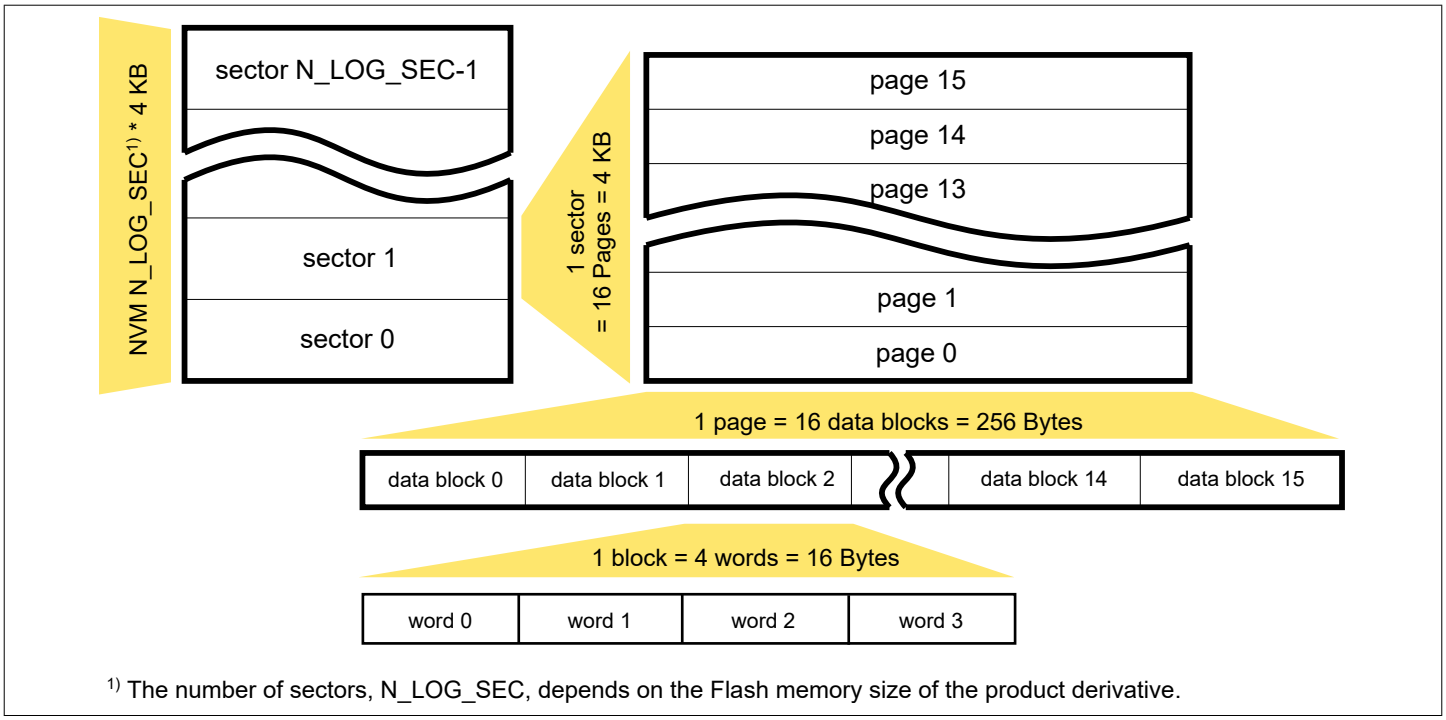
6.2.8 Flash memory parameters

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 20 Flash memory parameters

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Erase time per page/sector	t_{ERASE}	6.8	7.1	7.6	ms	
Program time per block	t_{PSER}	102	152	204	µs	
Wake-up time	t_{WU}	–	32.2	–	µs	
Read time per word	t_a	–	50	–	ns	
Data retention time	t_{RET}	10	–	–	years	Maximum 100 erase/ program cycles
Flash wait states[1)]	$N_{WSFLASH}$	0	0	0		f_{MCLK} = 8 MHz
		0	1	1		f_{MCLK} = 16 MHz
		1	2	2		f_{MCLK} = 32 MHz
		2	2	3		f_{MCLK} = 48 MHz
Erase cycles	N_{ECYC}	–	–	$5*10^4$	cycles	Sum of page and sector erase cycles
Total erase cycles	N_{TECYC}	–	–	$2*10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.



[1] The number of sectors, N_LOG_SEC, depends on the Flash memory size of the product derivative.

Figure 15 Logical structure of the flash

6.3 AC parameters

6.3.1 Testing waveforms

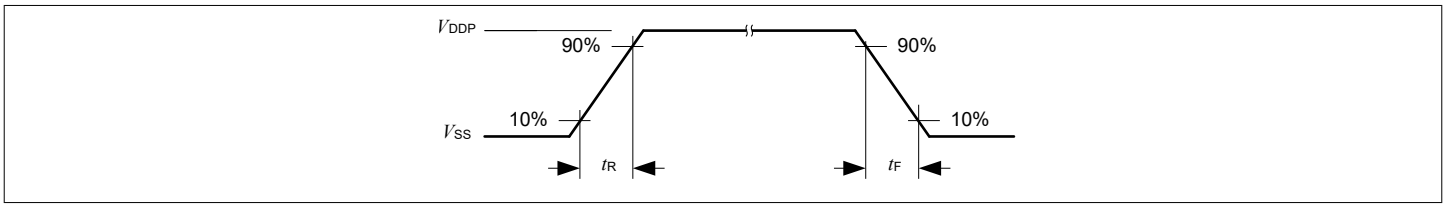


Figure 16 Rise/fall time parameters

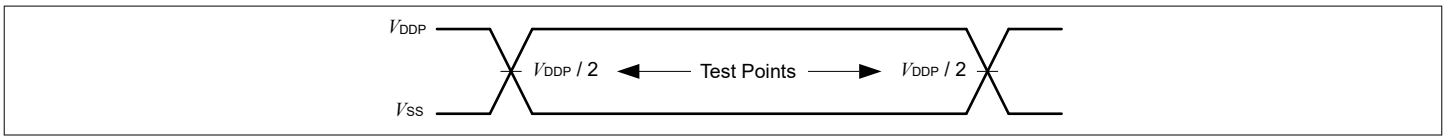


Figure 17 Testing waveform, output delay

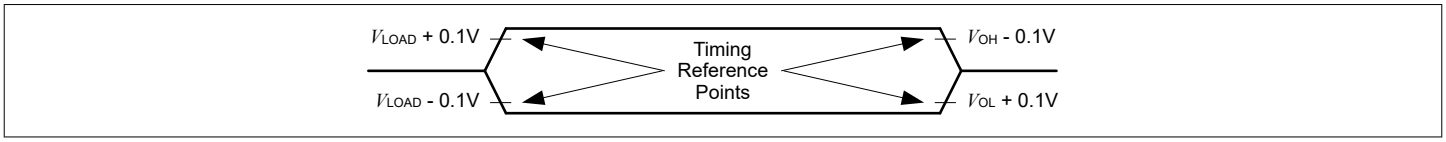


Figure 18 Testing waveform, output high impedance

6.3.2 Power-up and supply threshold characteristics

Table 21 provides the characteristics of the supply threshold in PSOC™ Control C1.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 21 Power-up and supply threshold parameters (operating conditions apply)

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
V_{DDP} ramp-up time	t_{RAMPUP}	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP}	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10}	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DDP}
	$S_{VDDPrise}$	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$ [1)]	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits [2)]
V_{DDP} prewarning voltage	V_{DDPPW}	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B
V_{DDP} brownout reset voltage	V_{DDPBO}	1.55	1.62	1.75	V	Calibrated, before user code starts running.
V_{DDP} voltage to ensure defined pad states	V_{DDPPA}	–	1.0	–	V	
Start-up time from power-on reset	t_{SSW}	–	260	–	µs	Time to the first user code instruction [3)]
BMI program time	t_{BMI}	–	8.25	–	ms	Time taken from a user-triggered system reset after BMI installation is requested.

1) A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.
2) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.
3) This values does not include the ramp-up time. During start-up firmware execution, MCLK is running at 48 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

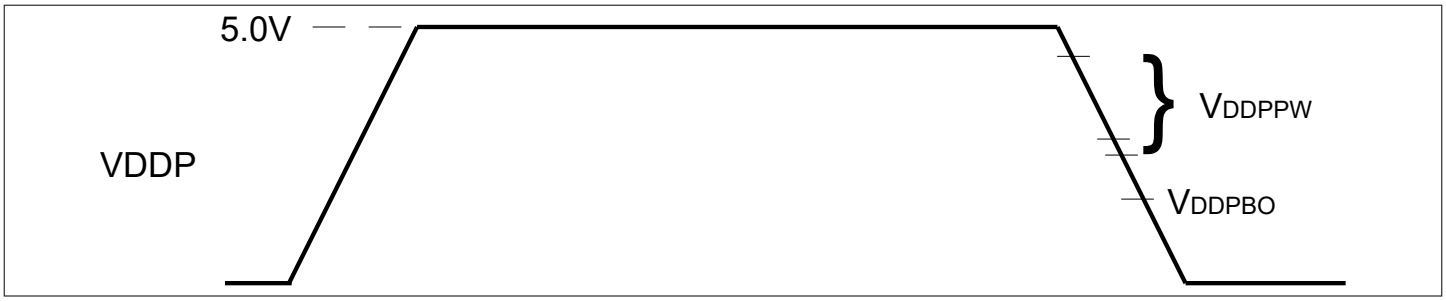


Figure 19 Supply threshold parameters

6.3.3 On-chip oscillator characteristics

Table 22 provides the characteristics of the 96-MHz digital controlled oscillator DCO1.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 22 96-MHz DCO1 characteristics (operating Conditions apply)

Parameter	Symbol	Limit values			Unit	Note/test condition
		Min	Typ	Max		
Nominal frequency	f_{NOM}	–	96	–	MHz	Under nominal conditions[1] after trimming
Accuracy with adjustment based on XTAL as reference	Δf_{LTX}	-0.3	–	0.3	%	With respect to f_{NOM}(typ), over temperature (-40°C to 105°C)
Accuracy	Δf_{LT}	-1.7	–	3.4	%	With respect to f_{NOM}(typ), over temperature (0°C to 85°C)
		-3.9	–	4.0	%	With respect to f_{NOM}(typ), over temperature (-40°C to 105°C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25°C.

Table 23 provides the characteristics of the 32-kHz digital controlled oscillator DCO2.

Table 23 32-kHz DCO2 characteristics (operating conditions apply)

Parameter	Symbol	Limit values			Unit	Note/test condition
		Min	Typ	Max		
Nominal frequency	f_{NOM}	–	32.75	–	kHz	Under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	-1.7	–	3.4	%	With respect to f_{NOM}(typ), over temperature (0°C to 85°C)
		-3.9	–	4.0	%	With respect to f_{NOM}(typ), over temperature (-40°C to 105°

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25°C.

6.3.4 Serial wire debug port (SW-DP) timing

The following parameters are applicable for communication through the SW-DP interface.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 24 SWD interface timing parameters (operating conditions apply)

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
SWDCLK high time	t_1	50	–	500000	ns	–
SWDCLK low time	t_2	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5	–	–	68	ns	C_L = 50 pF
		–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	4	–	–	ns	

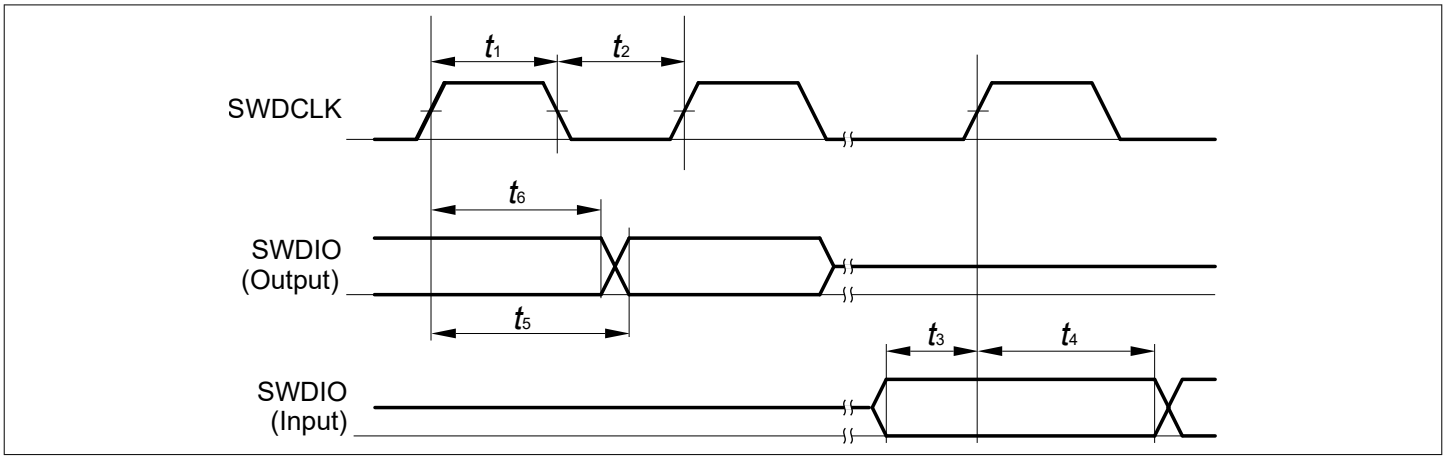


Figure 20 SWD timing

6.3.5 SPD timing requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 25 Optimum number of sample clocks for SPD

Sample frequency	Sampling factor	Sample clocks 0_B	Sample clocks 1_B	Effective decision time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks).

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is ±5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

6.3.6 Peripheral timings

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

6.3.6.1 Synchronous serial interface (USIC SSC) timing

The following parameters are applicable for a USIC channel operated in SSC mode.

***Note**: Operating conditions apply.*

Table 26 USIC SSC master mode timing

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
SCLKOUT master clock period	t_{CLK}	4/*MCLK*	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	t_{CLK}/2 - 28	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3	-28	–	28	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	75	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	0	–	–	ns	

Table 27 USIC SSC slave mode timing

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
DX1 slave clock period	t_{CLK}	4/*MCLK*	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10}	16	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge	t_{11}	17	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge	t_{12}	21	–	–	ns	

(table continues...)

Table 27 (continued) USIC SSC slave mode timing

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge	t_{13}	15	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	–	–	71	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

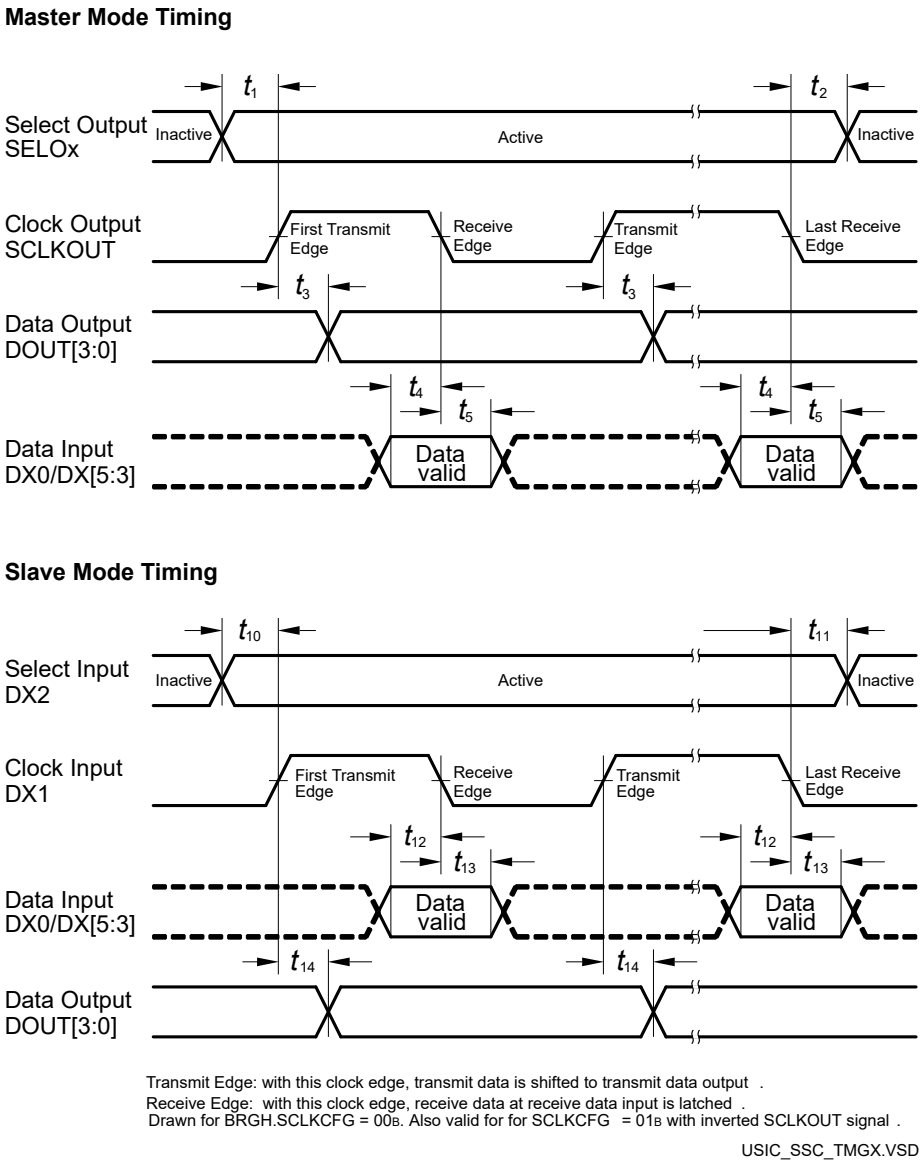


Figure 21 USIC - SSC master/slave mode timing

***Note**: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

6.3.6.2 Inter-IC (IIC) interface timing

The following parameters are applicable for a USIC channel operated in IIC mode.

***Note**: Operating conditions apply.*

Table 28 USIC IIC Standard Mode timing[1)]

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Fall time of both SDA and SCL	t_1	–	–	300	ns	
Rise time of both SDA and SCL	t_2	–	–	1000	ns	
Data hold time	t_3	0	–	–	µs	
Data set-up time	t_4	250	–	–	ns	
LOW period of SCL clock	t_5	4.7	–	–	µs	
HIGH period of SCL clock	t_6	4.0	–	–	µs	
Hold time for (repeated) START condition	t_7	4.0	–	–	µs	
Set-up time for repeated START condition	t_8	4.7	–	–	µs	
Set-up time for STOP condition	t_9	4.0	–	–	µs	
Bus free time between a STOP and START condition	t_{10}	4.7	–	–	µs	
Capacitive load for each bus line	C_b	–	–	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kΩ for operation at 100 kb/s, approximately 2 kΩ for operation at 400 kb/s.

Table 29 USIC IIC Fast Mode timing[1)]

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Fall time of both SDA and SCL	t_1	$20 + 0.1 * C_b$[2)]	–	300	ns	
Rise time of both SDA and SCL	t_2	$20 + 0.1 * C_b$	–	300	ns	
Data hold time	t_3	0	–	–	µs	
Data set-up time	t_4	100	–	–	ns	
LOW period of SCL clock	t_5	1.3	–	–	µs	
HIGH period of SCL clock	t_6	0.6	–	–	µs	
Hold time for (repeated) START condition	t_7	0.6	–	–	µs	
Set-up time for repeated START condition	t_8	0.6	–	–	µs	
Set-up time for STOP condition	t_9	0.6	–	–	µs	

(table continues...)

Table 29 (continued) USIC IIC Fast Mode timing[1)]

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Bus free time between a STOP and START condition	t_{10}	1.3	–	–	µs	
Capacitive load for each bus line	C_b	–	–	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kΩ for operation at 100 kb/s, approximately 2 kΩ for operation at 400 kb/s.
2) C_b refers to the total capacitance of one bus line in pF.

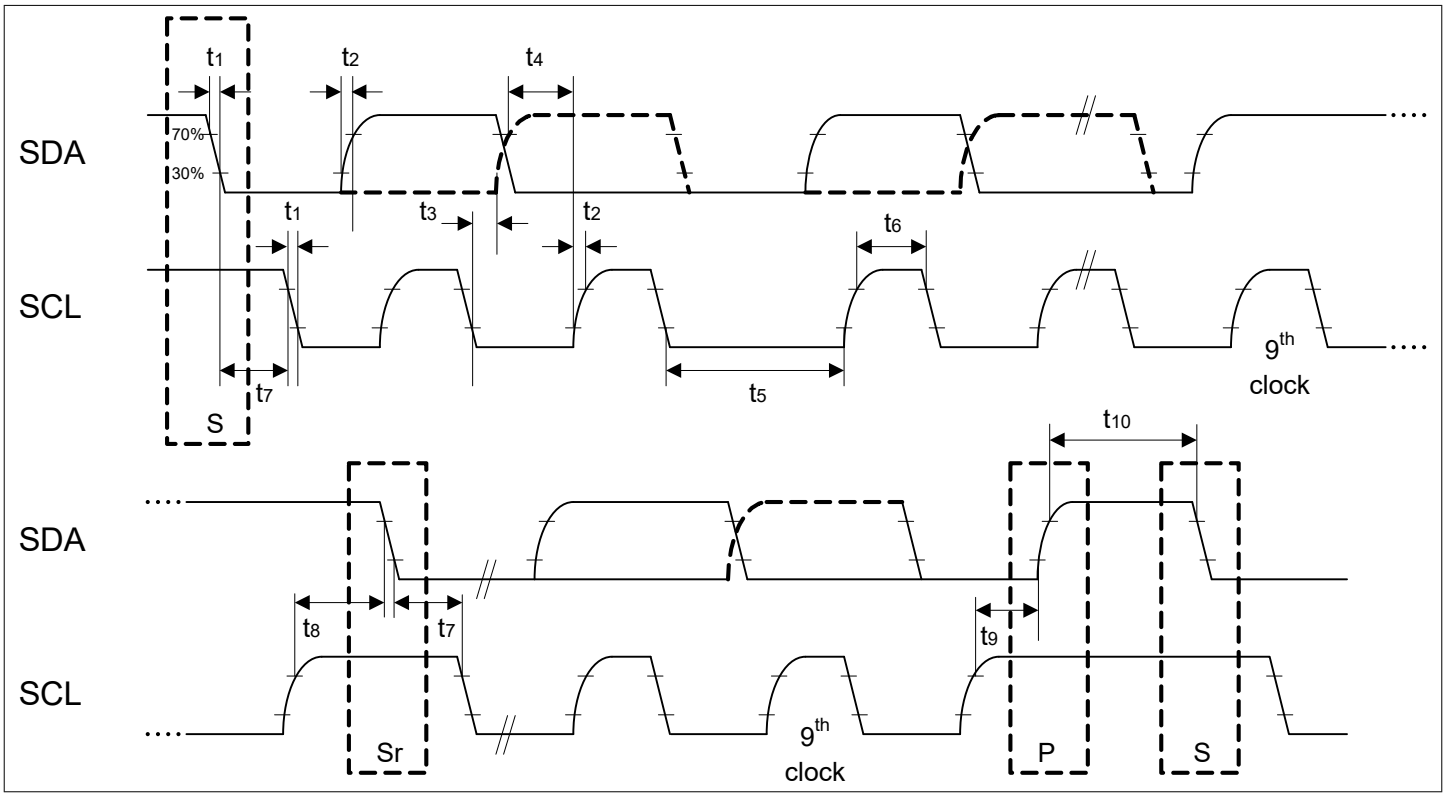


Figure 22 USIC IIC timing

6.3.6.3 Inter-IC Sound (IIS) interface timing

The following parameters are applicable for a USIC channel operated in IIS mode.

***Note**: Operating conditions apply.*

Table 30 USIC IIS master transmitter timing

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Clock period	t_1	$4/f_{MCLK}$	–	–	ns	
Clock HIGH	t_2	$0.35 \times t_{1min}$	–	–	ns	

(table continues...)

Table 30 (continued) USIC IIS master transmitter timing

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Clock LOW	t_3	0.35 × t_{1min}	–	–	ns	
Hold time	t_4	0	–	–	ns	
Clock rise time	t_5	–	–	0.15 × t_{1min}	ns	

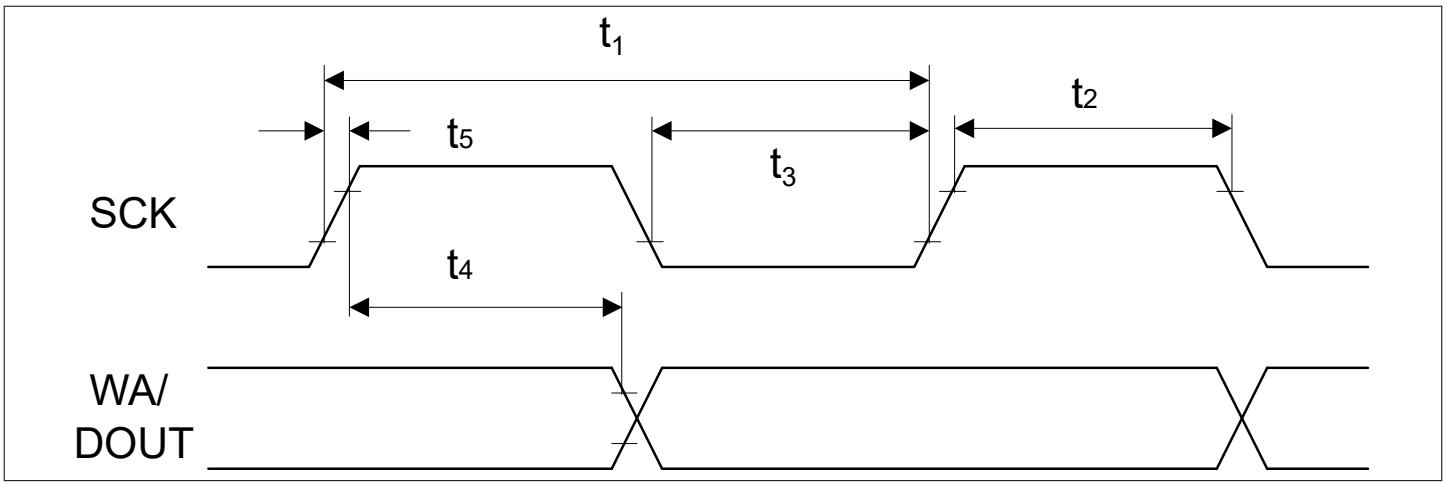


Figure 23 USIC IIS master transmitter timing

Table 31 USIC IIS slave receiver timing

Parameter	Symbol	Values			Unit	Note/test condition
		Min	Typ	Max		
Clock period	t_6	$4/f_{MCLK}$	–	–	ns	
Clock HIGH	t_7	$0.35 \times t_{6min}$	–	–	ns	
Clock LOW	t_8	$0.35 \times t_{6min}$	–	–	ns	
Set-up time	t_9	$0.3 \times t_{6min}$	–	–	ns	
Hold time	t_{10}	15	–	–	ns	

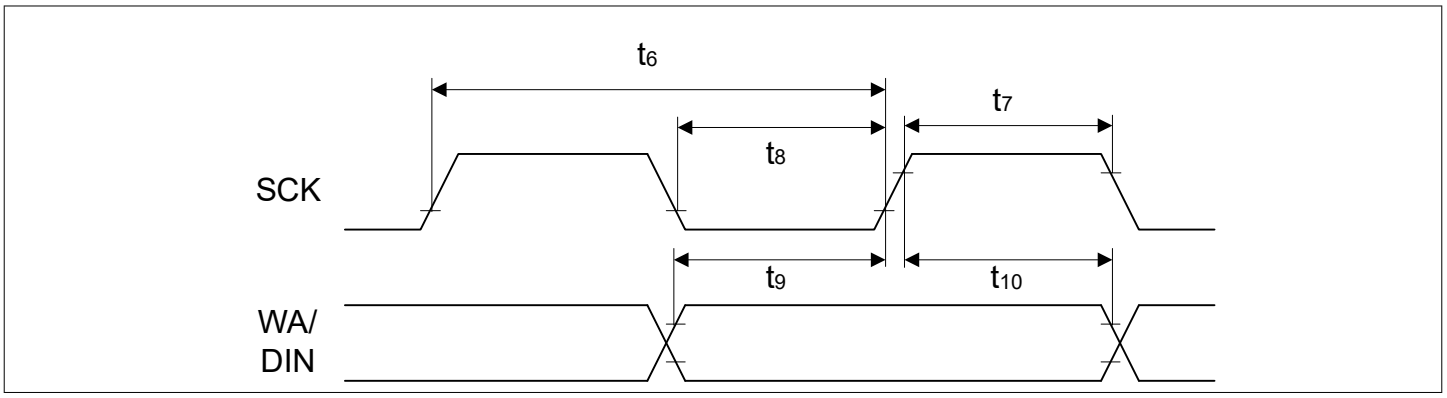


Figure 24 USIC IIS slave receiver timing

7 Ordering information

The following table lists the PSC1M2x, PSC1M3x device ordering information and features.

Table 32 Ordering information

Product	Flash	GPIO	GPI	CAN N/MO	Package
PSC1M2DBTBQ0AT	64 KB	26	8	-	TSSOP-38
PSC1M2EBTBQ0AT	128 KB	26	8	-	TSSOP-38
PSC1M2FBTBQ0AT	200KB	26	8	-	TSSOP-38
PSC1M2DBLEQ0AT	64 KB	27	8	-	VQFN-40
PSC1M2EBLEQ0AT	128 KB	27	8	-	VQFN-40
PSC1M2FBLEQ0AT	200 KB	27	8	-	VQFN-40
PSC1M2DBLGQ0AT	64 KB	34	8	-	VQFN-48
PSC1M2EBLGQ0AT	128 KB	34	8	-	VQFN-48
PSC1M2FBLGQ0AT	200 KB	34	8	-	VQFN-48
PSC1M2DBABQ0AT	64 KB	35	8	-	LQFP-48
PSC1M2EBABQ0AT	128 KB	35	8	-	LQFP-48
PSC1M2FBABQ0AT	200 KB	35	8	-	LQFP-48
PSC1M3DBLGQ0AT	64 KB	34	8	2/32	VQFN-48
PSC1M3EBLGQ0AT	128 KB	34	8	2/32	VQFN-48
PSC1M3FBLGQ0AT	200 KB	34	8	2/32	VQFN-48
PSC1M3DBABQ0AT	64 KB	35	8	2/32	LQFP-48
PSC1M3EBABQ0AT	128 KB	35	8	2/32	LQFP-48
PSC1M3FBABQ0AT	200 KB	35	8	2/32	LQFP-48

7.1 Chip identification number

The chip identification number allows software to identify the marking. It is an eight-word value with the most significant seven words stored in flash configuration sector 0 (CS0) at address location: 1000 0F00H (MSB) - 1000 0F1BH (LSB). The least significant word and most significant word of the chip identification number are the value of registers DBGROMID and IDCHIP, respectively.

Table 33 Chip identification number

Derivative	CHIP ID	Marking
PSC1M2DBTBQ0AT	000C1013 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083_H	AT
PSC1M2EBTBQ0AT	000C1013 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083_H	AT
PSC1M2FBTBQ0AT	000C1013 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083_H	AT
PSC1M2DBLEQ0AT	000C1043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00011000 10204083_H	AT

(table continues...)

Table 33 (continued) Chip identification number

Derivative	CHIP ID	Marking
PSC1M2EBLEQ0AT	000C1043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00021000 10204083_H	AT
PSC1M2FBLEQ0AT	000C1043 07FF00FF 1E071FF7 000F900F 00000D00 00001000 00033000 10204083_H	AT
PSC1M2DBLGQ0AT	000C1083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083_H	AT
PSC1M2EBLGQ0AT	000C1083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083_H	AT
PSC1M2FBLGQ0AT	000C1083 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083_H	AT
PSC1M2DBABQ0AT	000C10B3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00011000 10204083_H	AT
PSC1M2EBABQ0AT	000C10B3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00021000 10204083_H	AT
PSC1M2FBABQ0AT	000C10B3 07FF00FF 1E071FF7 100F900F 00000D00 00001000 00033000 10204083_H	AT
PSC1M3DBLGQ0AT	000C1083 07FF00FF 1E071FF7 10BF900F 00000D00 00001000 00011000 10204083_H	AT
PSC1M3EBLGQ0AT	000C1083 07FF00FF 1E071FF7 10BF900F 00000D00 00001000 00021000 10204083_H	AT
PSC1M3FBLGQ0AT	000C1083 07FF00FF 1E071FF7 10BF900F 00000D00 00001000 00033000 10204083_H	AT
PSC1M3DBABQ0AT	000C10B3 07FF00FF 1E071FF7 10BF900F 00000D00 00001000 00011000 10204083_H	AT
PSC1M3EBABQ0AT	000C10B3 07FF00FF 1E071FF7 10BF900F 00000D00 00001000 00021000 10204083_H	AT
PSC1M3FBABQ0AT	000C10B3 07FF00FF 1E071FF7 10BF900F 00000D00 00001000 00033000 10204083_H	AT

7.2 Part number nomenclature

PSOC™ Control C1 ordering information decoder:

PS C3 A B CC DD E FF G H II J K

Field	Description	Values	Meaning
PS	Brand	PS	Brand
C1	Family	C1	Family
A	Series	P	Power control

Field	Description	Values	Meaning
		M	Motor control
B	Sub-series	Entry Line	1-3
		Main Line	4-6
		Performance Line	7-9
CC	Memory (Flash/SRAM)	A	8 KB
		B	16 KB
		C	32 KB
		D	64 KB
		E	128 KB
		F	256 KB
		G	512 KB
		H	768 KB
		J	1 MB
		K	2 MB
		L	3 MB
		M	4 MB
		N	6 MB
		O	7 MB
		P	8 MB
DD	Security	S2	PSA L2 (PSA certification level)
		S3	PSA L3 (PSA certification level)
E	Special attributes	D	Dual core
		P	Programmable Power Control Subsystem
FF	Package	AB	EQFP-48 (0.5 mm)
		AC	EQFP-64 (0.5 mm)
		AF	EQFP-80 (0.5 mm)
		AH	QFP-100 (0.5 mm)
		AI	QFP-128 (0.5 mm)
		AE	QFP-144 (0.5 mm)
		LB	VQFN-24 (0.5 mm)
		LC	VQFN-32 (0.5 mm)
		LE	VQFN-40 (0.4 mm)
		LF	VQFN-48 (0.35 mm)

Field	Description	Values	Meaning
		LG	VQFN-48 (0.4 mm)
		LH	VQFN-64 (0.4 mm)
		TB	TSSOP-38 (0.5 mm)
G	Temperature	C	Consumer (0°C to +70°C)
		I	Industrial (-40°C to +85°C)
		Q	Extended range (-40°C to +105°C)
H	Maximum core frequency	1	100-199 MHz
		2	200-299 MHz
II	Sample (Optional)	ES	Engineering sample
J	Revision	-	Base
		A	Die revision
K	Packing (Optional)	T	Tape and Reel
		-	Tray

8 Package information

The PSC1M2x and PSC1M3x is a member of the PSOC™ Control C1 family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

8.1 Package parameters

Table 34 provides the thermal characteristics of the packages used in PSOC™ Control C1.

Table 34 Thermal characteristics of the packages

Parameter	Symbol	Limit values		Unit	Package types
		Min	Max		
Exposed die pad dimensions	Ex × Ey CC	–	3.7 × 3.7	mm	PG-VQFN-40-17
		–	4.2 × 4.2	mm	PG-VQFN-48-73
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	–	86.0	K/W	PG-TSSOP-38-9[1)]
		–	45.3	K/W	PG-VQFN-40-17
		–	44.9	K/W	PG-VQFN-48-73
		–	TBD	K/W	PG-LQFP-48-10

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

***Note**: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.*

8.2 Thermal considerations

When operating the PSOC™ Control C1 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$" quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115°C.

The difference between junction temperature and ambient temperature is determined by

$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as

$P_{IOSTAT} = \Sigma((V_{DDP}\text{-}V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system

- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

8.3 Package outlines

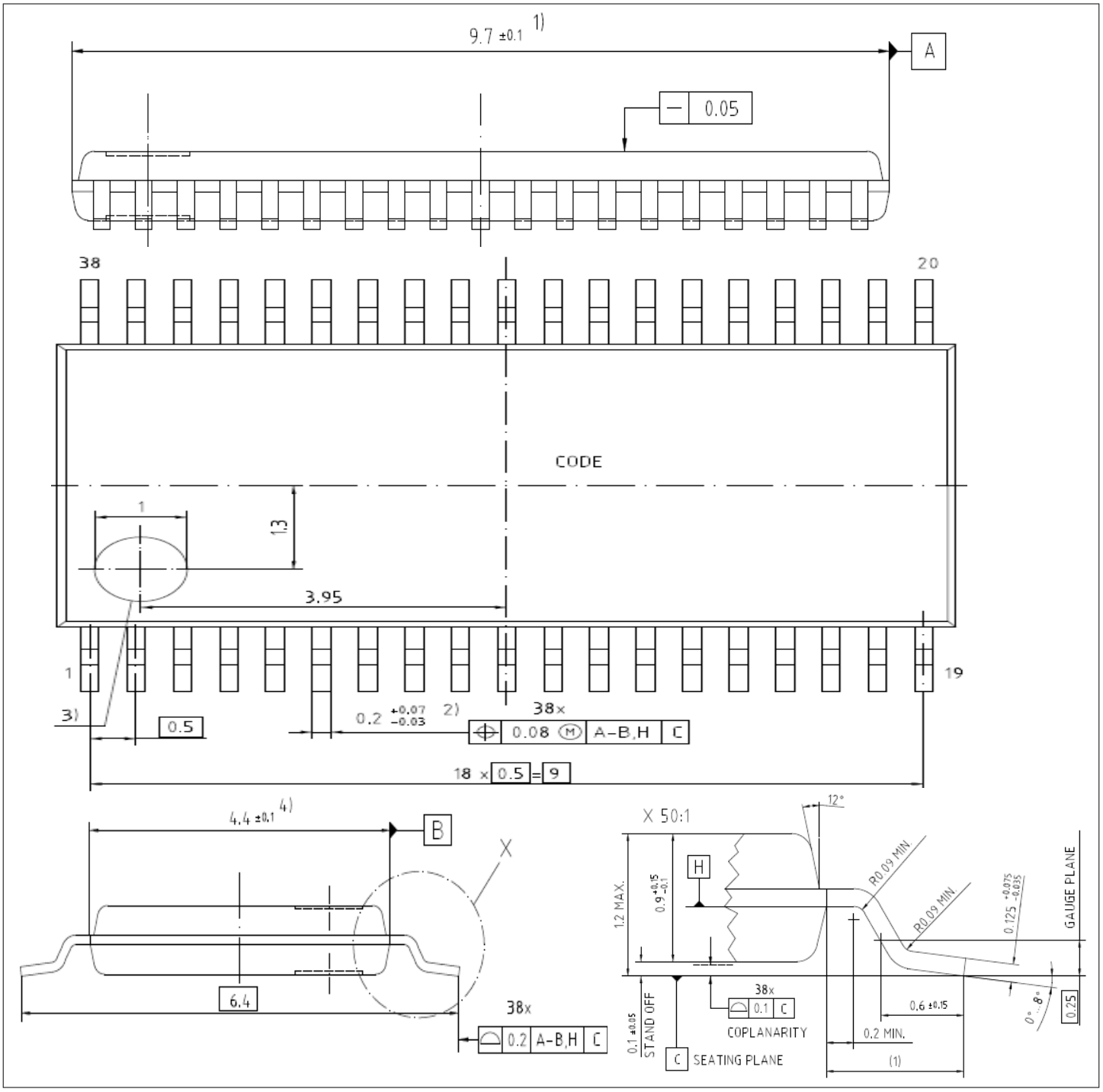


Figure 25 PG-TSSOP-38-9

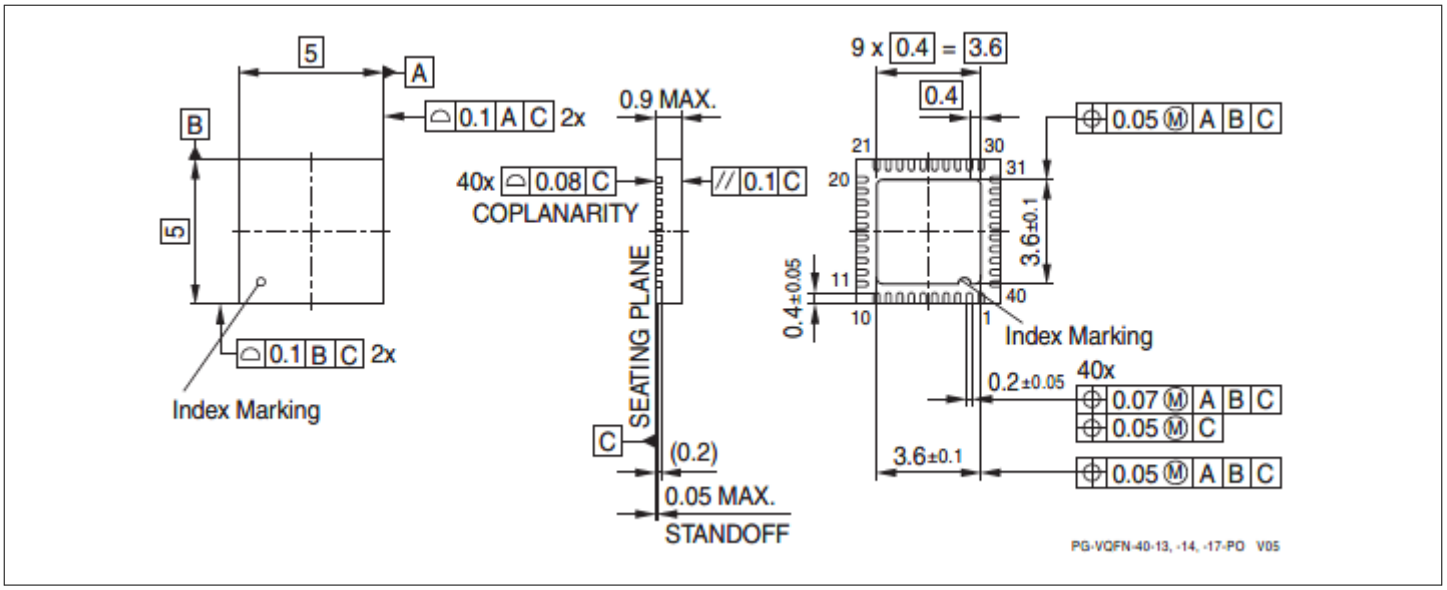


Figure 26 PG-VQFN-40-17

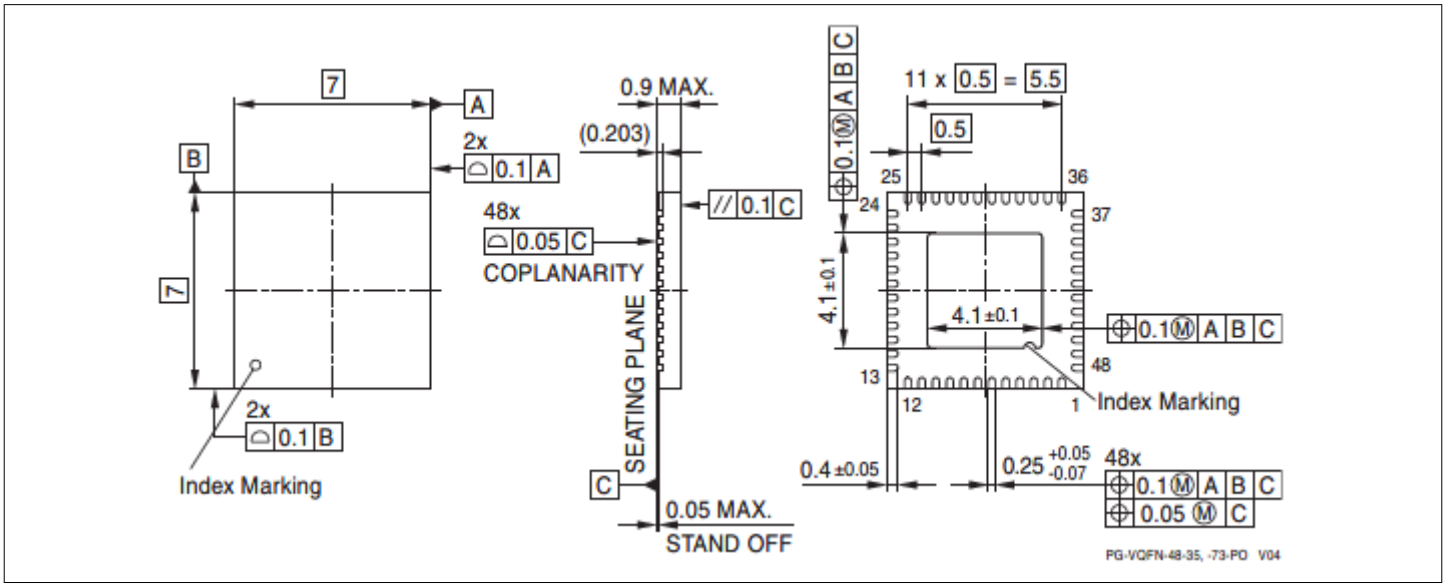


Figure 27 PG-VQFN-48-73

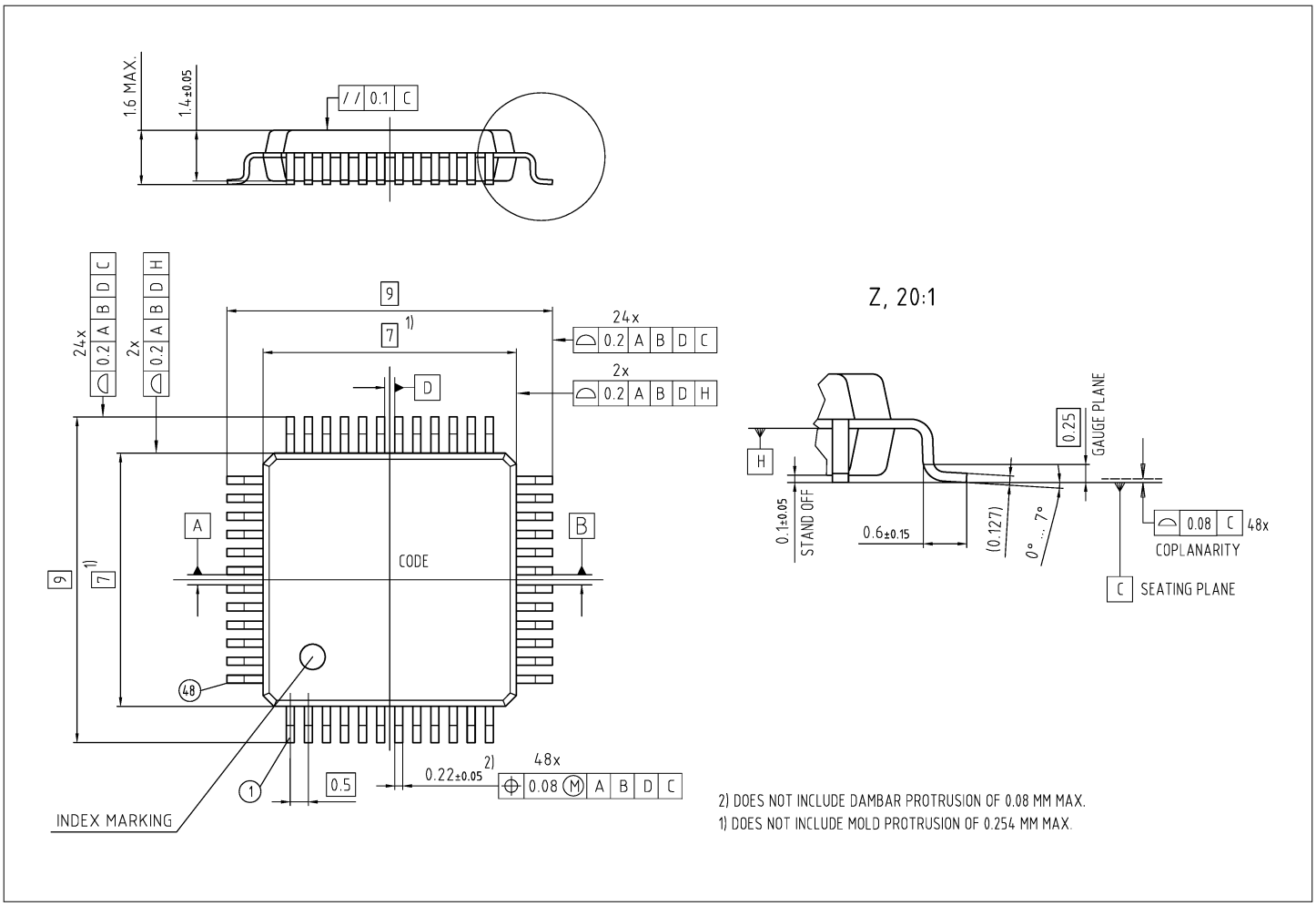


Figure 28 PG-LQFP-48-10

All dimensions in mm.

9 Acronyms

Table 35 Acronyms used in the document

ACMP	analog comparator
AHB	Advanced High-performance Bus
AMBA	Advanced microcontroller Bus Architecture
ANACTRL	Analog Control Unit
APB	Advanced Peripheral Bus
ASC	asynchronous serial channel
BCCU	Brightness and Colour Control Unit
BMI	Boot Mode Index
CMSIS	Cortex® microcontroller Software Interface Standard
CPU	central processing unit
CCU4	Capture Compare Unit 4
CCU8	Capture Compare Unit 8
CRC	cyclic redundancy code
DCO	digitally controlled oscillator
ECC	error correction code
ERU	Event Request Unit
EVR	embedded voltage regulator
FPU	floating point unit
GPIO	general purpose input/output
HMI	human-machine interface
IIC	Inter-Integrated Circuit (I2C)
IIS	Inter-IC Sound Interface
I/O	input/output
JTAG	Joint Test Action Group = IEEE1149.1
LED	light emitting diode
MSB	most significant bit
NC	not connected
NMI	non-maskable interrupt
NVIC	Nested Vectored Interrupt Controller
ORC	out-of-range comparator
PAU	Peripheral Access Unit
POSIF	Position Interface
PRNG	pseudorandom number generator

(table continues...)

Table 35 (continued) Acronyms used in the document

ROM	Read-Only Memory
RAM	Random Access Memory
RTC	real-time clock
SCU	System Control Unit
SFR	Special Function register
SHS	sample-and-hold sequencer
SPI	Serial Peripheral Interface
SRAM	Static RAM
SR	service request
SSC	synchronous serial channel
SSW	start-up software
TSE	temperature sensor
UART	Universal Asynchronous Receiver Transmitter
USIC	Universal Serial Interface Channel
VADC	versatile analog-to-digital converter
WDT	watchdog timer

10 Document conventions

10.1 Units of measure

Table 36 Units of measure

Symbol	Unit of measure
°C	degree Celsius
KB	1024 bytes
kHz	kilohertz
Mbps	megabits per second
Msps	million samples per second
MHz	megahertz
ns	nanosecond
%	percent
V	volt

Revision history

Document revision	Date	Description of changes
**	2026-06-25	Initial release.

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