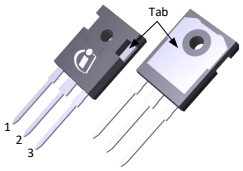
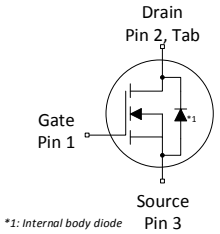
MOSFET

PG-TO247-3

650V CoolMOS™ CM8 Power Transistor

The CoolMOS™ 8th generation platform is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The 650V CoolMOS™ CM8 series is the successor to the 650V CoolMOS™ 7 Family and is enhancing Infineon's WBG offering. It combines the benefits of a fast switching SJ MOSFET with excellent ease of use, e.g low ringing tendency, implemented fast body diode (CFD) for all products with outstanding robustness against hard commutation and excellent ESD capability. Furthermore, extremely low switching and conduction losses of CM8, make switching applications even more efficient.





Features

- Best in class 650V SJ MOSFET performance
- Suitable for hard and soft switching topologies thanks to an outstanding commutation ruggedness
- Integrated fast body diode and ESD protection
- .XT interconnection technology for best in class thermal performance

Benefits

- Ease of use and fast design-in through low ringing tendency and usage across PFC and PWM stages
- Simplified thermal management due to our advanced die attach technique
- Increased power density solutions enabled by using products with smaller footprint and higher manufacturing quality due state of the art ESD protection
- Suitable for a wide variety of applications and power ranges

Potential applications

- Power supplies and converters
- PFC stages & LLC resonant converters
- High efficiency switching applications
- e.g. Datacenter, AI Server, Telecom Power Supply

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	60	mΩ
$Q_{g,typ}$	52	nC
$I_{D,pulse}$	148	A
E_{oss} @ 400V	6.0	µJ
Body diode di_F/dt	1300	A/µs
ESD class (HBM)	2	

Part number	Package	Marking	Related links
IPW65R060CM8	PG-TO247-3	65R060C8	see Appendix A

Table of contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	45	A	T_C=25°C
				28		T_C=100°C
Pulsed drain current [2]	$I_{D,pulse}$	-	-	148	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	87	mJ	I_D=3.7A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}			0.44		
Avalanche current, single pulse	I_{AS}	-	-	3.7	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	227	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j					
Extended operating junction temperature	T_j	150	-	175	°C	≤50 h in the application lifetime
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	45	A	T_C=25°C
Diode pulse current [2]	$I_{S,pulse}$			148		
Reverse diode dv/dt [3]	dv/dt	-	-	70	V/ns	V_{DS}=0...400V, I_{SD}≤45A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt			1300	A/µs	
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j,max}$

[2] Pulse width t_p limited by $T_{j,max}$

[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.55	K/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	K/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	K/W	-
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.7	4.2	4.7	V	V_{DS}=V_{GS}, I_D=0.44mA
Zero gate voltage drain current	I_{DSS}	-	-	1	µA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
			52.6	-		V_{DS}=650V, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	0.1	µA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.051	0.060	Ω	V_{GS}=10V, I_D=16.7A, T_j=25°C
			0.113	-		V_{GS}=10V, I_D=16.7A, T_j=150°C
Gate resistance	R_G	-	6	-	Ω	f=1MHz

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2462	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}		29			
Effective output capacitance, energy related [4]	$C_{o(er)}$	-	75	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related [5]	$C_{o(tr)}$	-	813	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	25.3	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=8.7A, R_G=5.3Ω; see table 9
Rise time	t_r		6.5			
Turn-off delay time	$t_{d(off)}$		92.5			
Fall time	t_f		7.1			

[4] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

[5] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 6 Gate charge characteristics

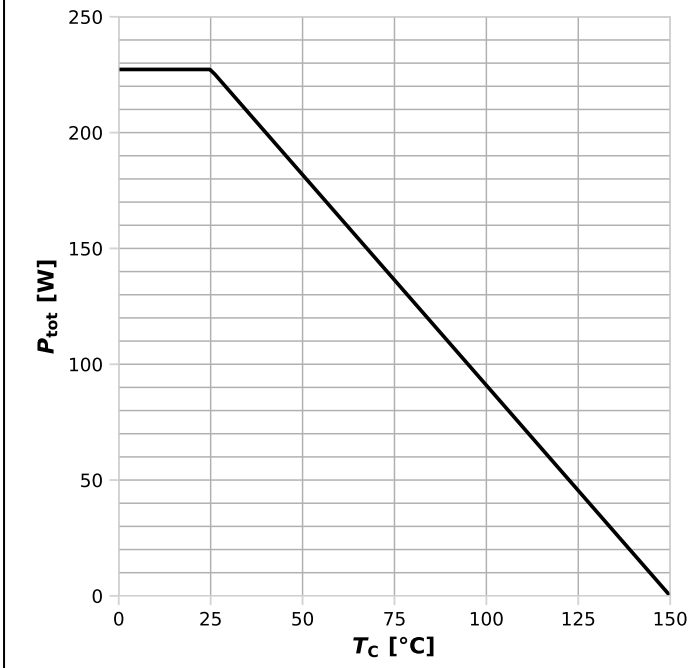
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	14	-	nC	V_{DD}=400V, I_D=8.7A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}		16		nC	
Gate charge total	Q_g		52		nC	
Gate plateau voltage	$V_{plateau}$		5.8		V	

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=8.7A, T_j=25°C
Reverse recovery time	t_{rr}	-	98	122.3	ns	V_R=400V, I_F=8.7A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}		0.48	0.72	µC	
Peak reverse recovery current	I_{rrm}		10.2	-	A	

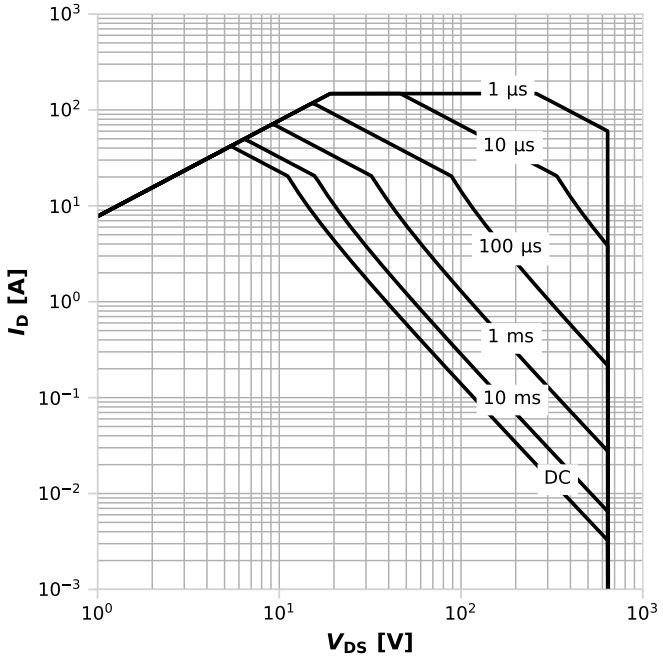
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



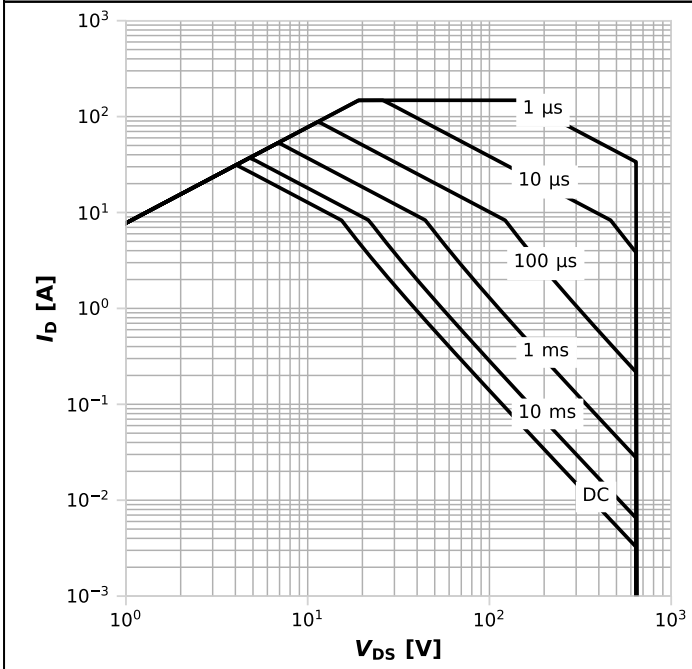
P_{tot}=f(T_C)

Diagram 2: Safe operating area



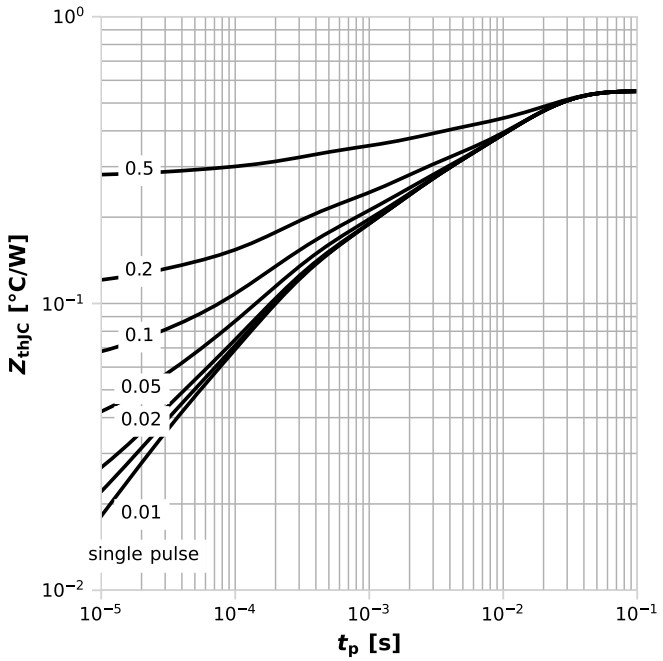
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC} =f(t_P); parameter: D=t_p/T

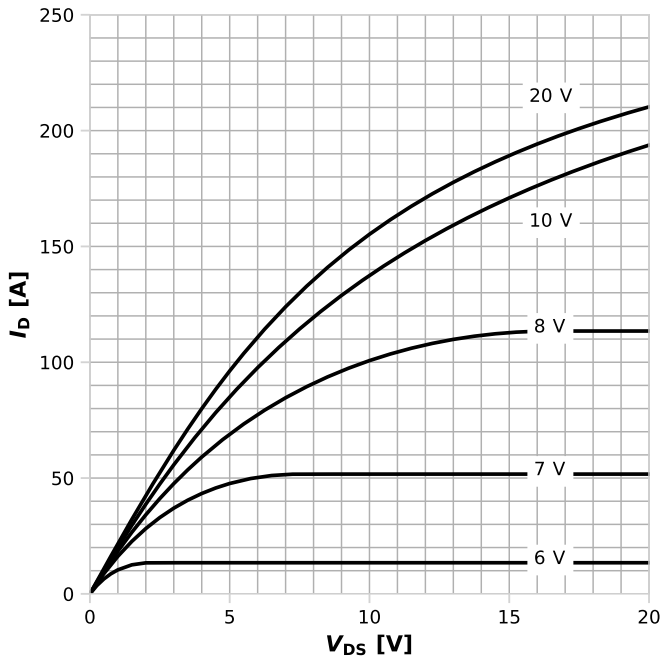
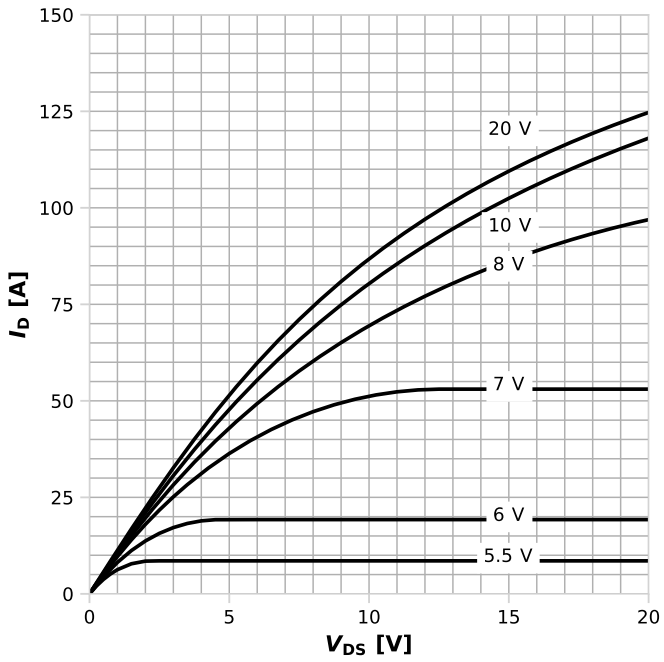
Diagram 5: Typ. output characteristics	Diagram 6: Typ. output characteristics
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

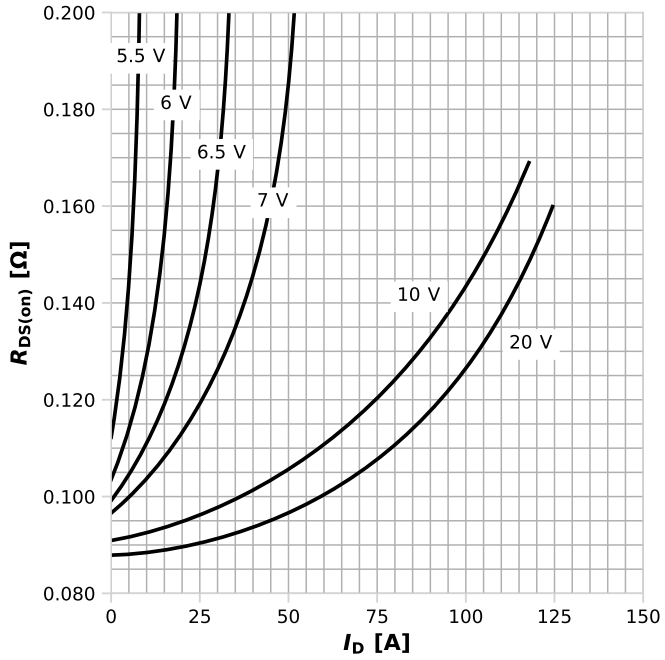
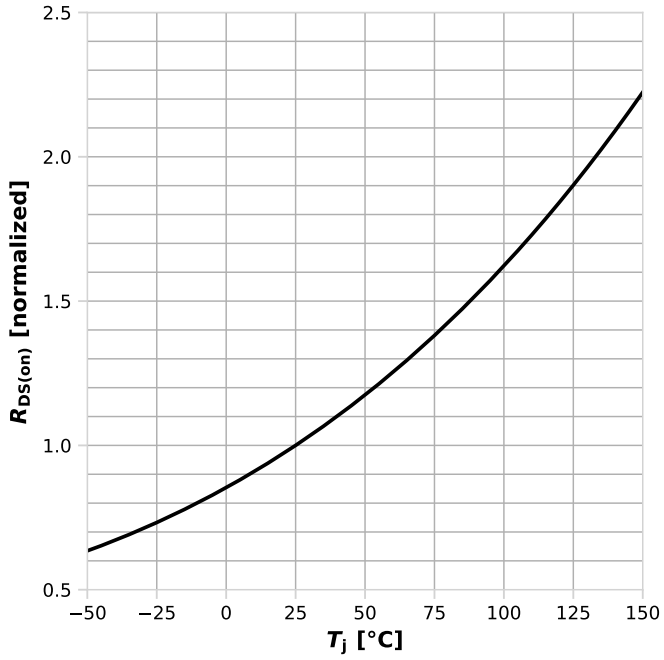
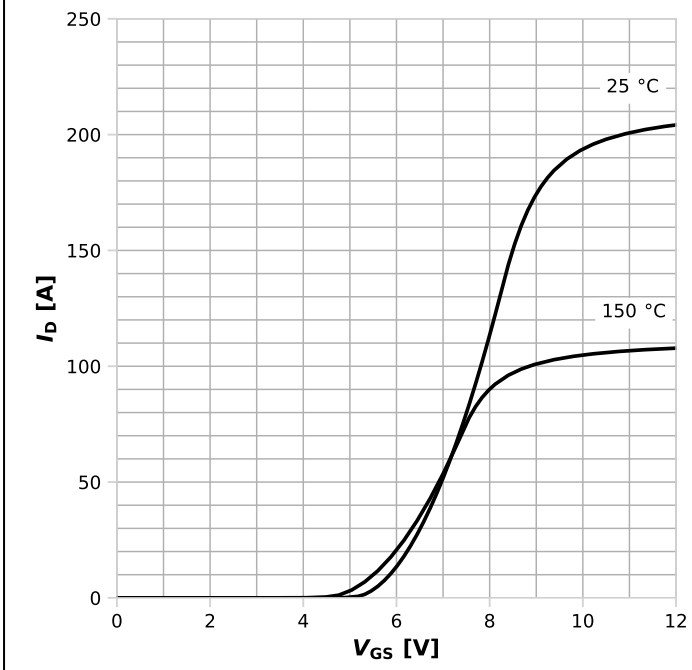
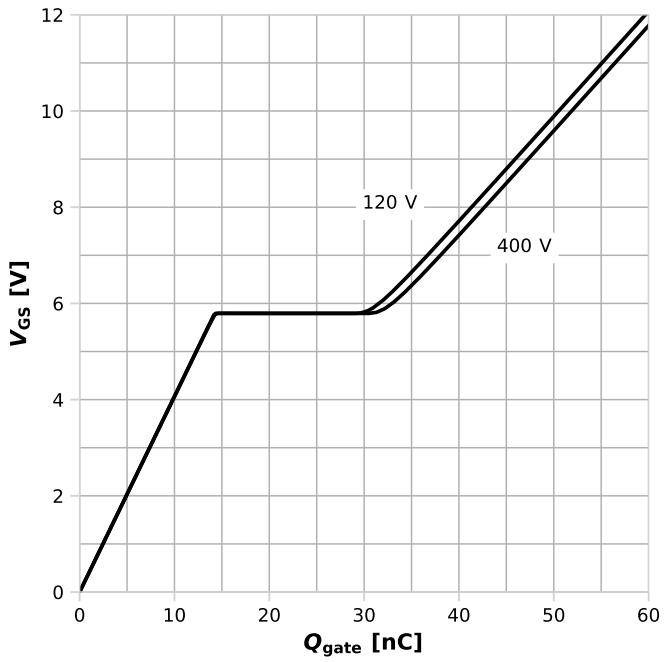
Diagram 7: Typ. drain-source on-state resistance	Diagram 8: Drain-source on-state resistance
	
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}	$R_{DS(on)}$=f(T_j); I_D=16.7 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



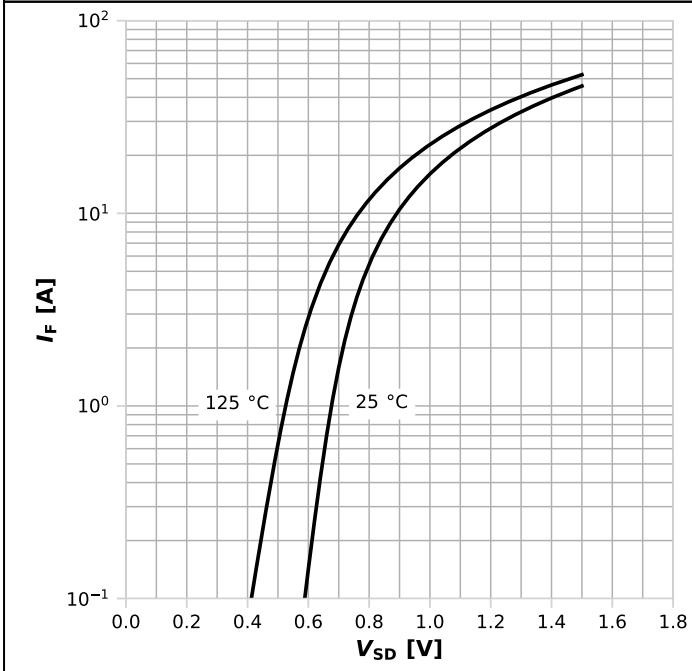
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



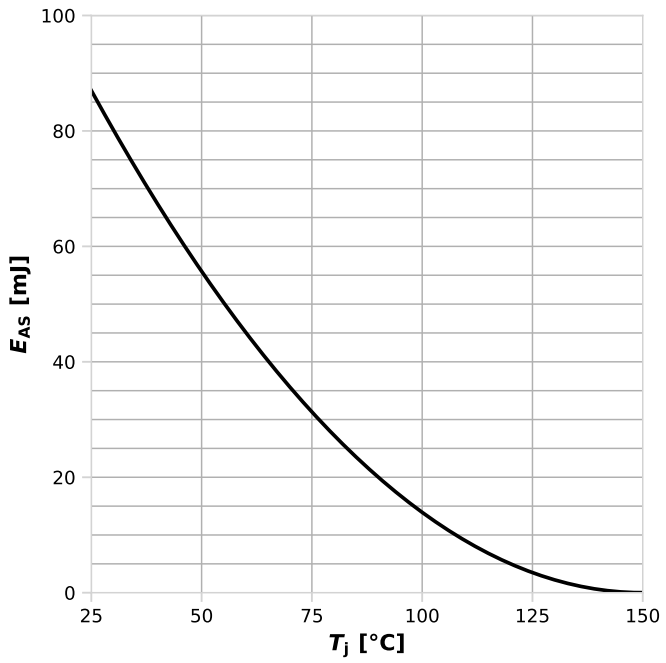
V_{GS}=f(Q_{gate}); I_D=8.7 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



E_{AS}=f(T_j); I_D=3.7 A; V_{DD}=50 V

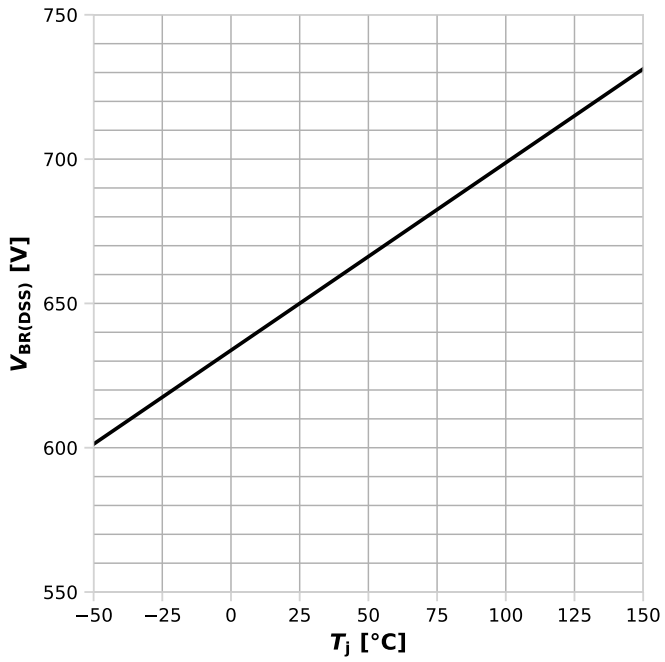
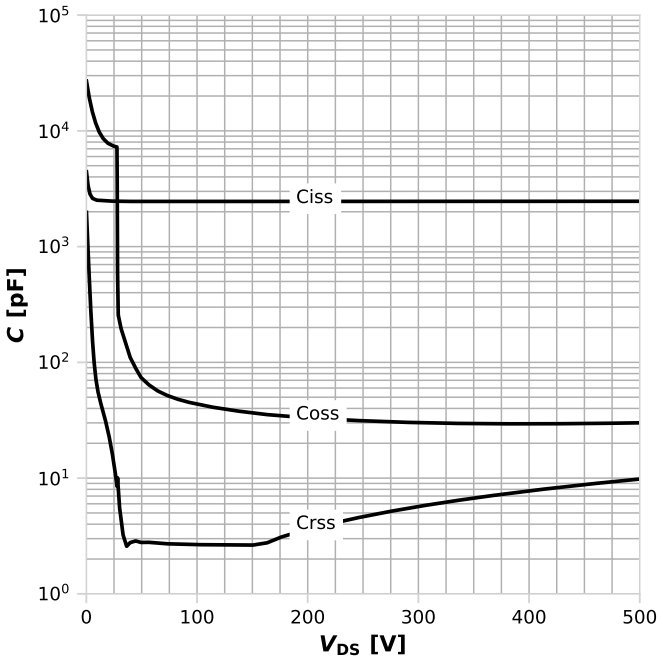
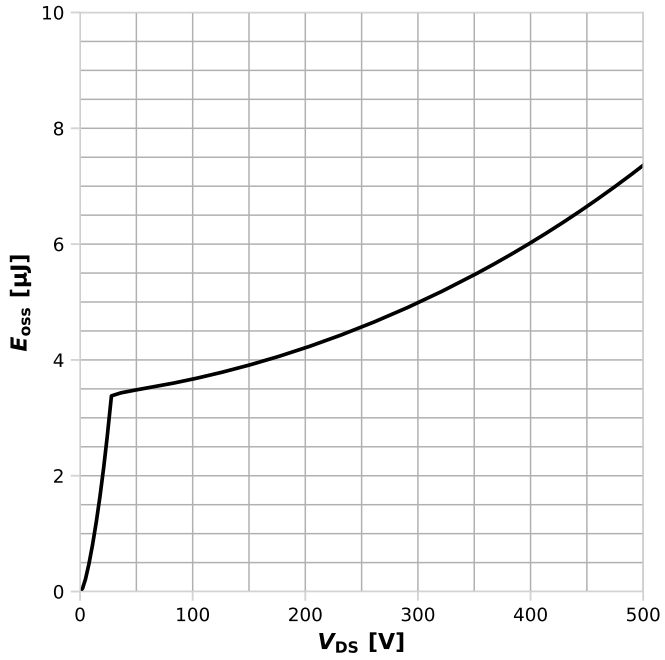
Diagram 13: Drain-source breakdown voltage	Diagram 14: Typ. capacitances
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy

E_{oss}=f(V_{DS})

5 Test circuits

Table 8 Diode characteristics

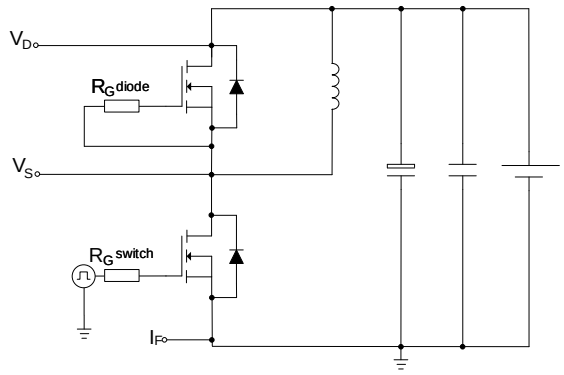
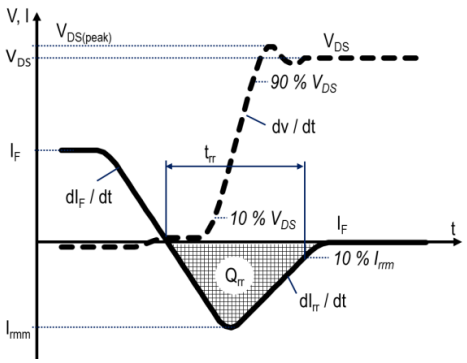
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

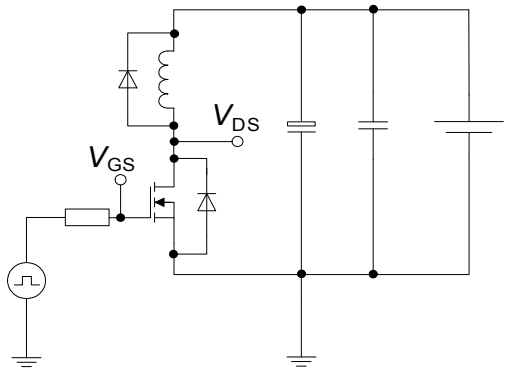
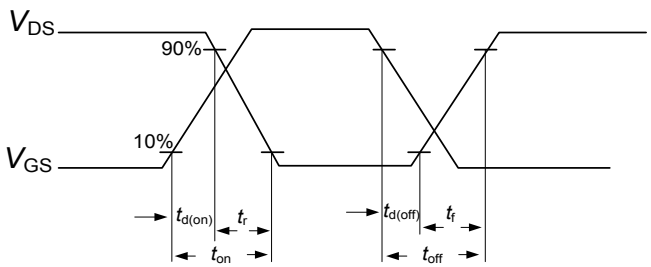
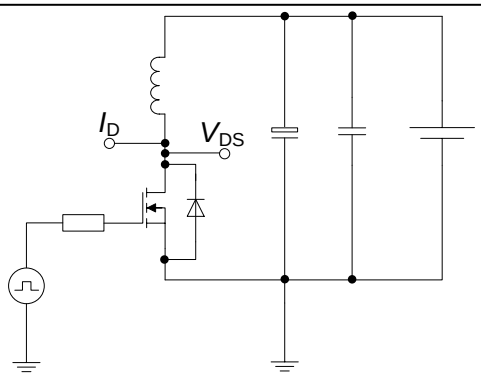
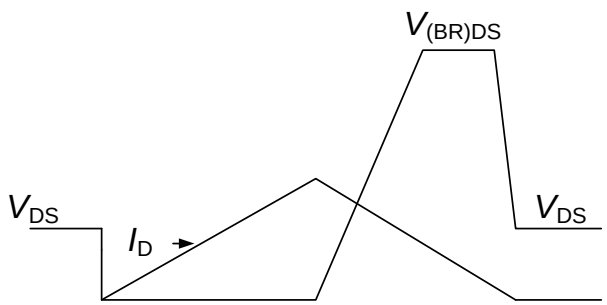
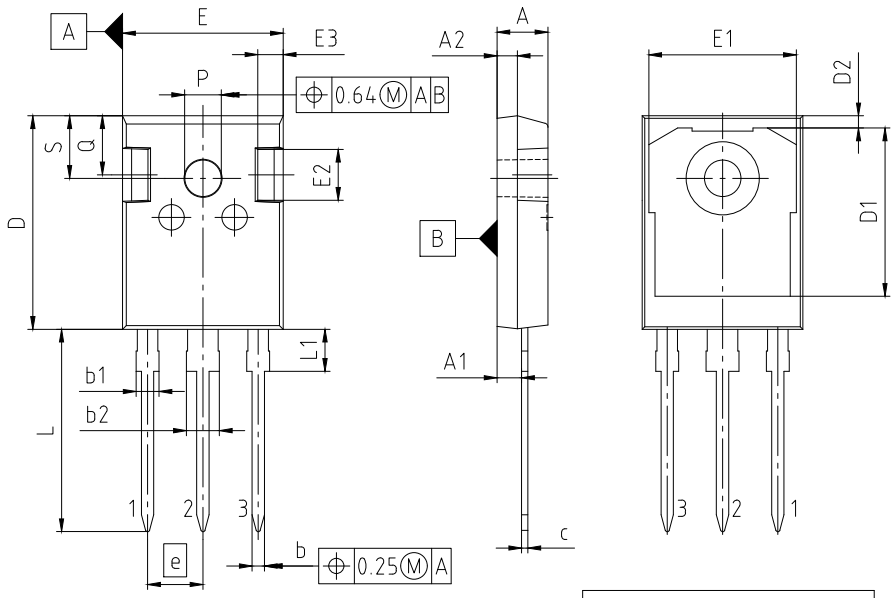
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO247-3-U06	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.83	5.21
A1	2.27	2.54
A2	1.85	2.16
b	1.07	1.33
b1	1.90	2.41
b2	2.87	3.38
c	0.55	0.68
D	20.80	21.10
D1	16.25	17.65
D2	0.95	1.35
E	15.70	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	2.60
e	5.44	
N	3	
L	19.80	20.32
L1	3.95	4.47
øP	3.50	3.70
Q	5.49	6.00
S	6.04	6.30

NOTE:
DIMENSIONS DO NOT INCLUDE MOLDFLASH; PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TO247-3, dimensions in mm

7 Appendix A

Table 11 Related links

- IFX CoolMOS CM8 Webpage
- IFX CoolMOS CM8 application note
- IFX CoolMOS CM8 simulation model
- IFX Design tools

Revision history

IPW65R060CM8

Revision 2025-03-07, Rev. 2.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2024-12-19	Release of final
2.1	2025-03-07	Update of maximum transient thermal impedance and SOA

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