APEX MICROTECHNOLOGY
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PA166

Dual High Voltage Power Operational Amplifier

RoHS COMPLIANT

FEATURES

- Monolithic MOS Technology for Amplifier Core
- High Voltage Operation (200V Output)
- Current Limit with Over-current Flag
- Configurable as Bridge or Parallel (optional)
- High Output Current 4A Peak
- Amplifier Disable feature
- Low Cost

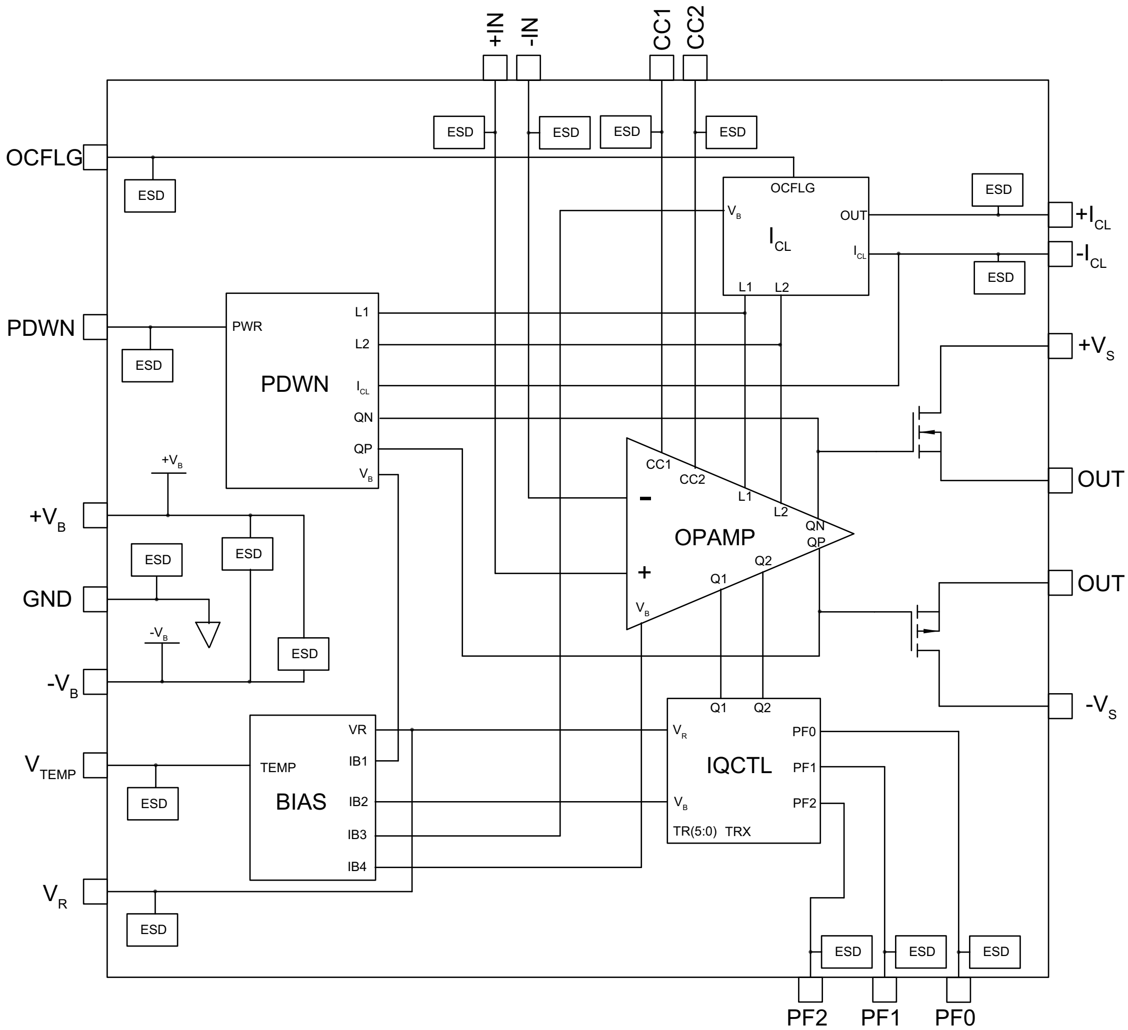
APPLICATIONS

- High Density Voltage or Current Supplies
- Electrostatic Transducer and Deflection
- Deformable Mirror Focusing
- Piezo Electric Positioning

DESCRIPTION

The PA166 is a dual high voltage monolithic operational amplifier. The PA166 houses two independent 200V, 4A peak operational amplifier (PA164) circuits within a 52 pin QFP package. Each channel consists of a monolithic IC input stage and an accompanying MOSFET push-pull output stage. This architecture favors high density power applications with large output current or voltage swing demands. Both independent channels are designed for operation up to 200V while providing 4A amp of peak output current. High package pin count allows for separate voltage supply pins for the amplifier IC and the output stage to optimize the overall power dissipation in each channel. Each channel offers a wide-range temperature compensated current limit. An over-current flag as well as an output disable function allow for optional implementation of system protection. Optional external phase compensation provides the user with flexibility in creating optimum gain and bandwidth conditions for their application.

Figure 1: PA166 Block Diagram (Single Channel)



PINOUT DESCRIPTION TABLE

Pin Number	Name	Description
1, 4, 27, 30	NIC	Pins are not connected internally
2, 3	$-V_S$_A	Negative supply voltage pin for A channel
5	$-V_B$_A	Negative boost voltage pin for A channel
6	CC2_A	Compensation capacitor pin for A channel. Connect a compensation capacitor from this pin to ground
7	CC1_A	Compensation capacitor pin for A channel. Connect a compensation capacitor from this pin to ground
8	-IN_A	Inverting input pin for A channel
9	+IN_A	Non - inverting pin for A channel
10	V_R_A	Pin connected to an internal 5V reference. Connect a 0.1µF bypass capacitor between this pin and GND. Do not use this pin as a reference for external components
11	VTMP_A	Temperature sensor output pin for A channel
12	PDWN_A	Power down pin for A channel
13	OCFLG_A	Over current flag for A channel. High = No current limit, Low = Current limit (Must be connected to 5V source through 5K resistor)
14,17,18,19,40,43,44,45	NC	No connection pin. Do not connect anything to the pin
15, 16	GND_A	Amplifier ground connection for A channel
20	$+V_B$_B	Positive boost voltage pin for B channel
21, 22	$+V_S$_B	Positive supply voltage pin for B channel
23	+ILIM_B	Positive current limit sense pin for B channel. Connect this pin to DUT side of the current limit resistor. Refer to typical connection figure
24	-ILIM_B	Negative current limit sense pin for B channel. Connect this pin to load side of the current limit resistor. Refer to typical connection figure
25, 26	OUT_B	Output current sourcing pins for B channel
28, 29	$-V_S$_B	Negative supply voltage pin for B channel
31	$-V_B$_B	Negative boost voltage pins for B channel
32	CC2_B	Compensation capacitor pin for B channel. Connect a compensation capacitor from this pin to ground
33	CC1_B	Compensation capacitor pin for B channel. Connect a compensation capacitor from this pin to ground
34	-IN_B	Inverting input pin for B channel
35	+IN_B	Non - inverting input pin for B channel
36	V_R_B	Pin connected to an internal 5V reference. Connect a 0.1µF bypass capacitor between this pin and GND. Do not use this pin as a reference for external components
37	VTMP_B	Temperature sensor output pin for B channel
38	PDWN_B	Power down pin for B channel

39	OCFLG_B	Over current flag for A channel. High = No current limit, Low = Current limit (Must be connected to 5V source through 5K resistor)
41, 42	GND_B	Amplifier ground connection for B channel
46	$+V_B$_A	Positive boost voltage pin for A channel
47, 48	$+V_S$_A	Positive supply voltage pin for A channel
49	+ILIM_A	Positive current limit sense pin for A channel. Connect this pin to DUT side of the current limit resistor. Refer to typical connection figure
50	-ILIM_A	Negative current limit sense pin for A channel. Connect this pin to load side of the current limit resistor. Refer to typical connection figure
51, 52	OUT_A	Output current sourcing pins for A channel

Figure 2: Typical Connection

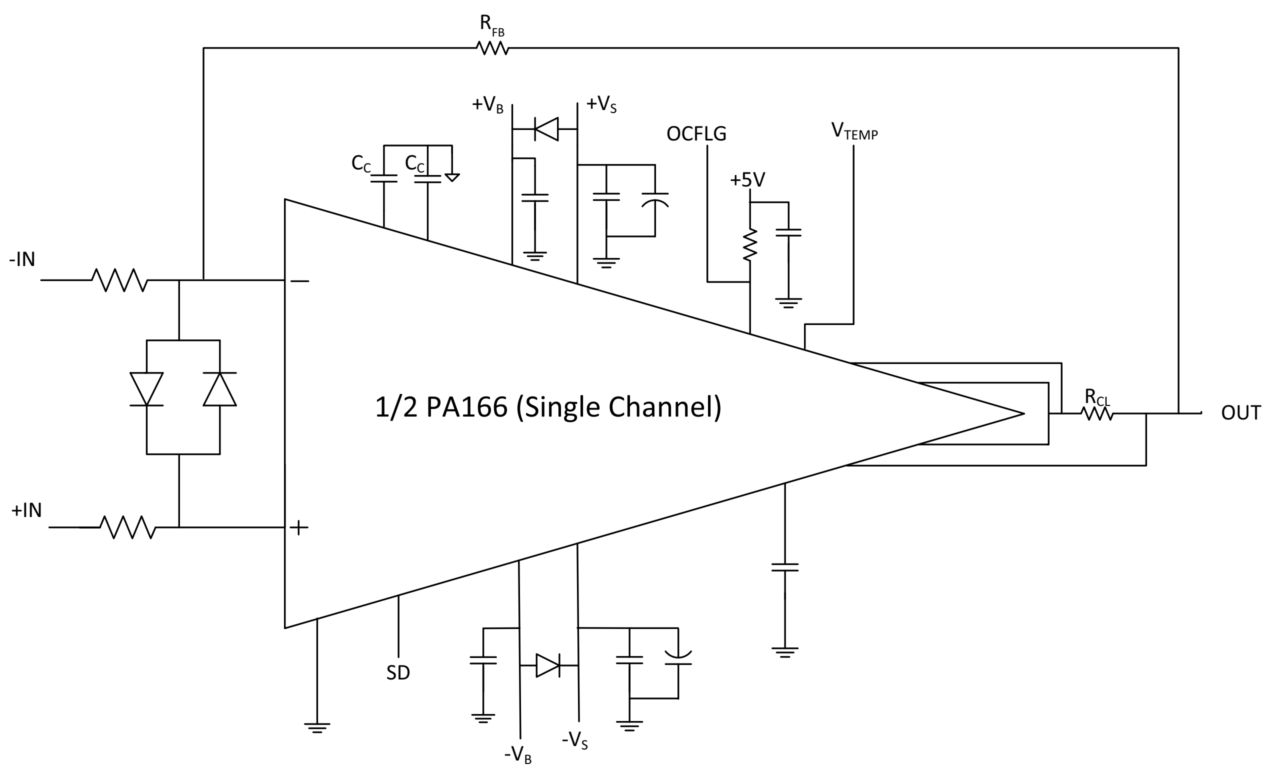


Figure 3: Bridge Configuration

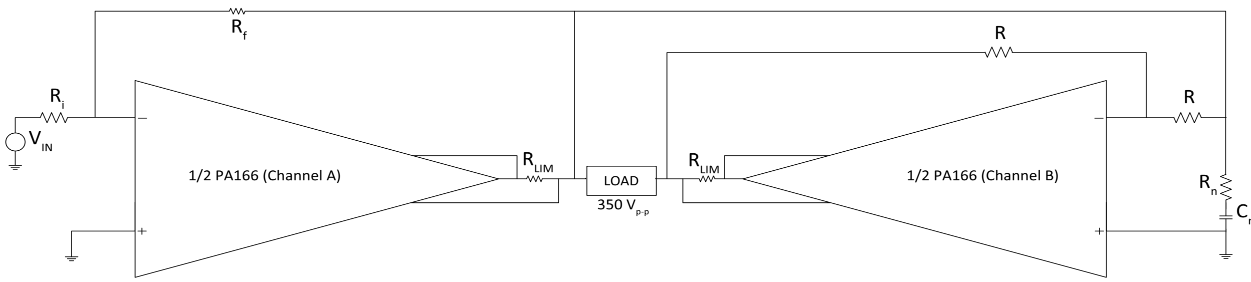
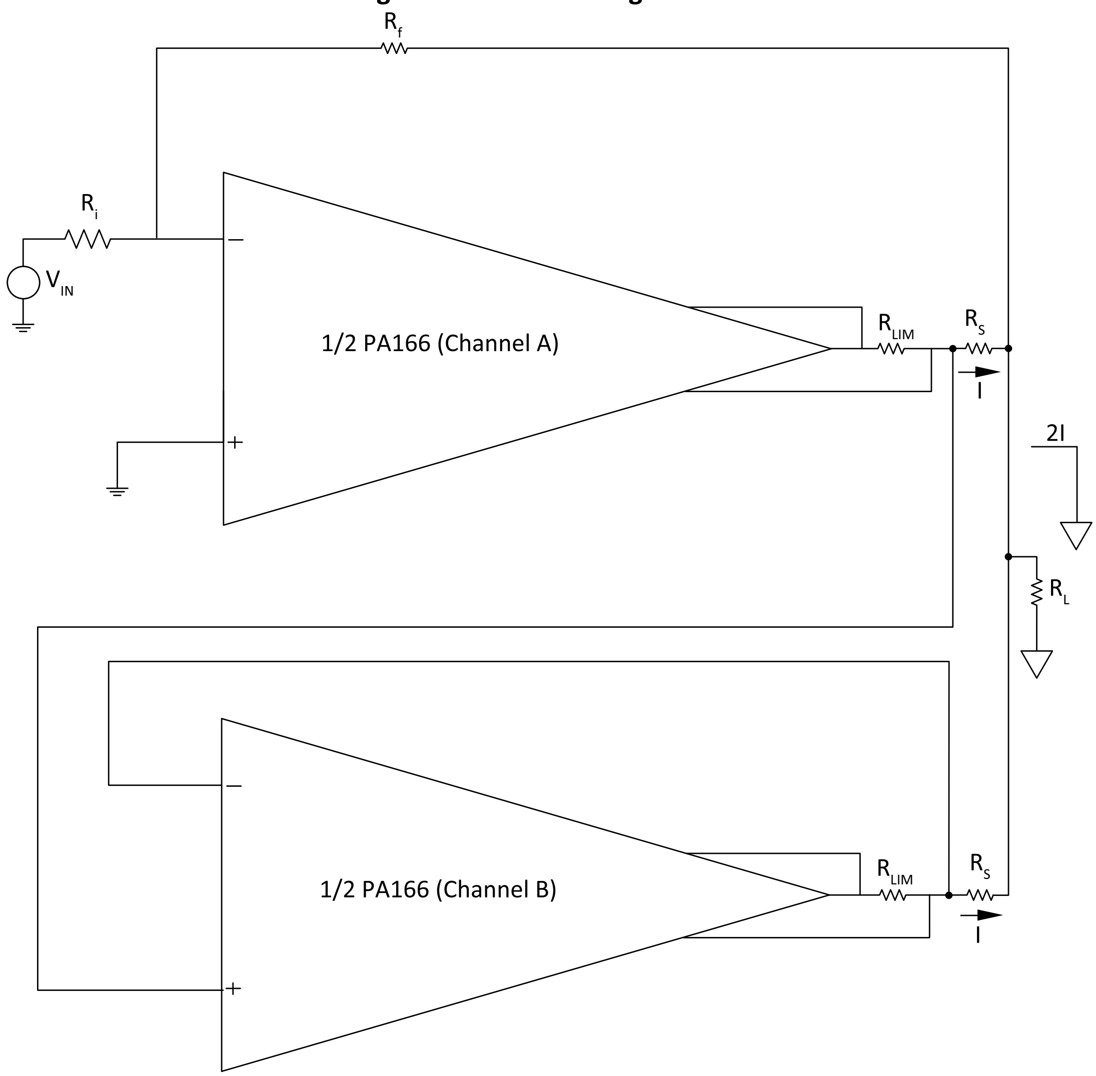


Figure 4: Parallel Configuration



SPECIFICATIONS

Unless otherwise noted; T_C = 25°C, C_{C1} = C_{C2} = 3.3pF. The power supply voltages are set at $\pm V_S$ = ±100V, and $\pm V_B$ = $\pm V_S$. Load R_L = 1 kΩ.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total[1]	$+V_S$ to $-V_S$		205	V
Supply Voltage[2]	$+V_B$	$+V_S$	$+V_S$+15	V
Supply Voltage	$-V_B$	$-V_S$-15	$-V_S$	V
Supply Voltage[3]	$+V_B$ to $-V_B$		235	V
Output Current, peak, within SOA			4	A
Power Dissipation, internal, continuous, per amplifier[4]			28	W
Power Dissipation, internal, continuous, both amplifiers[4]			40	W
Input Voltage, common mode		$-V_B$+10	$+V_B$-10	V
Input Voltage, Differential			±22	V
Peak Reflow Temperature, 30s			250	°C
Temperature, junction			150	°C
Temperature, storage		-40	150	°C
Operating Temperature Range, case		-40	+85	°C

1. Valid only for device temperature of 25°C or higher.
2. The supply of a boost voltage is optional and can be replaced by the general supply voltage ($+V_S$, $-V_S$). Please also note the restriction of the overall supply voltage $+V_B$ to $-V_B$.
3. If V_S is also used for V_B, then the maximum voltage can't exceed the 205V.
4. The case temperature is 25°C

INPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Offset Voltage, initial			-2	±20	mV
Offset Voltage vs. Temperature	-25°C to +85°C		6	250	µV/°C
Offset Voltage vs. Supply			2		µV/V
Offset Voltage vs. Time			80		µV/kh
Bias Current, initial			23	200	pA
Bias Current vs. Supply			2		pA/V
Offset Current, initial			50	200	pA
Input Impedance, DC			10^{11}		Ω
Input Capacitance			3		pF
Common Mode Voltage Range		$-V_B+15$		$+V_B-15$	V
Common Mode Rejection, DC	V_{CM} = ±90V DC	97	115		dB
Noise	1 MHz		13		nV/√Hz

GAIN

Parameter	Test Conditions	Min	Typ	Max	Units
Open Loop @ 15 Hz	R_L=5 kΩ	90	118		dB
Gain Bandwidth Product @ 1 MHz			20		MHz
Power Bandwidth	$150V_{P-P}$		80		kHz

OUTPUT

Parameter	Test Conditions	Min	Typ	Max	Units
Voltage Swing (no boost voltage) $\|V_B\|=\|V_S\|$	I_{OUT}=1A	$+V_S$-10	$+V_S$-8		V
	I_{OUT}=-1A	$-V_S$+10	$-V_S$+6		V
Voltage Swing (with boost voltage, $\|V_B\|=\|V_S\|$+10V)	I_{OUT}=1A	$+V_S$-1.8	$+V_S$-1.3		V
	I_{OUT}=-1A	$-V_S$+2.2	$-V_S$+1.6		V
Current, peak, within SOA		4			A
Current, continuous, within SOA		1			A
Settling Time to 0.1%[1]	10V step, A_V = -10		1.5		µs
Slew Rate[2]	A_V = -10, C_C =0pF		35		V/µs
Slew Rate	A_V = -10, C_C =3.3pF		29		V/µs
Channel Separation	Load = 50Ω Tab to ground		-80		dB

1. Do not exceed SOA when operating with $|V_B|=|V_S|$. Refer to Figure 4 for SOA, and Figure 18, 19 for Output Voltage Swing.
2. Confirmed by design, but not tested in production.

CURRENT LIMIT

Parameter	Test Conditions	Min	Typ	Max	Units
Absolute Accuracy	+25°C to 85°C		10		%
Temperature Dependency	+25°C to 85°C		0.05		%/K
Clamping Settling Time[1]	Short to ground, settling to the ±10% of limit		3		µs
Current Limit Range, PA164[1]		10		1000	mA
Current Limit Delay (OC Flag)	50mA current limit, 10V output voltage, short to ground		600		ns
Current Limit Circuit Input Bias/ Leakage Current			<1		µA

1. Confirmed by design, but not tested in production. Setting current limit below 10mA may damage the part.

POWER SUPPLY

Parameter	Test Conditions	Min	Typ	Max	Units
Supply Voltage V_S=+V_S-(-V_S)		20		205	V
Boost Supply Voltage V_B=+V_B-(-V_B)		30		V_S+30[1]	V
Current, Quiescent			10.5	20	mA

1. Please also note the conditions under ABSOLUTE MAXIMUM RATINGS

THERMAL

Parameter	Test Conditions	Min	Typ	Max	Units
Resistance, AC, junction to case	F≥60 Hz, single amplifier		2.6	3.2	°C/W
Resistance, AC, junction to case	F≥60 Hz, both amplifier		1.5	2.2	°C/W
Resistance, DC, junction to case	F<60 Hz, single amplifier		3.8	4.4	°C/W
Resistance, DC, junction to case	F<60 Hz, both amplifier		2.3	3.1	°C/W
Resistance, junction to air	Full temperature range		34		°C/W
Temperature Range, case	Meet full range specs	-25		+85	°C

TEMPERATURE SENSOR

Parameter	Test Conditions	Min	Typ	Max	Units
Temp Sensor Output Voltage, V_{TEMP}	T_C=25°C	1.8	2	2.2	V
Temp Sensor “Gain”[1]	T_C=25°C to +85°C	14.5	14.7	14.9	mV/°C
Temperature Accuracy	T_C=25°C to +85°C		±2.2		°C

1. Temperature sensor gain confirmed by design but not tested in production.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of the PA166 is not limited by secondary breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flybacks external fast recovery diodes must be used.

Figure 5: PA166 Safe Operating Area (SOA)

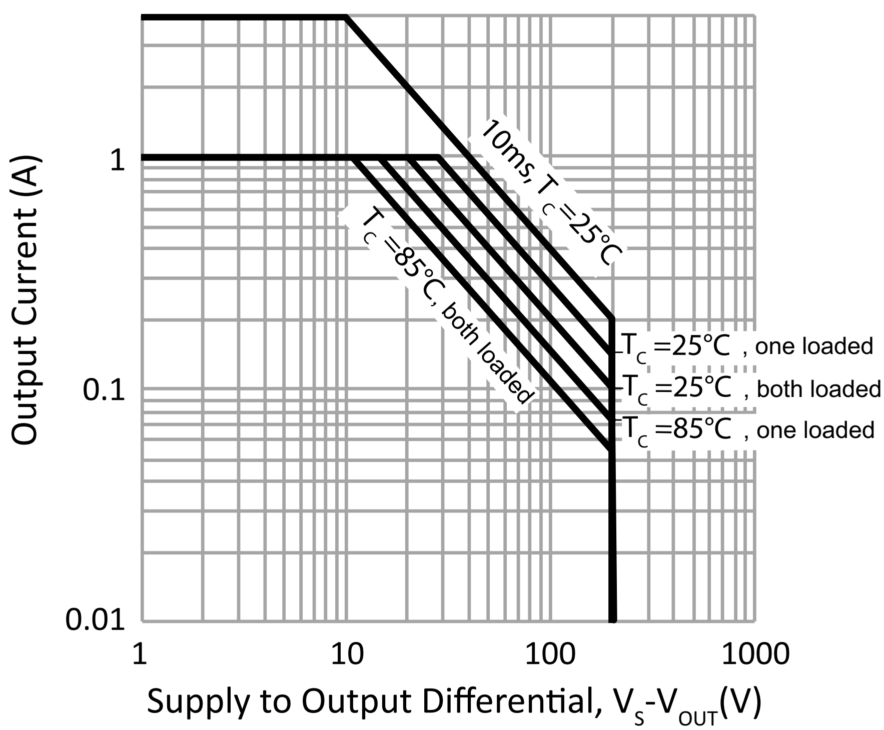


Figure 6: Power Derating

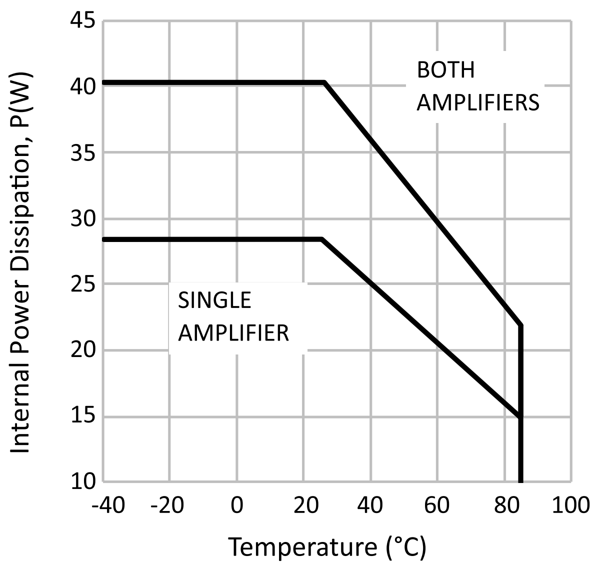


Figure 7: Current Limit vs. Current Limit Resistor

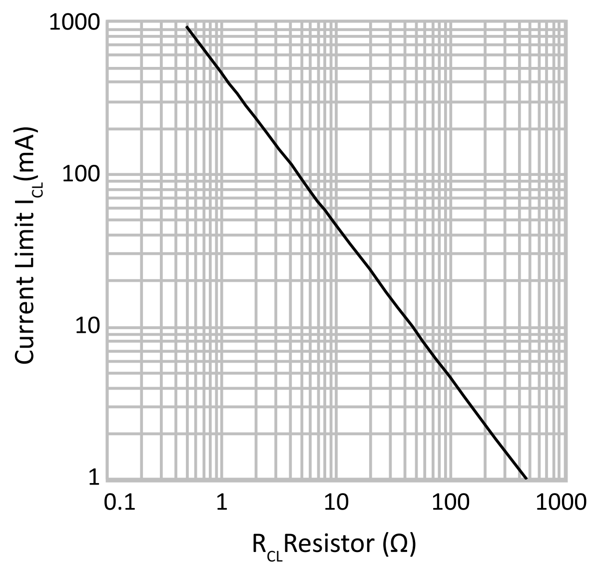


Figure 8: Input Noise

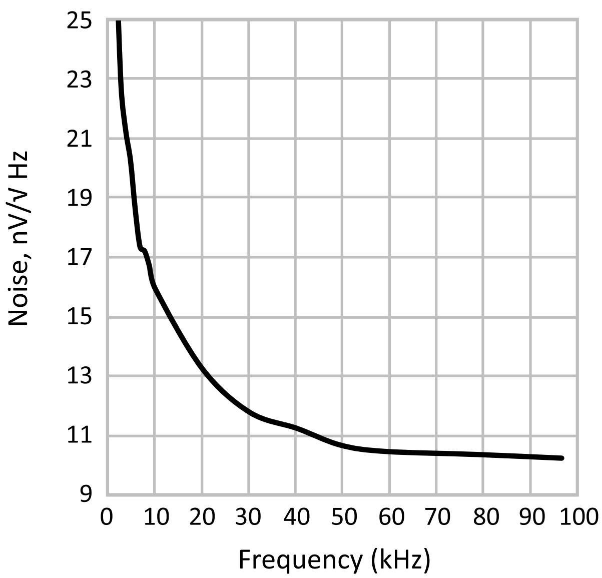


Figure 9: Power Response vs. Compensation

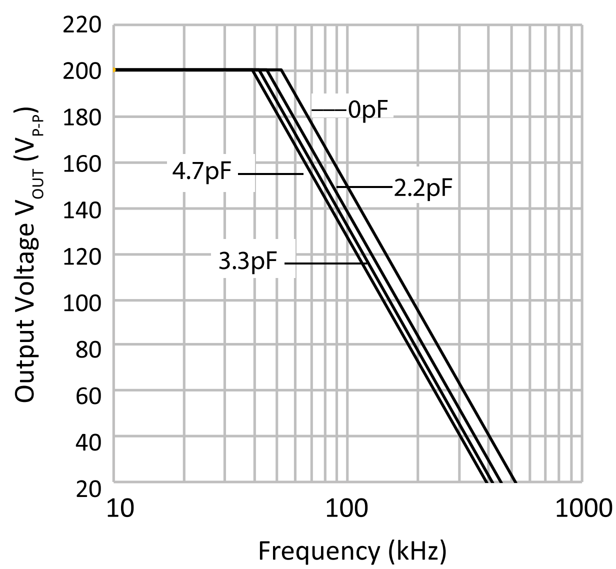


Figure 10: V_{TEMP} vs. Temperature

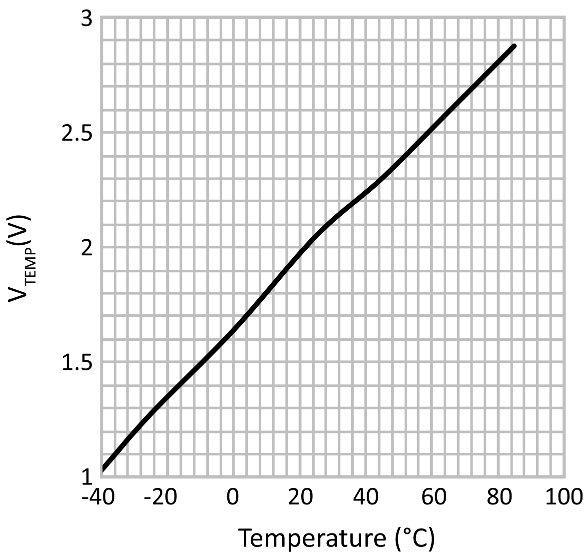


Figure 11: I_Q vs. Supply

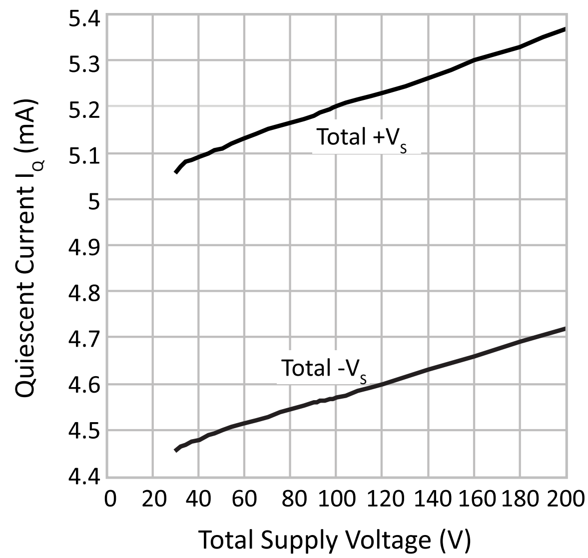


Figure 12: V_S Quiescent Current vs. Temperature

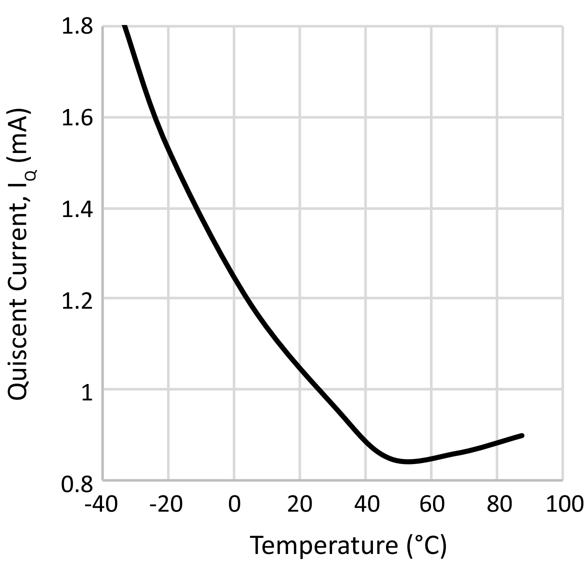


Figure 13: V_B Quiescent Current vs. Temperature

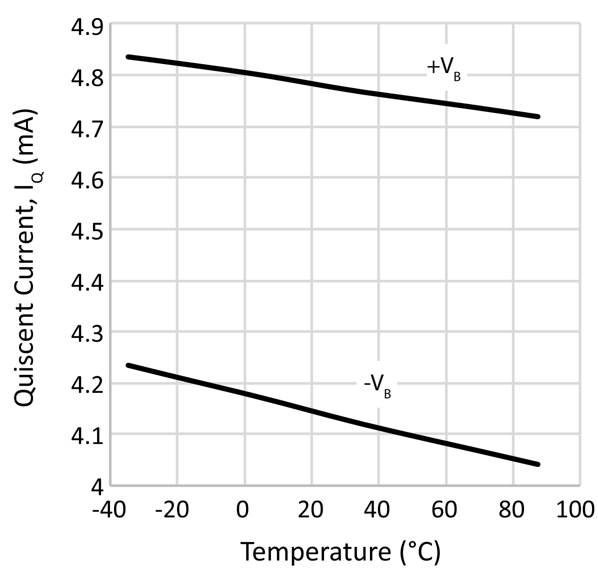


Figure 14: Slew Rate vs. Compensation

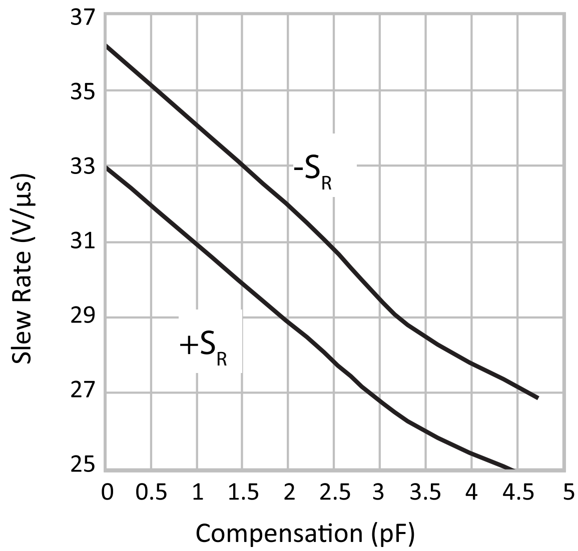


Figure 15: Open Loop Phase Response, C_C = 0pF

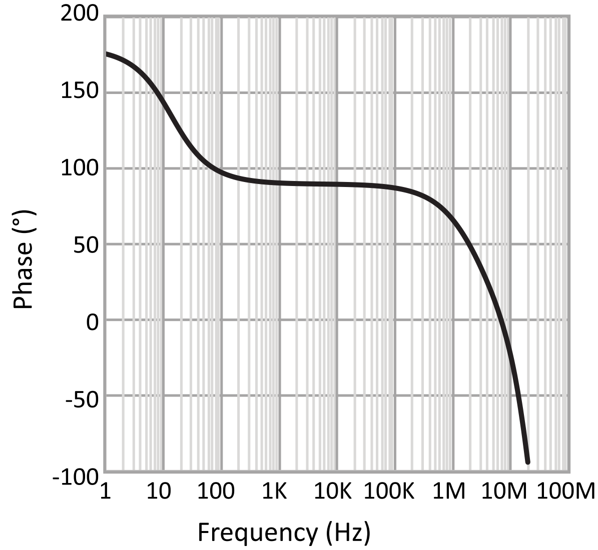


Figure 16: PA164 Open Loop Frequency Response, C_C = 0pF

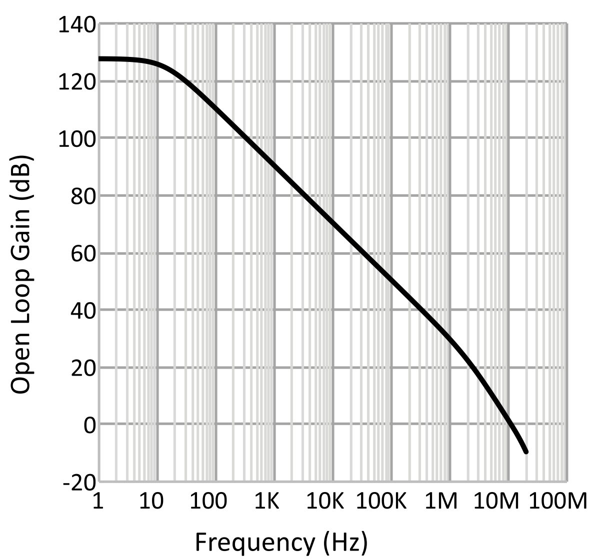


Figure 17: PA164 Output Voltage Swing (with additional boost voltage)

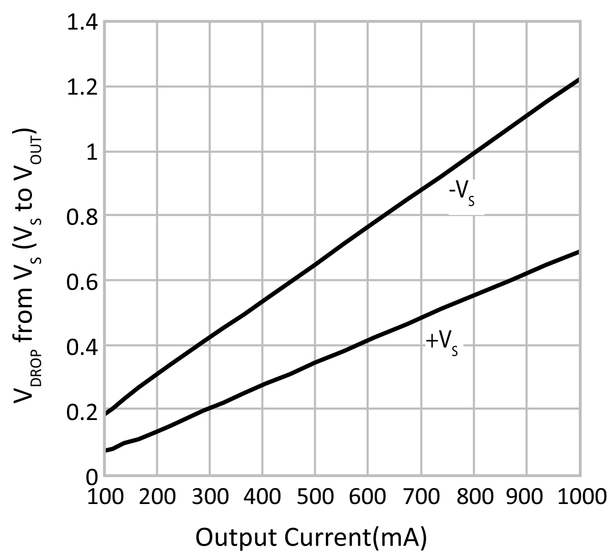


Figure 18: Output Voltage Swing (without additional boost voltage)

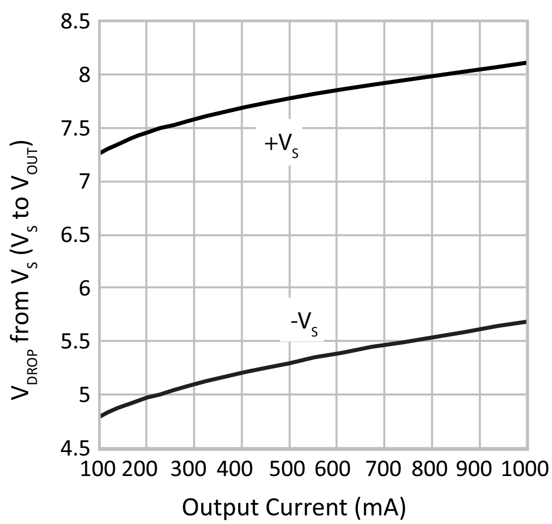
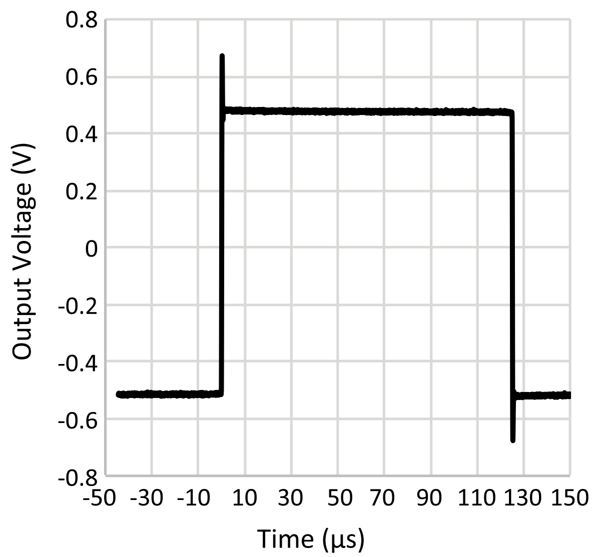


Figure 19: Small Signal Pulse Response



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology's complete Application Notes library, Power Design Tool, Technical Seminar Workbook, and Evaluation Kits.

BOOST OPERATION

With the boost feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_B$ and $-V_B$ are connected to the small signal stages and $+V_S$ and $-V_S$ are connected to the high current output stage. An additional 5V on the $+V_B$ and $-V_B$ pins is sufficient to allow the small signal stages to drive the output stage into the triode region and improve the output voltage swing for extra efficient operation when required. When the boost feature is not needed, $+V_S$ and $-V_S$ are connected to the $+V_B$ and $-V_B$ pins respectively. The $+V_B$ and $-V_B$ pins must not be operated at supply voltages less than $+V_S$ and $-V_S$ respectively.

POWER SUPPLY SEQUENCING

If separate boost supplies are not used, then connect $+V_B$ to $+V_S$ and $-V_B$ to $-V_S$. If separate boost supplies are used, then use the following sequence:

Turn ON Sequence: $\pm V_S$, $\pm V_B$

Turn OFF Sequence: $\pm V_B$, $\pm V_S$

To make sure $\pm V_B$ are not less than 1 diode drop below $\pm V_S$, Apex recommends (small signal) diodes to be connected between $+V_S$ (anode) and $+V_B$ (cathode) and between $-V_S$ (cathode) and $-V_B$ (anode), as shown in Figure 2: Typical Connection (diodes D3 & D4).

Alternatively, replacing diodes D3 and D4 in Figure 2 with 15V, 1W Zener diodes allows for the use of power supply sequence $\pm V_B$, ±VS when switching on, and reversely $\pm V_S$, $\pm V_B$, when switching off. These Zener diodes will prevent voltage difference between V_B and V_S greater than |15V| under either power supply sequence. With $\pm V_B$ turned on before $\pm V_S$, the voltage difference between the two power supply pins will not exceed approximately 15V. This is well within the limit. With the standard power supply sequence $\pm V_S$ will still be clamped at 1 diode voltage drop below $\pm V_B$.

TEMPERATURE SENSING

The case temperature of the PA166 can be monitored using the V_{TEMP} pin. The V_{TEMP} provides an output voltage that corresponds to the change in case temperature. The scale factor of the temperature sensor is 14.7mV/^{o}C. At an ambient temperature of 25^{o}C, the typical output voltage at the pin is 2V. The temperature error of the sensor is $\pm$ 2.2^{o}C.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The R_{CL} resistor sets the precision current limit for the amplifier output. The resistor should be connected inside the feedback loop. The current limit level can be determined by the following equation:

$$R_{CL} = \frac{0.465V}{I_{CL}}$$

INTEGRATED OVER CURRENT FLAG

The PA166 contains an over-current flag pin. Connect a 5 kΩ resistor between this pin and a 5V source referenced to ground, as shown in the typical connection drawing. The over current flag pin can be then used as a 0-5V logic. When the amplifier goes into current limit mode, the pin will sink 1mA current and 5V will be dropped across the resistor. In this configuration, 5V at the pin will indicate no current limit, while 0V at the pin indicates that the amplifier is set in current limit.

INTEGRATED SHUT DOWN FEATURE

PA166 includes a shut-down circuit that allows turning off the output stage of the amplifier, preventing any input signal from passing through the amplifier. The amplifier will work in normal operating mode when the shutdown pin is grounded or left floating. The output is disabled when the shutdown pin is brought high, 5V.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_{S,}$ $-V_{S,}$ $+V_{B,}$ and $-V_B$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the PA166. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) 0.1µF or greater.

POWER SUPPLY PROTECTION

Unidirectional transient Voltage suppressors are recommended as protection on the supply pins. TVS diodes clamp transients to voltages within the power supply rating and clamp power supply reversals to ground. Whether the TVS diodes are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation. Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional TVS diodes prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

ELECTROSTATIC DISCHARGE

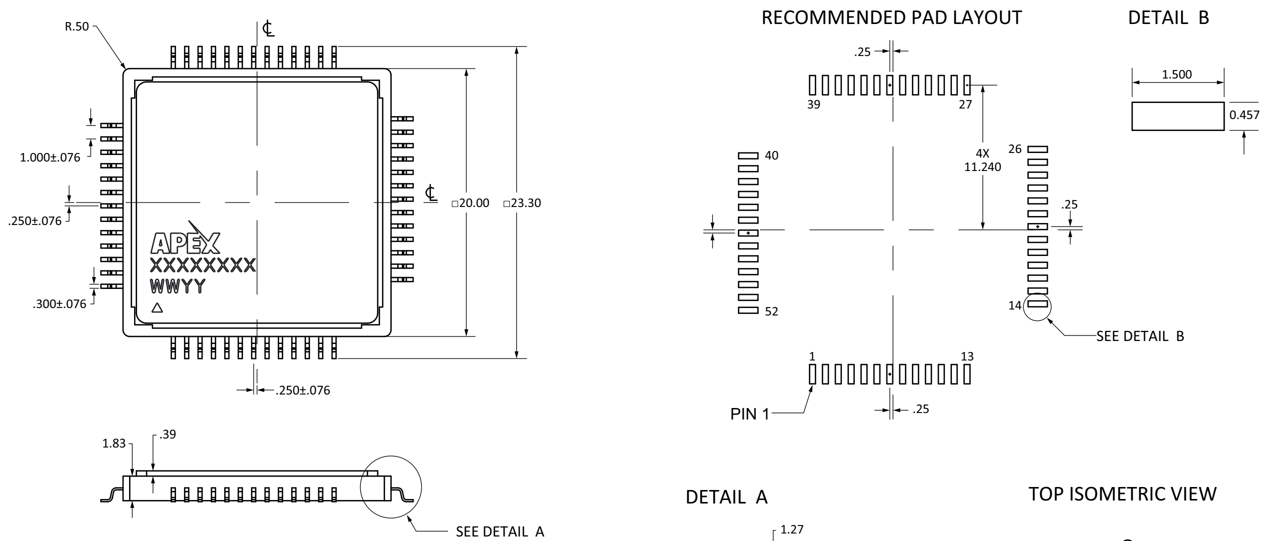
Like many high-performance amplifiers, the PA164 and PA165 are very sensitive to damage due to electrostatic discharge (ESD). Failure to follow proper ESD handling procedures could have results ranging from reduced operation performance to catastrophic damage. Minimum proper handling includes the use of grounded wrist or shoe straps, grounded work surfaces. Ionizers directed at the work in progress can neutralize the charge build up in the work environment and are strongly recommended.

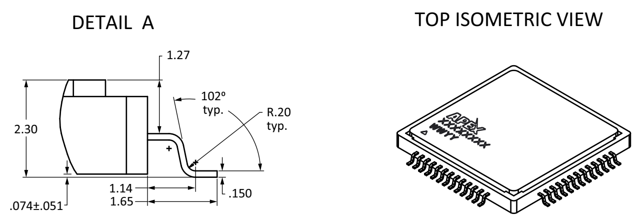
PACKAGE OPTIONS

Part Number	Apex Package Style	Description	MSL[1]
PA166	PQ	52-pin power quad	Level 6

1. The Moisture Sensitivity Level rating according to the JEDEC industry standard classification.

PACKAGE STYLE PQ





Notes:
1. Dimensions are in mm [in]
2. Unless otherwise noted, tolerances are ± 0.254 [0.10]
3. Angle tolerances are ± 3°
3. Pay special attention to the direction pins and pads are shifted with reference to axis
4. All leads to be coplanar within 0.1 [0.004]

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